

Comparative Study of T-Gate Structures in Nano-Channel GaN-on-SiC High Electron Mobility Transistors [†]

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[†] Presented at 8th International Conference on Knowledge Innovation and Invention 2025 (ICKII 2025), Fukuoka, Japan, 22–24 August 2025.

Abstract

We investigated the radio frequency (RF) performance of AlGaIn/GaN high electron mobility transistors (HEMTs) fabricated on silicon carbide substrates, featuring two distinct T-shaped gate structures. A comparative analysis between a silicon nitride (SiN_x)-passivated T-gate and a floating T-gate design reveals significant differences in parasitic capacitance and high-frequency behavior. The floating gate structure effectively reduces fringe capacitance, resulting in improved cut-off frequency (f_T) and maximum oscillation frequency (f_{max}), achieving $f_T = 82.7$ GHz and $f_{max} = 80.2$ GHz, respectively. These enhancements underscore the critical importance of optimizing gate structures to advance GaN-based HEMTs for high-speed and high-power applications. The findings provide valuable insights for the design of future RF and millimeter-wave (mm-wave) devices.

Keywords: AlGaIn/GaN; RF-HEMT; T-shape gate; GaN on SiC substrate; electron beam lithography (EBL)



Academic Editors: Teen-Hang Meen, Chun-Yen Chang and Cheng-Fu Yang

Published: 25 December 2025

Citation: Liu, Y.-C.; Wu, D.-Y.; Hsu, H.-C.; Wang, I.-H.; Wu, M.-C.

Comparative Study of T-Gate Structures in Nano-Channel GaN-on-SiC High Electron Mobility Transistors. *Eng. Proc.* **2025**, *120*, 8. <https://doi.org/10.3390/engproc2025120008>

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1. Introduction

Gallium nitride (GaN)-based HEMTs have emerged as a crucial enabling technology for next-generation radio frequency (RF) and power systems, particularly as wireless communication systems advance toward millimeter-wave frequencies [1–3]. Owing to GaN's exceptional material properties, including its wide bandgap, high electron mobility, and high breakdown electric field [4–6], GaN HEMTs demonstrate outstanding high-frequency performance and power density, making them strong candidates for Ka-band applications in 5G base station infrastructure [7–9].

As the operating frequency increases, enhancing key RF metrics, such as f_T , f_{max} , and power-added efficiency (PAE), becomes increasingly critical. Among various strategies, gate engineering has emerged as a vital approach. In particular, T-shaped gate (T-gate) structures have been widely adopted to reduce gate resistance and improve RF characteristics [10–12]. However, traditional T-gate structures typically utilize a SiN_x layer for mechanical support. While this method provides structural stability, it also introduces additional parasitic capacitance, most notably the gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) components, which negatively impact high-frequency performance [13,14].

In this study, we propose and experimentally demonstrate an optimized floating T-gate structure that eliminates the need for a SiN_x support layer. Instead, we utilize a bilayer photoresist stack composed of oly(methyl methacrylate) A4 and methyl methacrylate

EL11 during the gate fabrication process. Following development and resist removal, an air cavity is created beneath the gate stem. Since air has a dielectric constant close to 1, which is significantly lower than that of SiN_x , this structure effectively suppresses parasitic capacitance.

Experimental results demonstrate that the proposed GaN HEMTs exhibit significant improvements in both f_T and $f_{\max}$ when operating in the Ka-band. Due to space limitations, this paper primarily focuses on the high-frequency characteristics (f_T and $f_{\max}$). Detailed discussions on output power (P_{out}) and PAE, including load-pull measurements, will be presented in a future publication. This straightforward yet effective gate process enhancement significantly improves RF performance without adding fabrication complexity, offering a highly promising pathway for integrating high-efficiency 5G devices.

2. Device Structure and Fabrication

The epitaxial heterostructure was grown on a silicon carbide (SiC) substrate through metal–organic chemical vapor deposition (MOCVD). The layer stack comprised a 60 nm aluminum nitride (AlN) nucleation layer, followed by a 250 nm gallium nitride (GaN) channel, a 14 nm undoped $\text{Al}_{0.28}\text{Ga}_{0.72}\text{N}$ barrier, and a thin 2 nm GaN cap layer. Hall effect characterization confirmed the formation of a high-quality two-dimensional electron gas (2DEG) with an electron mobility of $2028 \text{ cm}^2/\text{V}\cdot\text{s}$ and a sheet carrier concentration of $1.2 \times 10^{13} \text{ cm}^{-2}$.

The T-gate HEMT fabrication process commenced with mesa isolation to delineate the active region, which was realized through inductively coupled plasma reactive ion etching (ICP-RIE) employing chlorine-based chemistry. Subsequently, a Ti/Al/Ti/Au (25/125/45/60 nm) multilayer metal stack was deposited via electron-beam evaporation to form the source and drain electrodes. These contacts were then subjected to rapid thermal annealing (RTA) at 850°C for 30 s to ensure low-resistance ohmic behavior. The gate electrode, composed of Ni/Au (40/400 nm), was deposited using thermal evaporation. To minimize surface-related traps and enhance device stability, a passivation layer was deposited over the device surface. Contact openings were defined using reactive ion etching (RIE), and the final ground-signal-ground (GSG) probe pads were realized by patterning Ni/Au (40/400 nm) interconnect metallization. The completed device structure is shown in Figure 1.

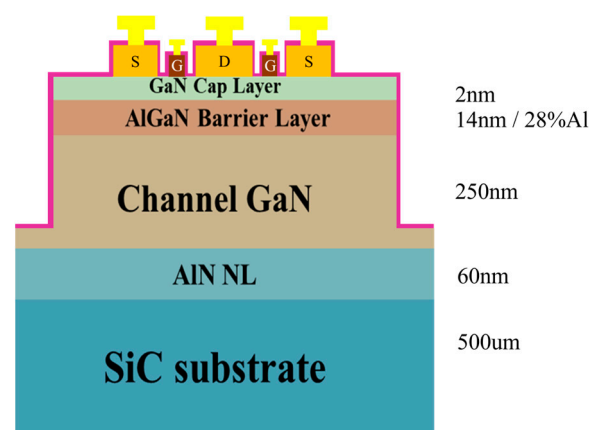


Figure 1. Cross-sectional schematic illustrating the structure of the fabricated GaN-based T-gate HEMT.

Two distinct T-gate configurations were investigated in this work. For Sample A, the T-gate structure was fabricated using a dual-layer photoresist system with different sensitivities. In contrast, Sample B incorporated a SiN_x layer at the base of the T-gate stem. The

gate region—defining both the footprint and gate length—was patterned through electron beam lithography (EBL), followed by etching via RIE to complete the structure definition.

Both fabricated devices possessed a gate length (L_G) of 100 nm and a total gate width (W_G) of $50\ \mu\text{m} \times 2$, with symmetric gate-to-source (L_{GS}) and gate-to-drain (L_{GD}) spacings of $1.6\ \mu\text{m}$.

3. Results and Discussion

3.1. GaN-HEMTs DC Characteristics

Figure 2 presents the linear-scale transfer characteristics and corresponding transconductance (G_m) for Samples A and B. The threshold voltage (V_{th}) was extracted at a drain current density of $1\ \text{mA}/\text{mm}$, taking specific contact resistance into account. Sample A exhibited a V_{th} of $-3.6\ \text{V}$ and a peak G_m of $319\ \text{mS}/\text{mm}$, while Sample B showed a V_{th} of $-2.9\ \text{V}$ and a peak G_m of $259\ \text{mS}/\text{mm}$. Figure 3 shows the output characteristics with the gate voltage (V_{GS}) swept from $-5\ \text{V}$ to $5\ \text{V}$. Sample A achieves a maximum drain saturation current density ($J_{DS, \max}$) of $1561\ \text{mA}/\text{mm}$, which is slightly higher than that of Sample B at $1175\ \text{mA}/\text{mm}$. The corresponding ON-resistances (R_{on}) are $3.5\ \text{ohm}\cdot\text{mm}$ and $3.3\ \text{ohm}\cdot\text{mm}$, respectively.

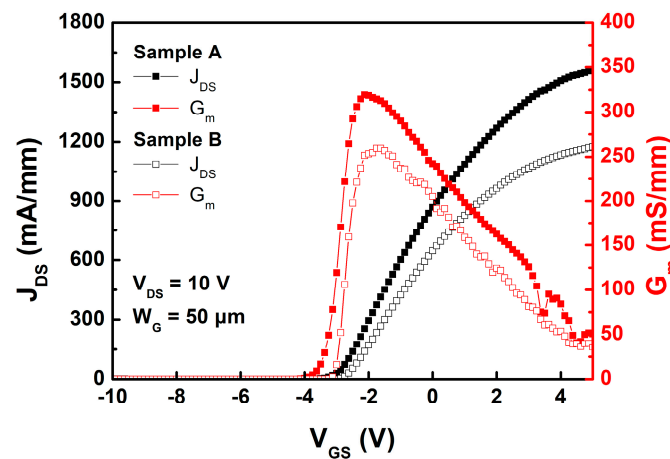


Figure 2. Comparison of the transfer and transconductance (G_m) characteristics for Samples A and B.

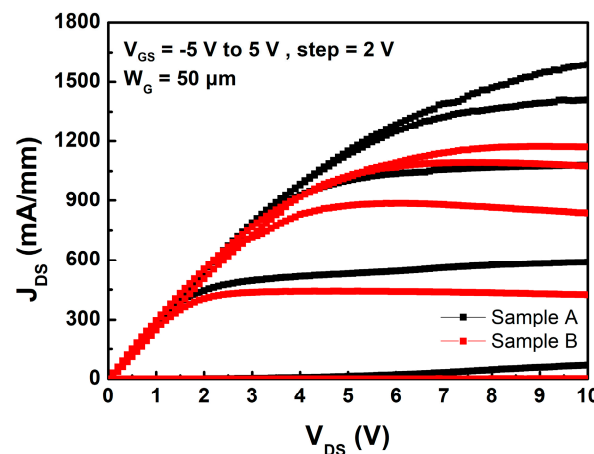


Figure 3. Output characteristics comparison between Samples A and B.

Figure 4 illustrates the transfer characteristics and gate leakage current plotted on a logarithmic scale. The on/off current ratios are 1.2×10^4 for Sample A and 3×10^6 for Sample B, indicating better off-state suppression in Sample B. The subthreshold swing (SS) was extracted from the log-scale transfer curve by analyzing five data points in the

subthreshold region ($J_{DS} < 1$ mA/mm). The extracted SS values are 438 mV/dec and 167 mV/dec for Samples A and B, respectively, suggesting weaker gate control in Sample A. The gate leakage current at $V_{GS} = 5$ V was measured to be 3.7×10^{-4} mA/mm for Sample A and 1×10^{-3} mA/mm for Sample B.

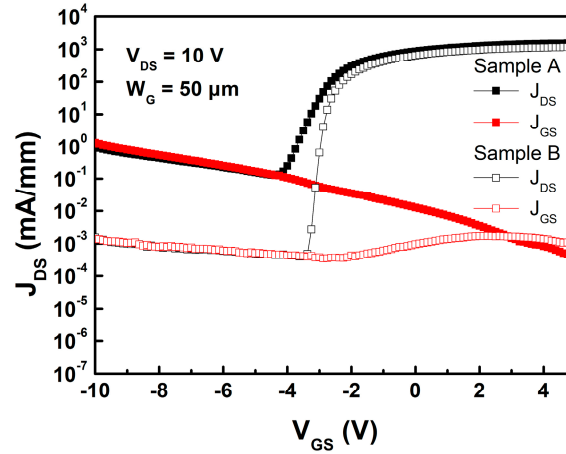


Figure 4. Comparison of the transfer characteristics and gate leakage current (in logarithmic scale) for Samples A and B.

3.2. GaN-HEMTs Small Signal Performance

Figure 5a,b present the small-signal characteristics of Samples A and B, specifically illustrating f_T and f_{max} . Measurements were performed under a bias condition of $(V_{GS}, V_{DS}) = (-2$ V, 10 V), where the gate voltage was selected to correspond to the peak transconductance ($G_{m, max}$) for both samples. Sample A achieved f_T and f_{max} values of 82.7 GHz and 80.2 GHz, respectively, while Sample B exhibited lower values of 66.2 GHz and 50.1 GHz.

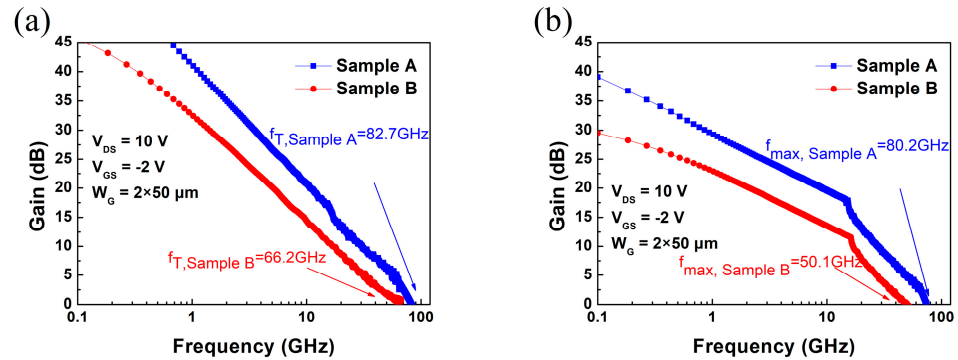


Figure 5. (a) Current gain and (b) maximum available gain versus frequency for Samples A and B. Sample A shows higher f_T and f_{max} due to lower parasitic effects.

The superior high-frequency performance of Sample A is primarily attributed to its reduced parasitic capacitances. Smaller capacitances result in lower signal propagation delays, thereby directly improving the device's frequency response. In addition, reduced parasitic capacitance leads to shorter carrier transit times and faster signal transitions, collectively contributing to the higher f_T and f_{max} observed in Sample A.

This improvement is closely related to the gate structure. The floating T-gate used in Sample A provides superior electrostatic control and lower overlap capacitance compared to the conventional T-gate fabricated on a SiN_x dielectric layer. This structural advantage effectively reduces parasitic effects, enhances signal integrity, and supports high-speed operation. Therefore, the floating T-gate architecture is particularly well suited for high-

frequency and millimeter-wave applications, such as next-generation RF front ends and 5G base stations. Table 1 summarizes key characteristics and measured data of both samples for easy comparison.

Table 1. Summary of key DC and small-signal characteristics of Samples A and B for performance comparison.

	Sample A	Sample B
V_{th} (V)	−3.6	−2.9
J_{DS} (mA/mm)	1561	1175
G_m (mS/mm)	319	259
R_{on} (Ω -mm)	3.5	3.3
On/off ratio	1.2×10^4	3×10^6
S.S. (mV/dec)	438	167
f_T (GHz)	82.7	66.2
f_{max} (GHz)	80.2	50.1

4. Conclusions

We report the successful realization of two variants of 100 nm T-gate AlGaIn/GaN HEMTs fabricated on SiC substrates, followed by a thorough investigation of their DC and RF behavior. To improve high-frequency performance, a floating T-gate configuration was implemented by removing the conventional SiN_x supporting layer, effectively lowering the parasitic capacitance. Experimental observations show that this structural modification enhances the peak drain current from 1175 mA/mm to 1561 mA/mm and raises the transconductance from 259 mS/mm to 319 mS/mm. In RF characterization, the floating T-gate device exhibits f_T of 82.7 GHz and f_{max} of 80.2 GHz. These results clearly demonstrate that the gate configuration plays a crucial role in determining RF performance, validating the potential of the proposed fabrication process for advanced high-power and high-frequency GaN device applications.

Author Contributions: Conceptualization, Y.-C.L. and M.-C.W.; investigation, H.-C.H. and I.-H.W.; formal analysis, Y.-C.L. and D.-Y.W.; data curation, Y.-C.L., H.-C.H. and I.-H.W.; writing—original draft preparation, Y.-C.L.; writing—review and editing, Y.-C.L. and M.-C.W.; supervision, M.-C.W.; project administration, M.-C.W.; funding acquisition, M.-C.W. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the Ministry of Science and Technology, Taiwan, under Grant No. 112-2622-E-007-020.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: No new data were created or analyzed in this study.

Conflicts of Interest: The authors declare no conflict of interest.

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