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A New Transformer-Less Structure for a Boost DC-DC Converter with Suitable Voltage Stress

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Abstract: In this paper, a new structure is proposed for a boost dc–dc converter based on the voltage-lift (VL) technique. The main advantages of the proposed converter are its lack of transformer, simple structure, free and low input current ripple, high voltage gain capability by using an input source, suitable voltage stress on semiconductors and lower output capacitance. Herein, the analysis of the proposed converter operating and its elements voltage and current relations in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are presented, and the voltage gain of each operating mode is individually calculated. Additionally, the critical inductance, current stress of switches, calculation of passive components' values and efficiency are analyzed. In addition, the proposed converter is compared with other studied boost converters in terms of ideal voltage gain in the CCM and the number of active and passive components, maximum voltage stress on semiconductors, and situation of input current ripples. The correctness of the theoretical concepts is examined from the experimental results using the laboratory prototype.

Keywords: DC-DC converter; boost converter; voltage-lift technique; critical inductance

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1. Introduction

The reduction of fossil fuels, increasing energy demands and increasing air pollution has created demand for energy production in the field of renewable energies such as wind turbines, solar cells and fuel cells. The structure of this kind of energy produces low level dc voltage at output, therefore, dc–dc converters are used in the structure of these types of energy resources to achieve different output voltage at the output side for different duty cycle (D) [1,2]. These types of converters are classified into isolated and non-isolated categories. Control of these converters can be achieved by the pulse width modulation (PWM) and switching frequency variation techniques [3,4]. A high-frequency transformer is used in the structure of the isolated converters as it makes a high level of insulation. The electrical insulation is the most important factor in selecting dc–dc converters, and especially in some applications such as batteries in order to provide suitable galvanic isolation; however, using high-frequency transformers causes increases in the size and cost [3]. On the other hand, the problem of leakage inductance and its energy are other important drawbacks of these types of converters.

Knowing that isolated converters have a better level of insulation than non-insulated converters, the non-isolated converters such as the conventional non-isolated boost converter in theory have some suitable features, such as direct connection of input inductor (as filter), free current ripple, less capacitance of output capacitor and filter size, less stress on the elements, higher response ratio and infinite output gain for duty cycle ratio near to one. However, in practice, due to electromagnetic interference (EMI) of elements and the stress between them, the switch protection against overvoltage, reverse recovery problems and the stability, reduction of efficiency and power density, the duty cycle ratio is limited to approximately 0.8 [5,6]. Therefore, new structures with different techniques have been introduced to achieve higher voltage gain compared to conventional boost converters.

The interleaving or cascade connection technique is one of the presented techniques for increasing voltage gain [7,8]. In these techniques, the higher output voltage gain can be achieved for low duty cycle ratios. However, the converters based on these techniques have less advantages compared to conventional boost converters due to the voltage across the main switches, increasing size and cost, interference problem and complex control system.

The switched-capacitor (SC) technique is the other technique which has been introduced to increase the output voltage gain. In this technique, a number of diodes and capacitors are combined and provide the higher output voltage and lower voltage stress. However, the current stress of switching and hard switching, high input current ripple increases the losses of the switching and conductance of active switches, reduces the efficiency and makes the control system more complex for this type converter [9,10]. On the other hand, the current ripple is significant in this technique.

The coupled inductor or high frequency transformer technique is introduced from other techniques [11,12]. In this technique, the desired output voltage can be achieved by increasing the turn ratio of the transformer. In addition, the current stress of switching and the voltage stress across main switch are solved in this technique [13,14]. However, increasing the physical dimensions of the converters is the drawback of this method. In addition, the leakage inductance and its energy are the main problems of this technique. Even though the problem of leakage inductance and increasing the efficiency is solved by non-dissipative snubber or active clamp circuits [15], use of the active clamp circuit in this technique makes the control process more complex.

The technique to combine multiple converters together is another technique to achieve higher voltage gain and lower voltage across switches [16,17], although its application is limited due to the balance problem of the series capacitor at output side.

The other technique for boosting voltage is the switched-boost network where the impedance network has been replaced to input inductor. This method provides higher voltage gain with lower duty cycles but the high input current ripple is the main drawback of it [18].

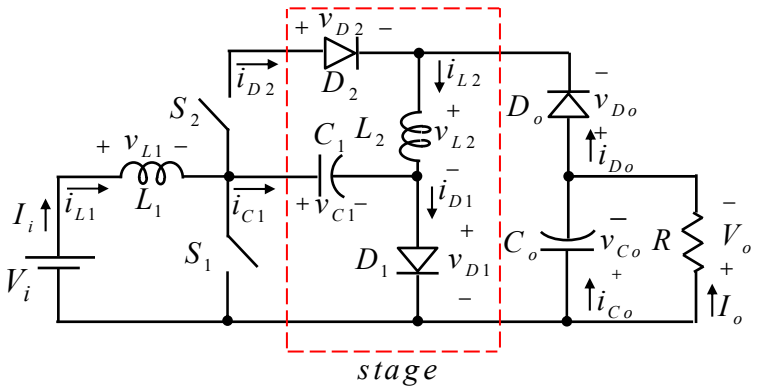
The voltage-lift (VL) technique is another method to increase the output voltage gain that is used in many studies [19–22]. This technique is discussed for converters with periodic switching. This technique provides simpler structure, less element stress, less current ripple, high efficiency, high power density and lower price compared with other discussed techniques. The increasing process of this technique is step to step. In addition, the voltage multiplier cells (VMCs), which include a combination of diode and capacitor can be used to achieve higher output voltage gain [23]. As the voltage stress on the main switch is low, the Schottky diode with low reverse recovery time can be used to reduce the conduction losses.

This paper proposes a new high-gain transformer-less structure for a boost dc–dc converter based on the VL technique, such as in [6,19–22], with a simple structure with suitable voltage stress on semiconductors, free and low input current ripple by using one input voltage source and lower output capacitance. Although the proposed converter and [6] has the same number of passive components (inductors and capacitors) and ideal voltage gain but the proposed converter has one less active component (one diode), its non-ideal voltage gain, total losses and efficiency will be improved. In this paper the following procedure will be presented: first, the relations between voltage and current of each element in CCM and DCM are calculated as well as voltage gain in each mode. Then, the critical inductances, switching current stress, passive components value and efficiency calculations are discussed. In the following, the proposed converter in this paper is compared with some other presented boost converters in studies in terms of different indexes. Finally, the validity of theoretical concepts is examined by the experimental results using the laboratory prototype.

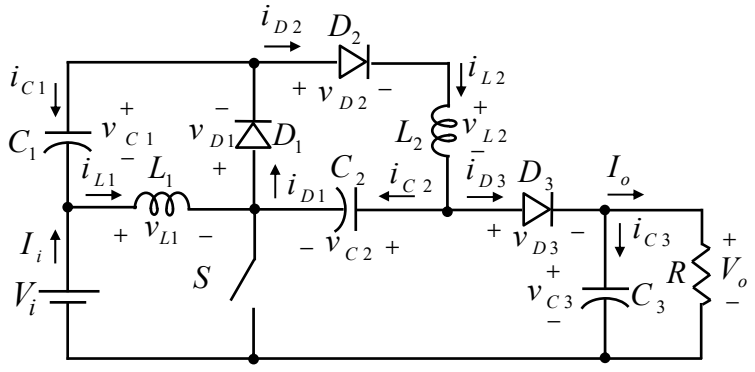
2. The Proposed Converter Structure

Several voltage-lift structures for dc–dc boost converter which have been presented in lecturers are shown in Figure 1a–c [20–22]. Additionally, the structure of the proposed converter and its drive circuit are shown in Figure 1d. As shown in Figure 1, the proposed converter has two power electronic switches (such as in [20,22]), two inductors (such as in [20–22]), three capacitors and three diodes (such as in [20,21]) and the proposed converter's driving circuits consist of a microcontroller to providing PWM and a gate driver such as TLP250, a logical IC to generate the opposite PWM wave because the two switches of the proposed converter acts as mutually opposed at a period. The transformer-less and simple structure, direct connection of inductor to the input with lower input current ripple (as filter), lower output capacitance, suitable voltage stress on semiconductors and increasing step-to-step voltage to output are the features of the proposed converter while its drawback is the use of two switches that are switched mutually opposed at a period. For the convenience of analysis, it is intended that:

(a) The proposed converter is in steady state, and then the output voltage is assumed to be constant;
(b) The capacitors are large enough and as a result the capacitors voltage can be assumed to be constant in each switching cycle;
(c) The switches and diodes are ideal.



(**a**)



(**b**)

Figure 1. *Cont.*

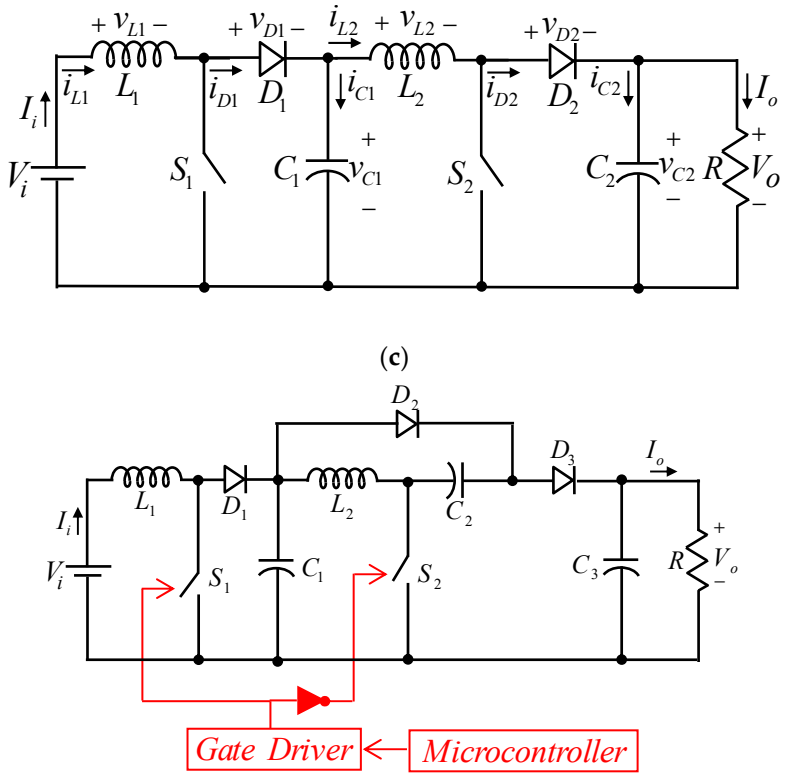


Figure 1. (**a**) The presented converter in [20], (**b**) the presented converter in [21], (**c**) the presented converter in [22], (**d**) the proposed converter.

2.1. Operating Principle

Here, the operating principle of the proposed converter is described with details in CCM and DCM as follows:

2.1.1. The Time Intervals of T_{on} in CCM and (t_0, t_1) in DCM:

In this time interval that the switch S_1 is turned on, the switch S_2 is turned off, the diodes of D_1 and D_2 are reversely biased and the D_3 diode is directly biased, the inductor L_1 is directly connected to the input voltage source (V_i), as a result, its current is linearly increased from its minimum value (I_{LV1}) to its maximum value (I_{LP1}). During this time interval, the inductor L_2 and the capacitors C_1 and C_2 are connected in series and provided the load current and the capacitor C_3 charge current. In this case, the inductor L_2 current is gradually decreased from its maximum value (I_{LP2}) to its minimum value (I_{LV2}). Additionally, the voltage of the capacitors C_1 and C_2 are decreased from their maximum values (V_{CP1}) (V_{CP2}) to their minimum values (V_{CV1}) (V_{CV2}). During this time interval, the capacitor C_3 voltage and its stored energy are increased from its minimum value (V_{CV3}) to its maximum value (V_{CP3}). In DCM, this time interval continues until the current of the inductor L_2 goes to zero.

2.1.2. The Time Interval of (t_1, t_2) in DCM:

In this time interval, the switch S_1 is still turned on, the switch S_2 is turned off, and the diodes of D_1 and D_2 are reversely biased and as the current the inductor L_2 is zero, therefore, the D_3 diode is reversely biased as well. As a result, the inductor L_1 current is increased to I_{LP1}. In addition, the voltage of the capacitors C_1 and C_2, and their stored energy remain unchanged. In this condition, the load current is provided by the capacitor C_3 discharge current, as a result, its voltage is gradually decreased.

2.1.3. The Time Intervals of T_{off} in CCM and (t_2, t_3) in DCM:

This interval begins when the switch S_1 is turned off and the switch S_2 is turned on. In this state, the diodes of D_1 and D_2 are directly biased while the D_3 diode is still reversely biased. Therefore, the inductor L_1 is connected to the inductor L_2 and the capacitors C_1 and C_2. As a result, the inductor L_1 current is gradually decreased to I_{LV1} while the inductor L_2 current and the voltage of the capacitors C_1 and C_2 is increased to their maximum values. As the load current is provided by the capacitor C_3 discharge current, therefore, the capacitor C_3 voltage is decreased to minimum value. In DCM, this time interval continues until the current of L_1 goes to zero.

2.1.4. The Time Interval of (t_3, t_4) in DCM:

In this time interval, the switch S_1 is still turned off, the switch S_2 is turned on and the D_3 diode is reversely biased. Due to the fact that the inductor L_1 current is equal to zero, the diodes of D_1 and D_2 are reversely biased. Therefore, the stored energy of the inductor L_2 and the capacitors C_1 and C_2 remains unchanged. On the other hand, the capacitor C_3 stored energy is still released to load, so, the capacitor C_3 voltage is gradually decreased.

In the following sections, indices 1 and 2 represent time intervals of T_{on} and T_{off} in CCM, respectively, and indices 1, 2, and 3 indicate time intervals of (t_0, t_1), (t_1, t_2) and (t_2, t_3) in DCM, respectively. Additionally, v and i show voltage and current, respectively.

2.2. Analysis of Proposed Converter in CCM

By applying kirchhoff's voltage law (KVL) in Figure 1d, we would have:

$$v_{L1,1} = V_i = L_1 \frac{di_{L1,1}}{dt} = L_1 \frac{\Delta i_{L1}}{T_{on}} \tag{1}$$

Applying KVL in Figure 1d, the following is obtained:

$$v_{L1,2} = V_i - v_{C1,2} = L_1 \frac{di_{L1,2}}{dt} = -L_1 \frac{\Delta i_{L1}}{T_{off}} \tag{2}$$

Applying the voltage-second principle for L_1, defining duty cycle for dc–dc converter as $D = T_{on}/T$ and assuming sufficiently large capacitance for C_1, we get:

$$v_{C1,2} = \frac{1}{1-D} V_i = v_{C1} = v_{C1,1} \tag{3}$$

By applying KVL in Figure 1d, we get the following equation:

$$v_{L2,1} = v_{C1,1} + v_{C2,1} - V_o = L_2 \frac{di_{L2,1}}{dt} = -L_2 \frac{\Delta i_{L2}}{T_{on}} \tag{4}$$

By applying KVL in Figure 1d, the below relation is obtained:

$$v_{L2,2} = v_{C2,2} = L_2 \frac{di_{L2,2}}{dt} = L_2 \frac{\Delta i_{L2,2}}{T_{off}} \tag{5}$$

From Figure 1d and considering sufficiently large capacitance for C_2, the following relation is obtained:

$$v_{C2} = v_{C2,1} = v_{C2,2} = v_{C1} \tag{6}$$

According to Figure 1d, the following equation is obtained for the average voltage of the capacitor C_3:

$$v_{C3} = V_o \tag{7}$$

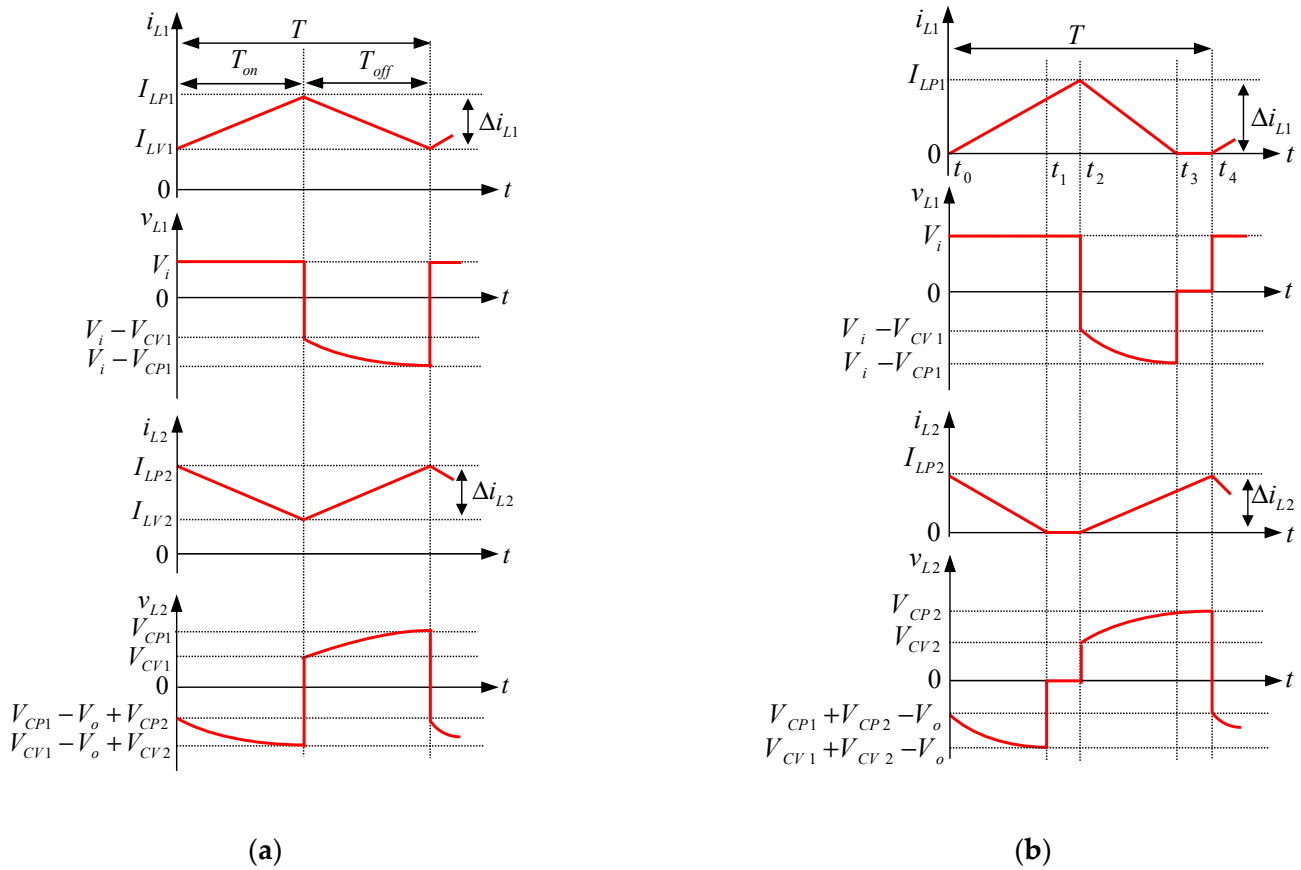
Applying voltage-second principle for L_2 and substituting (4) and (5), the voltage gain of the proposed converter in CCM is extracted as follows:

$$M = \frac{V_o}{V_i} = \frac{1+D}{D(1-D)} \tag{8}$$

Other voltage and current relations in CCM are presented in Table 1. Additionally, the voltage and current waveforms of inductors in CCM are shown in Figure 2a.

Table 1. The voltage and current equations of elements in CCM and DCM.

Element/Time Interval	CCM		DCM			
	T_{on}	T_{off}	(t_0, t_1)	(t_1, t_2)	(t_2, t_3)	(t_3, t_4)
C_1	$i_{C1,1} = i_{C2,1} = i_{L2,1}$	$i_{C1,2} = i_{L1,2} - i_{L2,2} - i_{C2,2}$	$i_{C1,1} = i_{C2,1} = i_{L2,1}$	0	$i_{C1,3} = i_{L1,3} - i_{C2,3} - i_{L2,3}$	0
C_2	$i_{C1,1} = i_{C2,1} = i_{L2,1}$	$i_{C2,2} = i_{L1,2} - i_{L2,2} - i_{C1,2}$	$i_{C1,1} = i_{C2,1} = i_{L2,1}$	0	$i_{C2,3} = i_{L1,3} - i_{L2,3} - i_{C1,3}$	0
C_3	$i_{C3,1} = i_{L2,1} - I_o$	$i_{C3,2} = -I_o$	$i_{C3,1} = i_{L2,1} - I_o$		$i_{C3,4} = -I_o$	
D_1	$v_{D1,1} = -v_{C1,1}$	$i_{D1,2} = i_{L2,2} + i_{C1,2}$	$v_{D1,2} = -v_{C1,2}$		$i_{D1,3} = i_{L1,3} - i_{C2,3}$	$v_{D1,4} = V_i - v_{C1,4}$
D_2	$v_{D2,1} = -v_{C1,1} - v_{C2,1} + v_{L2,1}$	$i_{D2,2} = i_{C2,2}$	$v_{D2,2} = -v_{C1,2} - v_{C2,2} - v_{L2,2}$		$i_{D2,3} = i_{L1,3} - i_{C1,3} - i_{L2,3}$	$v_{D2,4} = V_i - v_{C2,2}$
D_3	$i_{D3,1} = i_{L2,1}$	$v_{D3,2} = v_{C2,3} - V_o$	$i_{D3,1} = i_{L2,1}$		$v_{D3,4} = v_{C2,4} - V_o$	
S_1	$i_{S1} = i_{L1}$	$v_{S1} = V_i - v_{L1,2}$	$i_{S1} = i_{L1}$		$v_{S1} = V_i - v_{L1,3}$	$v_{S1} = V_i$
S_2	$v_{S2} = v_{C1,1} - v_{L2,1}$	$i_{S2} = i_{L2} + i_{C2}$	$v_{S2} = v_{C1,1} - v_{L2,1}$	$v_{S2} = v_{C1,2}$	$i_{S2} = i_{L2} + i_{C2}$	$v_{S2} = v_{C1,4} - v_{L2,4}$



(**a**) (**b**)

Figure 2. The voltage and current waveforms for inductors: (**a**) in CCM; (**b**) in DCM.

2.3. Analysis of the Proposed Converter in DCM

By applying KVL in Figure 1d, we get:

$$v_{L1,2} = V_i = L_1 \frac{di_{L1,2}}{dt} = L_1 \frac{\Delta i_{L1}}{\Delta t} \tag{9}$$

By applying KVL in Figure 1d, it is resulted that:

$$v_{L1,3} = V_i - v_{C1,3} = L_1 \frac{di_{L1,3}}{dt} = -L_1 \frac{\Delta i_{L1}}{\Delta t} \tag{10}$$

At (t_3, t_4), the inductor L_1 voltage is equal to:

$$v_{L1,4} = 0 \tag{11}$$

Applying the voltage-second principle for L_1, defining different time intervals in DCM as $D'_1 = (t_1 - t_0)/T$, $D'_2 = (t_2 - t_1)/T$, $D'_3 = (t_3 - t_2)/T$ and $D'_4 = (t_4 - t_3)/T$, and duty cycle in DCM as $D' = D'_1 + D'_2$, the following equation is obtained for the capacitor C_1:

$$v_{C1,3} = \frac{D'_1 + D'_2 + D'_3}{D'_3} = v_{C1,1} = v_{C1,2} = v_{C1,4} = v_{C1} \tag{12}$$

By applying KVL in Figure 1d, the below relation is resulted:

$$v_{L2,1} = v_{C1,1} + v_{C2,1} - V_o = L_2 \frac{di_{L2,1}}{dt} = -L_2 \frac{\Delta i_{L2}}{\Delta t} \tag{13}$$

The following equation is true for the inductor L_2 voltage at (t_1, t_2):

$$v_{L2,2} = 0 \tag{14}$$

By applying KVL in Figure 1d, we have:

$$v_{L2,4} = v_{C1,4} = L_2 \frac{di_{L2,4}}{dt} = L_2 \frac{\Delta i_{L2}}{\Delta t} \tag{15}$$

From Figure 1d and assuming large enough capacity for C_1, the following equation is derived:

$$v_{C1} = v_{C2} \tag{16}$$

From Figure 1d, the below relation can be resulted:

$$v_{C3} = V_o \tag{17}$$

Applying the voltage-second principle for L_2 and substituting (13) to (15), the proposed converter voltage gain in DCM is obtained as follows:

$$M' = \frac{V_o}{V_i} = \frac{1}{2}\left[\frac{1+D}{D} + \sqrt{\left(\frac{1+D}{D}\right)^2 + \frac{4D^2}{K}}\right] \tag{18}$$

where $K = \frac{2L_1}{RT}$. Other voltage and current relations in DCM are presented in Table 1. Meanwhile, the voltage and current waveforms of inductors in DCM are shown in Figure 2b.

3. Critical Inductance Calculation

The boundary between CCM and DCM in a dc–dc converter can be determined by the critical inductance. In the proposed converter, the performance can be identified by determining the critical inductance $L_1(L_{C1})$ and $L_2(L_{C2})$. $I_{LV1} + I_{LV2} = 0$ is true for the proposed converter in critical mode. Applying the current-second principle for capacitor C_3 in CCM, the following equations can be derived:

$$I_{LP2} = \frac{V_i}{2L_2} T + \frac{I_o}{D} \tag{19}$$

Substituting (19) into (5) and considering $I_{LV2} = 0$, yields the following equation for L_{C2}:

$$L_{C2} = \frac{D^2(1-D)R}{2(1+D)f} \tag{20}$$

Applying the current-second principle for capacitor C_1 in CCM, the below relation is obtained:

$$I_{LP1} = \frac{V_i}{L_1}T + \frac{V_o}{V_i}\frac{I_o}{D} \tag{21}$$

The value of L_{C1} is obtained using (2) and (21) as follows:

$$L_{C1} = \frac{D^3(1-D)^2R}{2(1+D)^2f} \tag{22}$$

According to (20) and (22), it can be concluded that L_{C2} and L_{C1} depends on R, f and D.

4. Switching Stress Calculation

By appropriate selection of semiconductor elements and switches the cost of a converter can be reduced optimal amount. One of the key devices are power electronics switches and the calculation of peak current flow switch (PCFS) can play an important role in choosing the type of switches. In the following, the PCFS for S_1 and S_2 are discussed.

4.1. Calculation of PCFS in CCM

The current of switch S_1 (i_{S1}) is increased to its peak value (i_{SP1}^{CCM}) at $t = T_{on}$ and is calculated as follows:

$$i_{SP1}^{CCM} = I_{LP1} \tag{23}$$

The maximum PCFS of the switch S_1 in CCM ($i_{SP1,\max}^{CCM}$) is achieved by substituting $L_1 = L_{C1}$ as follows:

$$i_{SP1,\max}^{CCM} = \frac{2V_o^2}{DV_i}T + \frac{V_o}{V_i}\frac{I_o}{D} \tag{24}$$

The PCFS of S_2 in CCM (i_{SP2}^{CCM}) at $t = T_{on}$ is as follows:

$$i_{SP2}^{CCM} = I_{LP2} + i_{C2} \tag{25}$$

Using (19) and considering $L_2 = L_{C2}$, the maximum PCFS of the switch S_1 in CCM ($i_{SP2,\max}^{CCM}$) is obtained as follows:

$$i_{SP2,\max}^{CCM} = \frac{V_o}{D}T + \frac{I_o}{D} + i_{C2} \tag{26}$$

4.2. Calculation of PCFS in DCM

At $t = t_2$, the peak current flow of the switch S_1 in DCM (i_{SP1}^{DCM}) is equal to:

$$i_{SP1}^{DCM} = I_{LP1} \tag{27}$$

At $t = t_2$, the peak current flow of the switch S_2 in DCM (i_{SP2}^{DCM}) is as follows:

$$i_{SP2}^{DCM} = I_{LP2} + i_{C2} \tag{28}$$

5. Design Consideration

The calculations of the ripples of inductors current and capacitors voltage have a key role in determining the values of the inductors and capacitors, and the values of the inductors and capacitors are determined from these relations. Neglecting inductors current ripple, the root-means-square (rms) of current in CCM, I_{L1} and I_{L2}, are calculated

and shown in Table 2. The allowed range for inductors current ripple, $\%x_{L1}$ and $\%x_{L2}$, are calculated from (1) to (4) and are also shown in Table 2. Considering $C_1 = C_2$ and $|\Delta v_{C1}| = |\Delta v_{C2}|$, the capacitors voltage ripple in CCM are calculated from (5) and (7).

Table 2. Ripples calculations for inductors current and capacitors voltage.

Element	Relation	
L_1	$I_{L1} = \frac{(1+D)^2}{D^2(1-D)^2}\frac{V_i}{R}$	$\%x_{L1} = \frac{\Delta i_{L1}}{I_{L1}} = \frac{D^3(1-D)^2R}{L_1 f(1+D)^2}$
L_2	$I_{L2} = \frac{D(1+D)}{D^2(1-D)^2}\frac{V_i}{R}$	$\%x_{L2} = \frac{\Delta i_{L2}}{I_{L2}} = \frac{D(1-D)^2R}{L_2 f(1+D)}$
$C_1 = C_2$	$\|\Delta v_{C1}\| = \|\Delta v_{C2}\| = \frac{D}{2C_1 f}\left[\frac{(1+D)V_i}{D^2(1-D)^2R}\right]$	$\%x_{C1} = \%x_{C2} = \frac{\|\Delta v_{C1}\|}{v_{C1}} = \frac{D(1+D)}{2RC_1 f D^2(1-D)}$
C_3	$\|\Delta v_{C3}\| = \frac{I_o(1-D)}{C_3 f}$	$\%x_{C3} = \frac{\|\Delta v_{C3}\|}{v_{C3}} = \frac{1-D}{RC_3 f}$

6. Efficiency Analysis

Neglecting ripples of the inductors current and the capacitors voltage, the root-mean-square (RMS) current relations of inductors and their losses are given as follows:

$$I_{L1} = \frac{1+D}{D(1-D)} I_o \tag{29}$$

$$I_{L2} = \frac{1+D}{3D(1-D)} I_o \tag{30}$$

$$P_{L1} = r_{L1} I_{L1}^2 + (K f^{\alpha} B_{ac}^{\beta} W_{tfe})(10^{-3}) \tag{31}$$

$$P_{L2} = r_{L2} I_{L2}^2 + (K f^{\alpha} B_{ac}^{\beta} W_{tfe})(10^{-3}) \tag{32}$$

The diodes RMS current relations are calculated as follows:

$$I_{D1} = \frac{1+D}{D}\sqrt{\frac{1}{1-D}} I_o \tag{33}$$

$$I_{D2} = \frac{1+D}{D}\sqrt{\frac{1}{(1-D)}\frac{I_o}{3}} \tag{34}$$

$$I_{D3} = I_{C3} + I_o = \frac{1+D}{1-D}\sqrt{\frac{1}{D}\frac{I_o}{3}} \tag{35}$$

$$P_{D1} = V_{F1} I_{D1,ave} + r_{D1} I_{D1}^2 + 0.25 Q_{rr} V_{D1} f \tag{36}$$

$$P_{D2} = V_{F2} I_{D2,ave} + r_{D2} I_{D2}^2 + 0.25 Q_{rr} V_{D2} f \tag{37}$$

$$P_{D3} = V_F I_{D3,ave} + r_D I_{D3}^2 + 0.25 Q_{rr} V_D f \tag{38}$$

The RMS values of C_1 and C_2 currents are obtained as follows:

$$I_{C1} = I_{C2} = I_o\sqrt{D + \left(\frac{1+D}{3D}\right)^2 \frac{1}{1-D}} \tag{39}$$

Considering $Q_{Co}^{+} = Q_{Co}^{-}$, the RMS current of C_3 current is as follows:

$$I_{C3} = I_o\sqrt{\frac{1}{9D}\left(\frac{1+D}{1-D}\right)^2 + 1 - D} \tag{40}$$

The capacitors losses are calculated as follows:

$$P_{Cn} = \sum_{N=1}^{3} r_{CN} I_{CN}^2 \tag{41}$$

The switches RMS current and their losses are equal to:

$$I_{S1} = \frac{1+D}{1-D}\sqrt{\frac{1}{D}}I_o \tag{42}$$

$$I_{S2} = \frac{1+D}{D}\sqrt{\frac{1}{1-D}\frac{2I_o}{3}} \tag{43}$$

$$\begin{aligned} P_{S1} &= r_{DS-on} I_{S1}^2 + 0.5(t_r + t_f) I_{S1,ave} V_{S1} f + 0.5 C_{OSS} V_{S1}^2 f \\ &\quad + 0.25 f Q_{rr,BD} V_{S1} + r_{BD1,} I_{BD1}^2 + V_{BF1} I_{BD1,ave} \end{aligned} \tag{44}$$

$$\begin{aligned} P_{S2} &= r_{DS-on} I_{S2}^2 + 0.5(t_r + t_f) I_{S2,ave} V_{S2} f + 0.5 C_{OSS} V_{S2}^2 f \\ &\quad + 0.25 f Q_{rr,BD} V_{S2} + r_{BD2,} I_{BD2}^2 + V_{BF2} I_{BD2,ave} \end{aligned} \tag{45}$$

Finally, the total loss and efficiency are calculated as follows:

$$P_{Loss} = P_{L1} + P_{L2} + P_{S1} + P_{S2} + P_{Cn} + P_{D1} + P_{D2} + P_{D3} \tag{46}$$

$$\eta\% = \frac{P_{out}}{P_{out} + P_{Loss}} \times 100 \tag{47}$$

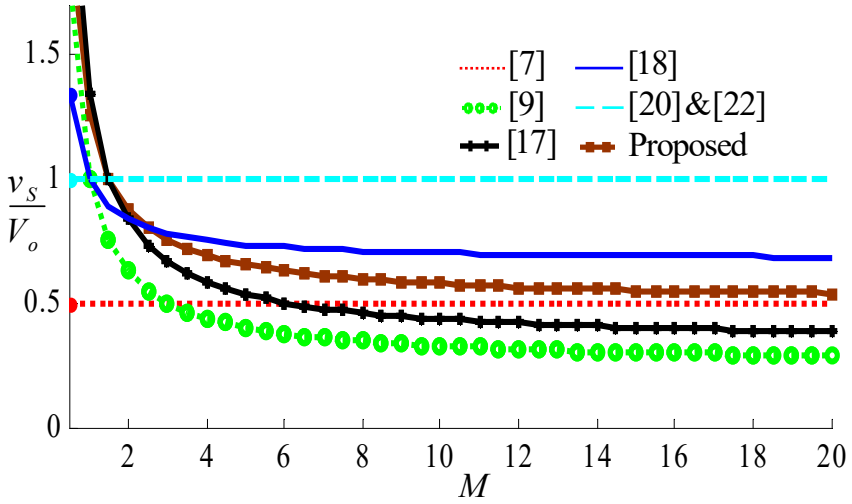
7. Comparison

In this section, the proposed converter is compared with other presented boost dc–dc converters in terms of number of switches, diodes, inductors and capacitors, maximum normalized voltage stresses on switches and diodes, ideal voltage gain, input current ripple and efficiency. The summary of this comparison is shown in Table 3. From the number of active components (switches and diodes), the proposed converter has more active components than [9,17,21,22]. On the other hand, the active components number of the proposed converter is less than [18] and is equal to [7,20]. Of course, the proposed converter has one more switch compared to [17,21]. In terms of passive components (inductors and capacitors), the proposed converter has fewer passive components compared to [9,17,18], and has more compared to [20,22], whereas, the passive components of the proposed converter are equal to [7,21]. Such as in [7,17,20,22], the proposed converter has low input current ripple, while [9,18] has a high current ripple problem. The maximum normalized voltage stresses curve of the switches and diodes are plotted in Figure 3a,b, respectively. As seen in Figure 3a, the maximum normalized voltage stresses of the switches and diodes for the proposed converter are less than [18,20,22], and are higher that [7,17]. Additionally, the maximum normalized voltage stress of the switches for the proposed converter is more than [9] while its maximum normalized voltage stress of the diodes is less than [9]. Comparison of the ideal voltage gain variations with [7,9,17,18,20–22] is shown in Figure 3c. As illustrated, the proposed converter provides more ideal voltage gain compared to other for $D < 0.5$ while the ideal voltage gain of [18] is higher than the proposed converter for $0.5 < D < 0.7$. For $D > 0.7$, the proposed converter ideal voltage gain value is more than [7,20–22] and is less than [9,17].

Table 3. Comparison between different converters.

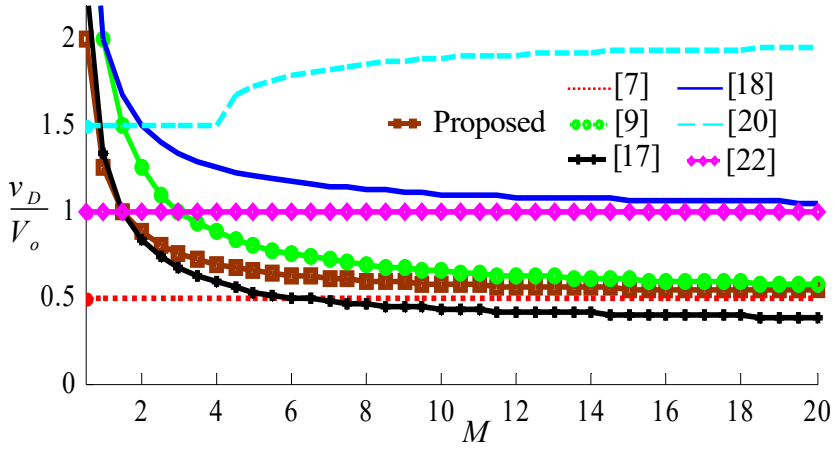
Element/Ref.		[7]	[9]	[17]	[18]	[20] (n = 1)	[21]	[22]	Proposed
Active component	switch	2	2	1	3	2	1	2	2
	diode	3	2	3	12	3	3	2	3
Passive component	inductor	2	3	4	6	2	2	2	2
	capacitor	3	3	6	1	2	3	2	3
Input ripple current		Low	High	Low	High	Low	Low	Low	Low
Max. voltage stress of switches		$\frac{1}{2}$	$\frac{3+M}{4M}$	$\frac{3+M}{3M}$	$\frac{1+2M}{3M}$	1	$\frac{1+M}{2}$	1	$\frac{3+2M}{4M}$
Max. voltage stress of diodes		$\frac{1}{2}$	$\frac{3+M}{2M}$	$\frac{3+M}{3M}$	$\frac{1+M}{M}$	$\frac{\frac{3}{2}+\sqrt{\frac{1}{4}-\frac{1}{M}}}{}$	$\frac{1+M}{2}$	1	$\frac{3+2M}{4M}$
Voltage gain in CCM (M)		$\frac{2}{1-D}$	$\frac{1+3D}{1-D}$	$\frac{3D}{1-D}$	$\frac{1+5D}{1-D}$	$\frac{1}{D(1-D)}$	$\frac{1+D}{1-D}$	$\frac{1}{D(1-D)}$	$\frac{1+D}{D(1-D)}$
Voltage gain variation ($D: 0 \rightarrow 0.9$)		$2 \rightarrow 20$	$1 \rightarrow 37$	$0 \rightarrow 27$	$1 \rightarrow 55$	$- \rightarrow 11$	$- \rightarrow 19$	$- \rightarrow 11$	$- \rightarrow 21$

The efficiency changes of the proposed converter for different output power are shown in Figure 3d. As shown, the proposed converter has a higher calculated efficiency than [21,22] and its value is less than [20] for lower output power. Increasing output power, the calculated efficiency of the proposed converter reaches to efficiency value in [20,21] while its value gets much better than [22].



(**a**)

Figure 3. *Cont.*



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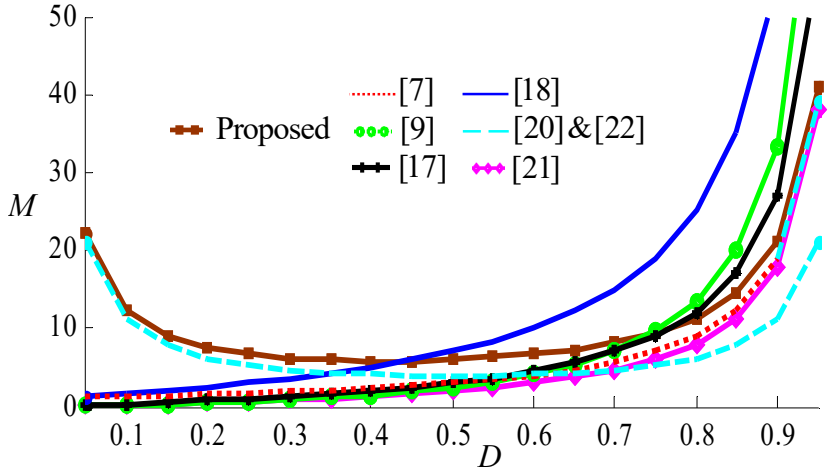

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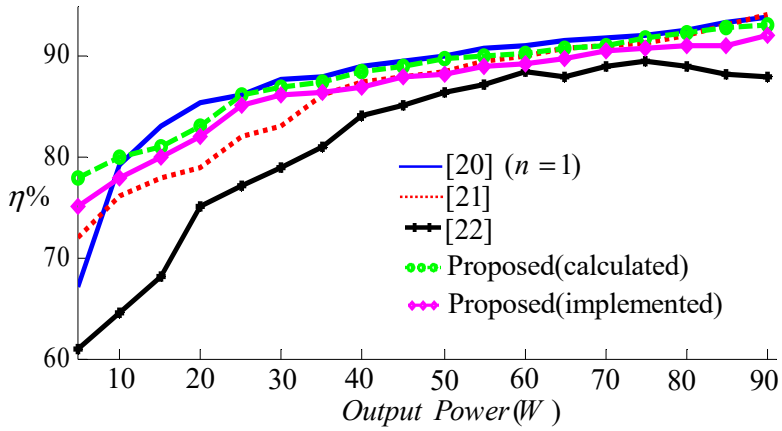


(**d**)

Figure 3. Compression between different converters: (**a**) maximum normalized voltage stress on switches, (**b**) maximum normalized voltage stress on diodes, (**c**) ideal voltage gain variation in versus duty ratios, (**d**) efficiency variations.

8. Experimental Results

The experimental results by laboratory prototype are used to evaluate the theoretical concepts and relations. The details of experimental laboratory prototype are presented in Table 4. It should be noted that the values of $C_1 = C_2$ and C_3 are selected from the common values in the market, taking into account Table 2 and $\%x_{C1} = \%x_{C2} = \%5$ and $\%x_{C3} = \%1$. Meanwhile, the core material of the inductors is selected the same in each operating mode. Except for the critical mode and regarding section III, the inductors are designed for free current ripple conditions. In Table 4, K is the eddy current loss coefficient, β_{ac} is the magnetic flux variation, m and n are constant and depend on the core type and W_{tfe} is core weight in grams. Powder core has been selected for all of the inductors. Additionally, r_{DS-on}, t_r, t_f, t_{rr}, t_c, C_{OSS}, Q_{rr} and di/dt are static drain-source on resistance, rise time, fall time, reverse recovery time, cross-over time, output capacitance, reverse recovery charge and peak diode recovery current slope, respectively.

Table 4. Experimental parameters.

Parameters	CCM	DCM
L_1 (Powder core)	$L_1 = 3$ mH; $r_{L1} = 0.17\ \Omega$; $K = 0.00551$; $\alpha = 1.23$; $\beta = 2.12$; $W_{tfe} = 44.6$; $B_{ac} = 0.0527$	$L_1 = 35$ µH; $r_{L1} = 0.002\ \Omega$; $K = 0.00551$; $\alpha = 1.23$; $\beta = 2.12$; $W_{tfe} = 44.6$; $B_{ac} = 0.0527$
L_2 (Powder core)	$L_2 = 1.5$ mH; $r_{L2} = 0.11\ \Omega$; $K = 0.00551$; $\alpha = 1.23$; $\beta = 2.12$; $W_{tfe} = 39.1$; $B_{ac} = 0.0545$	$L_2 = 250$ µH; $r_{L2} = 0.004\ \Omega$; $K = 0.00551$; $\alpha = 1.23$; $\beta = 2.12$; $W_{tfe} = 39.1$; $B_{ac} = 0.0545$
$C_1 = C_2$ & C_3	110 µF; $r_{C1} = 0.02\ \Omega$ & 63 µF; $r_{C3} = 0.015\ \Omega$	
Diodes	Type: MUR1560; $V_{F,D} = 0.8$ V; $r_D = 0.01\ \Omega$	
N-channel MOSFET	Type: STW45NM50F; $r_{DS-on} = 0.07\ \Omega$; $t_r = 11$ nS; $t_f = 25$ nS; $t_{rr} = 245$ nS; $t_c = 44$ nS; $C_{OSS} = 1260$ pF; $Q_{rr} = 1600$ nC; $di/dt = 100$ A/µS	
V_i,f,D,D,R	12 V, 10 kHz, 50%, 50%, 100 Ω	
Output Power	51.8 W	89.3 W

8.1. Experimental Results for Critical Mode

Considering (20) and (22) and Table 4, the values of $L_{C1} = 69.4$ µH and $L_{C2} = 416.6$ µH are obtained. Considering $L_1 = L_{C1}$ and $L_2 = L_{C2}$, the proposed converter would be in critical mode. Figure 4a,b show the waveforms of current though the inductors L_1 and L_2 in critical mode, respectively. If $L_1 < L_{C1}$ and $L_2 < L_{C2}$ then the proposed converter would operates in DCM and the proposed converter operates in CCM for $L_1 > L_{C1}$ and $L_2 > L_{C2}$ values. Substituting into Table 2 yields $i_{SP1,\max}^{CCM} = 8.15$ A and $i_{SP2,\max}^{CCM} = 4$ A which the results are verified by Figure 4c,d.

8.2. Experimental Results for CCM

Considering parameters in Table 4, the proposed converter operates in CCM. Some experimental results of the voltage and current of elements are presented in Figure 5. As shown in Figure 5a, the inductor L_1 voltage equals 12 V at T_{on} (Equation (1)) and it is equal to -14 V at T_{off} (Equation (2)). As shown, the voltage of inductor L_2 is equal to 24 V and -24 V at T_{on} and T_{off}, respectively, which confirmed (4) and (5). Substituting the parameters of Table 4 into (3), (6) and (8), yields $v_{C1} = 24$ V, $v_{C2} = 24$ V and $v_{C3} = 72$ V. The calculated values for the capacitors voltage are confirmed by experimental results. As shown in Figure 5e,f, the current variations of the switches S_1 and S_2 are in accordance with Table 2. As illustrated, the PCFS of the switches S_1 and S_2 are equal to $i_{SP1}^{CCM} = 4.5$ A and $i_{SP2}^{CCM} = 3$ A, respectively (Equations (23) and (25)).

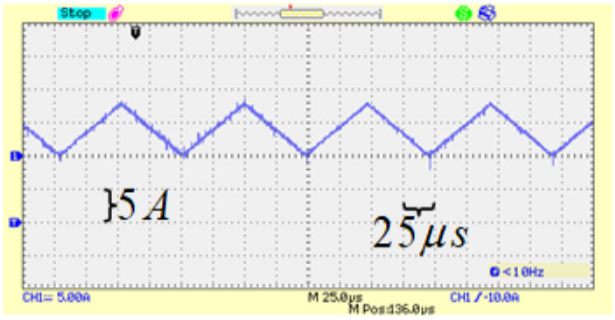
Considering the presented parameters in Table 4 into (29) and (47), and from the third term of the diodes losses relations and fifth and sixth terms of switch losses relations yields $P_{L1} = 2.033$ W, $P_{L2} = 0.4352$ W, $P_{C1} = P_{C2} = 0.0512$ W, $P_{C3} = 0.0073$ W, $P_{D1} = 0.1849$ W, $P_{D2} = P_{D3} = 0.0256$ W, $P_{S1} = 0.12943$ W and $P_{S2} = 0.7168$ W. Thus, the calculated efficiency is 91.4%, whereas the implemented efficiency is 90.6%. The calculated and implemented efficiencies for different loads are shown in Figure 3d. As shown, the calculated efficiency of the proposed converter is increased for higher loads and its maximum value are obtained 96.1%.

8.3. Experimental Results for DCM

Considering presented parameters in Table 4, the proposed converter operates in DCM. Some experimental results in this operating mode are shown in Figure 6. According to Figure 6a, the voltage variations of inductor in one period of time are in accordance with (9), (10) and (11) so that $v_{L1,2} = 12$ V, $v_{L1,3} = -16$ V and $v_{L1,4} = 0$. Additionally, the relations (13) to (15) are evaluated by experimental results in Figure 6a. As it can be seen, $v_{L2,1} = -42$ V, $v_{L2,2} = 0$ and $v_{L2,4} = 30$ V. In addition, $v_{C1} = 27$ V, $v_{C2} = 27$ V and $v_{C3} = 94.5$ V that verifies (12), (16) and (18), respectively. Furthermore, it is obtained $i_{SP1}^{DCM} = 18$ A and $i_{SP2}^{DCM} = 7.1$ A (see Figure 6e,f) which verifies the accuracy of Table 2. Table 5 shows the summery of experimental results of some parameters under CCM, critical mode and DCM.

Table 5. Summary of experimental results for different operating modes.

Parameters	CCM	Critical Mode	DCM
$i_{SP1,\max}$	4.5 A	8.15 A	18 A
$i_{SP2,\max}$	3 A	4 A	7.1 A
$i_{L1,\max}$	-	8 A	-
$i_{L2,\max}$	-	3 A	-
v_{C1}	24	-	27
v_{C2}	24	-	27
v_{C3}	72	-	94



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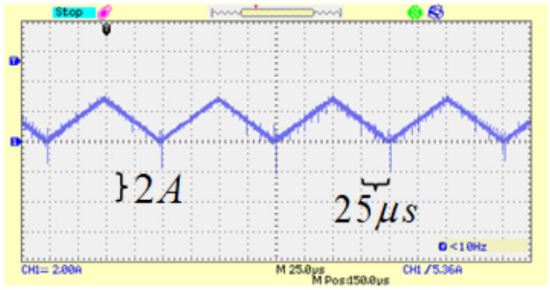

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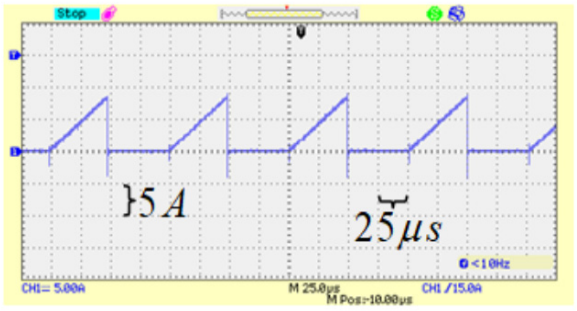

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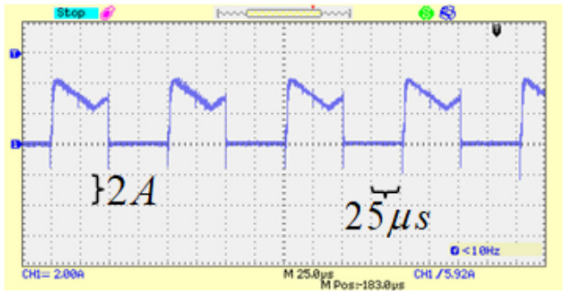
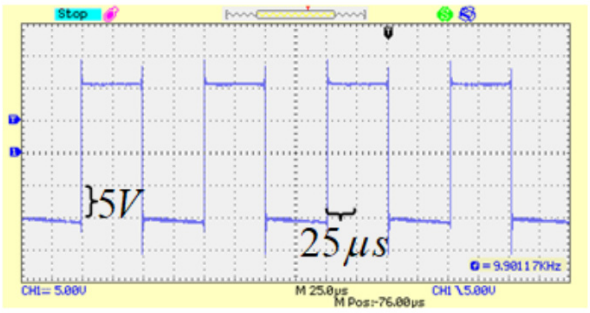


(**d**)

Figure 4. The current waveforms in a critical mode for; (**a**) L_1 current, (**b**) L_2 current; (**c**) S_1 current, (**d**) S_2 current.



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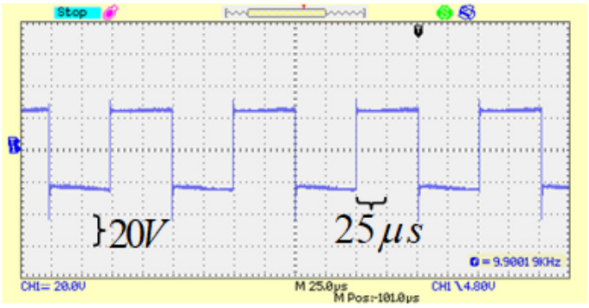

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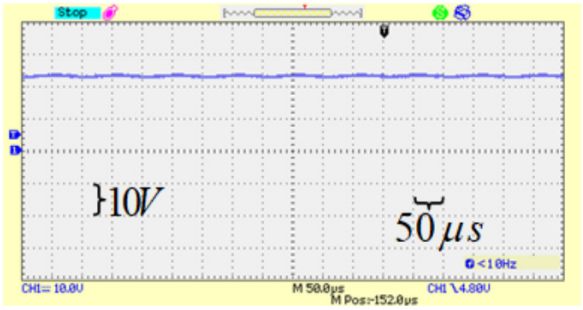

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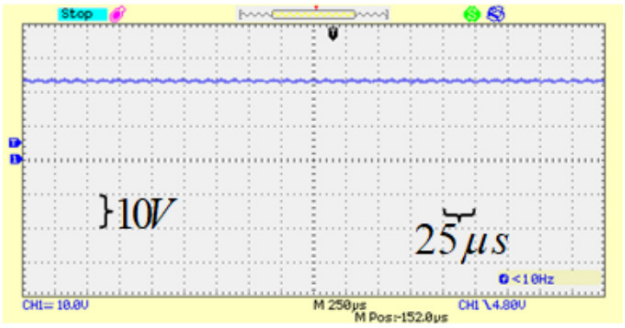

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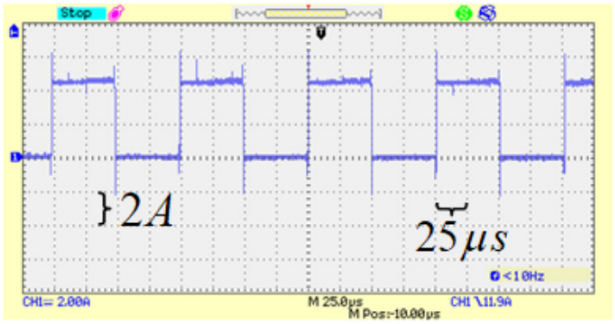

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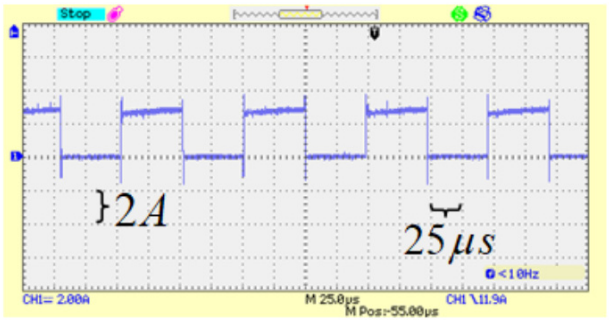
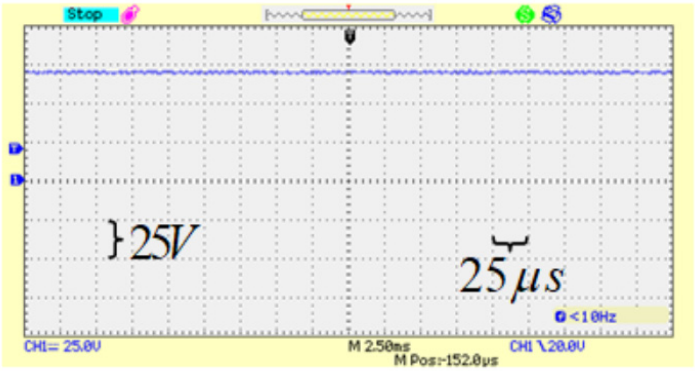
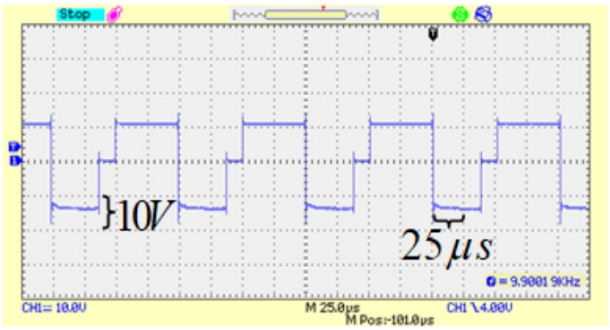


(**f**)



(**g**)

Figure 5. Experimental results in CCM: (**a**) L_1 voltage; (**b**) L_2 voltage; (**c**) C_1 voltage; (**d**) C_2 voltage; (**e**) S_1 current; (**f**) S_2 current; (**g**) C_3 voltage.



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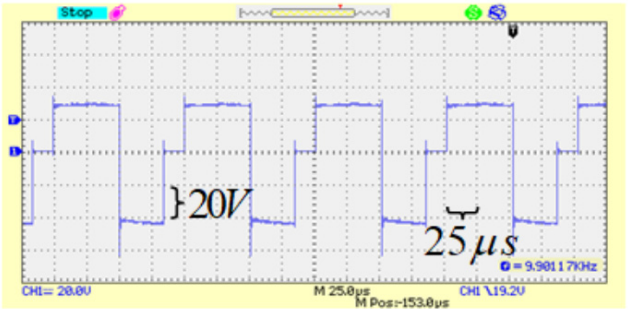

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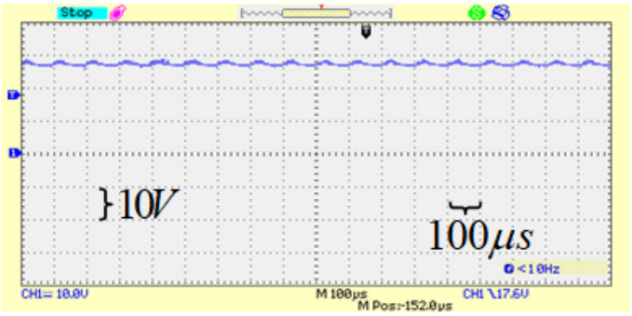

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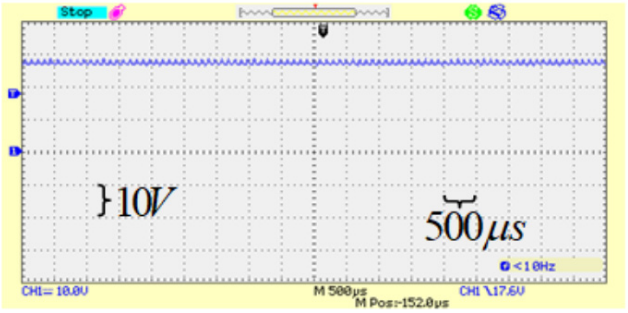

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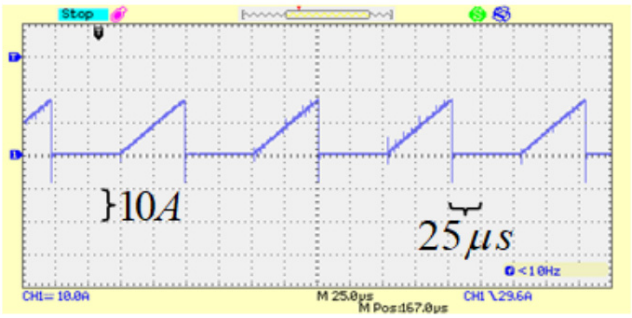

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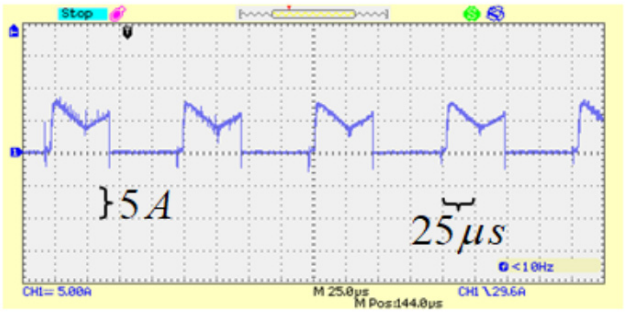

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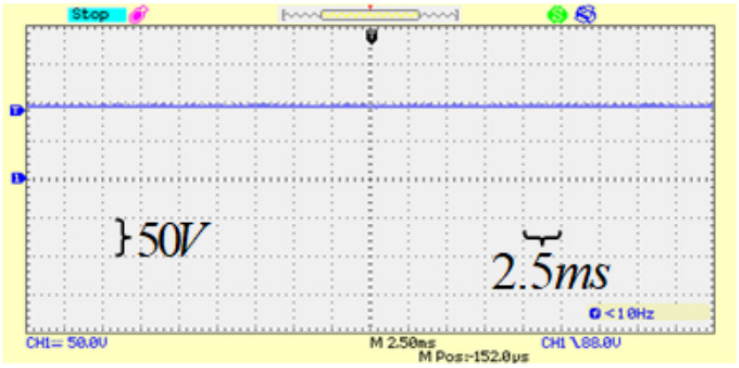

(**g**)

Figure 6. Experimental results in DCM: (**a**) L_1 voltage; (**b**) L_2 voltage; (**c**) C_1 voltage; (**d**) C_2 voltage; (**e**) S_1 current; (**f**) S_2 current; (**g**) C_3 voltage.

9. Conclusions

This paper proposed a new transformer-less structure for a boost dc–dc converter with free and low input current ripple, high voltage gain capability by using an input source, lower output capacitance and suitable voltage stress on semiconductors. This new structure was proposed using the VL technique. For the proposed converter, the voltage and current relations of components were extracted in CCM and DCM in order to design purpose and the output voltage gain was calculated in each operating mode. Additionally, the critical inductance calculations of the proposed converter were presented to operate in critical mode. Moreover, current stress of switches, calculation of passive components values and efficiency are analyzed. Additionally, the proposed converter performance was compared with some other presented converters in terms of the ideal voltage gain in CCM, the number passive and active components, voltage stress on semiconductors, input current conditions and efficiency. As shown, the proposed converter has lower and suitable voltage stress on its semiconductors compared with some presented structures. Additionally, the ideal voltage gain of the proposed converter in CCM was higher than some others in more duty cycles. On the other hand, the proposed converter calculated and implemented maximum efficiencies were increased for higher loads to 96.1% and 94.8%, respectively. Of course, a drawback of the proposed converter is the use of two power electronics switches. However, the output voltage gain increased very well. The output voltage for $D = D' = 50\%$, $V_i = 12$ V and $f = 10$ kHz in CCM and DCM are 72 V and 94.5 V, respectively. The current of switches are obtained as $i_{SP1}^{CCM} = 4.5$ A, $i_{SP2}^{CCM} = 3$ A, $i_{SP1,\max}^{CCM} = 8.15$ A, $i_{SP2,\max}^{CCM} = 4$ A, $i_{SP1}^{DCM} = 18$ A and $i_{SP2}^{DCM} = 7.1$ A. Finally, the performance of the proposed converter has been reaffirmed with mathematical and experimental results.

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