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A Simple Strategy to Reduce the NDZ Caused by the Parallel Operation of DER-Inverters

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Abstract: In this work the harmonic injection active anti-islanding technique that has been recently proposed in reference Voglitsis et al. (2018) published in *Trans. Power Electron.* is generalized under the prospect of a high penetration level of distributed energy resource (DER) installations. Towards this direction, the theoretical limitation for the penetration level of such schemes is investigated and a firm theoretical background is presented that takes into account the installation parameters, as well as the penetration level at the installation common coupling point. Furthermore, a substantial feature which indicates the upgrade-ability of each installation is studied. Finally, extensive simulations and experiments verify the theoretical analysis.

Keywords: islanding; DER-inverters; NDZ; parallel inverters

1. Introduction

The global cumulative capacity of distributed energy resources (DERs) has grown at almost an exponential rate over the past decade, pushed by strong feed-in policies and declining DER prices [1]. Nowadays, worldwide expectations for renewable energy sources are still increasing, with PVs and wind parks being the predominant representatives of the DERs energy market share. Regarding PV-technology, the majority of PV installations consists of low power residential applications that are connected into the low voltage grid network. An indicative example is the renewable energy market share of Germany, where 70% of installed PVs are connected to the low voltage grid [1].

Until recently, for these installations, the guidelines concerning the integration of PVs were relatively modest, including only few basic demands for the PV installation, requiring the THDi of the inverter output injected current to be less than 5%, while the DPF needed to be close to unity. Therefore, the common (and cost effective) practice concerning the control of these systems has involved two main tasks: to track the maximum power from the PV-panel (by applying an MPPT control); and to inject a current waveform with a low THDi and unity DPF (e.g., by synchronizing with the utility voltage through a PLL). On the other hand, the power production of these installations typically varies between 0.1 and 10 kW, being characterized by low PL levels thus far. However, the continually rising share of renewable energy sources is currently pushing towards innovative solutions that will allow higher levels of renewable sources to be integrated into the low (and medium) voltage networks. A sign of this direction comes from the new IEEE 1547-2018 standard, which states that new DERs should be, among other capabilities, able to provide ancillary services into the grid.

Another major issue associated with interconnected DERs towards the upcoming PL growth is the facilitation of unintentional islanding detection. Undoubtedly, protection against this undesirable

condition is of significant importance for the proper operation, safety, and reliability of the electrical system. Several recommendations and directives have been published on this subject aiming to protect maintenance personnel and the electric equipment of interconnected DERs. For example, the California Electric Public Utilities Commission (CPUC) Rule 21 describes the interconnecting, operating, and metering requirements for new generation facilities emphasizing, among other things, the importance of robust anti-islanding protection features. Furthermore, the foremost standardization institutions require a disconnection ability from the utility grid within a timeframe of 2 s., such as the IEEE Std. 1547, IEC Std. 62116, UL Std. 1741, and the former IEEE Std. 929-2000.

Until recently, passive anti-islanding protection schemes (i.e., by means of under/over voltage/frequency) were the common practice for small scale DERs (like residential PVs). However, in the anticipation of their power increase and high penetration level, those schemes are expected to end up suffering from large NDZs. Therefore, more sophisticated communication or active based anti-islanding techniques are required to meet the above mentioned standards.

An active based anti-islanding scheme which is dedicated for implementation under high penetration levels of DERs, has been proposed in reference [2]. According to that scheme, anti-islanding detection can be based on the injection of the 2nd harmonic current component, achieving both low NDZ and low FDZ and without affecting the power quality at the PCC. While the abovementioned work considers the high penetration levels of DERs, the rather significant cancelling effect that comes from the operation of multiple grid-tied inverters that inject the same order harmonic current was not be taken into consideration. This effect was thoroughly analyzed in the current work and it is consistent with any harmonic injection base scheme that is described by the following formula and the structure shown in Figure 1:

$$H_{i,h} = \hat{I}_{i,h} \cdot Z_{i,h} \cdot e_{i,h} = \hat{V}_{PCC,i,h} \cdot e_{i,h}. \quad (1)$$

The equation above describes anti-islanding techniques that periodically inject a low current harmonic component, and estimate the grid condition at PCC (grid-tied or islanded) based on the evaluation parameter, H_h, and a predefined threshold value (H_{thr}). Normally H_h is based on Equation (1), while typically the condition $H_h > H_{thr}$ indicates the islanded-operation of the installation. Grid response is usually evaluated through a DFT algorithm, as in references [2–4], by other means such as through cross-correlation, as in references [2,5,6], or through a Goertzel algorithm, as in reference [7]. A comprehensive comparative review on the above methods can be found in reference [8]. Various *PL* values have been used, while the effect of the anti-islanding schemes on the quality of the delivered power has also been studied. However, in reference [8], the *PL* level values were achieved by adjusting the power of a single grid-tied inverter along with the internal impedance of the grid transformer. As such, the concept of multiple inverters was not achieved in that work.

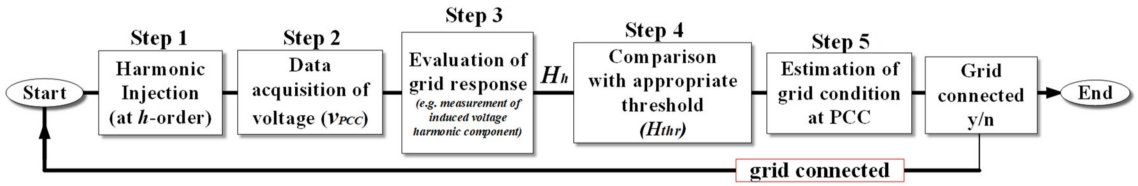


Figure 1. Generic description of the harmonic injection based anti-islanding techniques.

In the current work, the anti-islanding protection technique that has been proposed in reference [2] is modified, in order to take into account the effect of parallel operation of multiple DER-inverters that are connected to the same node. This problem has been also stated in reference [9], where a solution based on an external accumulator was proposed. In this work, a different solution is proposed that prolongs the harmonic injection in order to achieve a required overlap among the injected harmonic components of inverters. The modified technique that is proposed in this work is very simple and does not require an external accumulator, which are the main reasons not to use the technique discussed in reference [9]. On the other hand, the proposed modified technique has some limitations (particularly

for a large number of inverters), because of the harmonic regulations of grid-tied inverters. Those limitations are discussed in more detail in Section 3.4. The effectiveness of the proposed technique is verified through extensive simulations as well as experimental results, which are presented in Sections 4 and 5, respectively. Finally, Section 6 concludes the paper.

2. Description of System Under Study

The general description of the system under study is illustrated in Figure 2. PV-generators have been considered in this scheme, which are the predominant DER for low-voltage networks nowadays [2]. The power flow of each subsystem is also illustrated in Figure 2. It is noted that according to the new version of IEEE 1547-2018 [10], DER-generators should provide ancillary services to the grid and be capable of reactive power flow operation [1,11,12]. Finally, Figure 3 depicts the equivalent electrical diagram of a typical PV grid-tied CSI [13,14], which is an attractive configuration for low-power (typically below 500 W) PV-microinverters [3]. The topology consists of two stages. The inverter stage of the topology operates in line frequency with a very simple control and very low switching losses. On the other hand, the dc-dc converter stage operates in a high switching frequency driven by a maximum power point tracking (MPPT) algorithm. The utility grid and an RLC load (local-load) are also illustrated in Figure 3, forming the recommended circuit based on the IEEE 929-2000 [15] and IEEE 1547.1-2005 [16] for assessing the anti-islanding features of grid-tied inverters. The resistance R_g and inductance L_g (also shown in Figure 3), represent the power-line and power-transformer equivalent impedance.

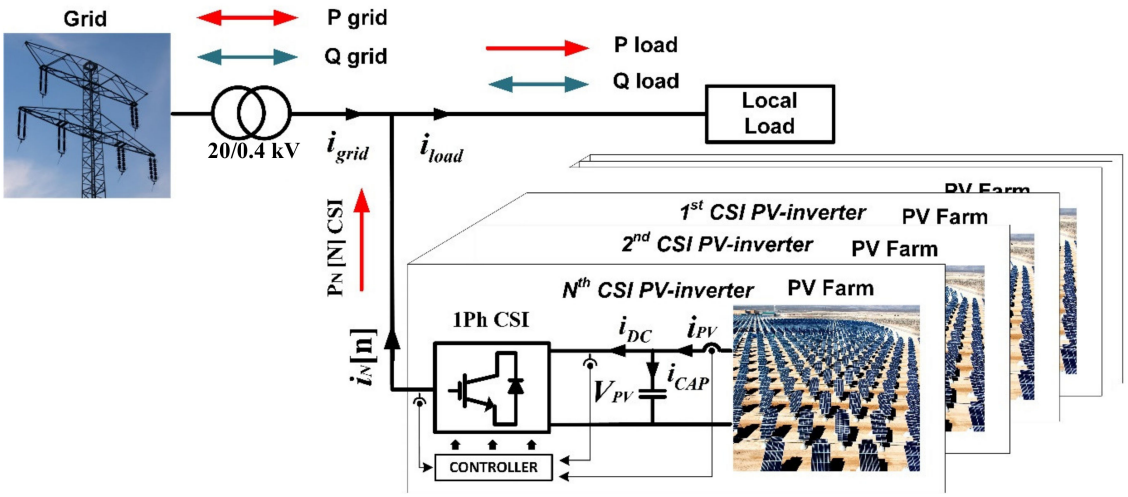


Figure 2. Schematic diagram of the system under study, where PV-distributed energy resources (DER) generators have been used.

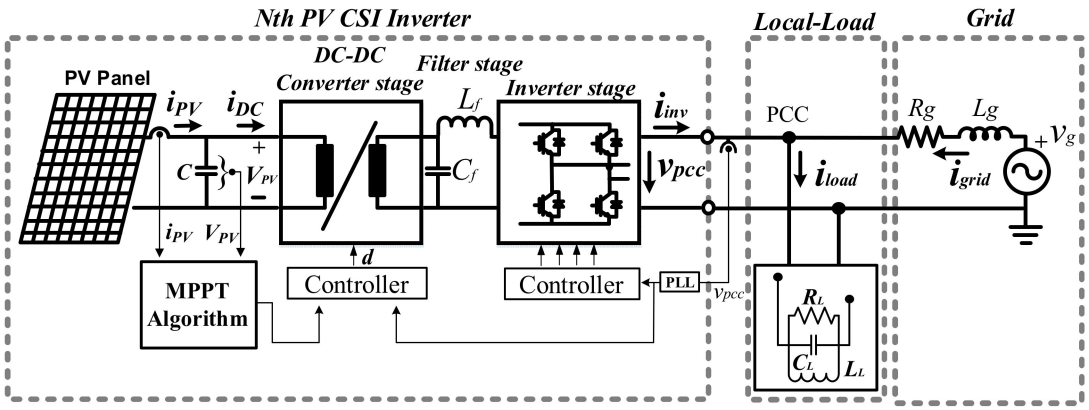


Figure 3. Electrical diagram of a PV-based DER-CSI.

3. Proposed Modification and Description of the Anti-Islanding Technique in reference [2]

3.1. Description of the Anti-Islanding Technique That Has Been Proposed in reference [2]

The anti-islanding technique that has been proposed in reference [2] is a harmonic-injection-based technique which is based on the cross-correlation algorithm to generate the evaluation index in Equation (1). It injects a harmonic current component with twice the base frequency aiming to distort the PCC voltage, which correlates with a reference signal (that also has twice the base frequency). The correlated value is compared against a threshold value to identify a potential islanding condition. The correlated signal is periodically stored through the sample and hold subsystem of Figure 4, and is compared against CC_{thr} every T_{Std} seconds. An islanding condition is detected only when the correlated value surpasses CC_{thr} REP consecutive times (typically REP = 2), adding a countermeasure against false tripping of the inverter. Finally, when an islanding condition is identified, the inverter operation is ceased and locked-in, through the D flip-flop and zero-hold circuit of Figure 4.

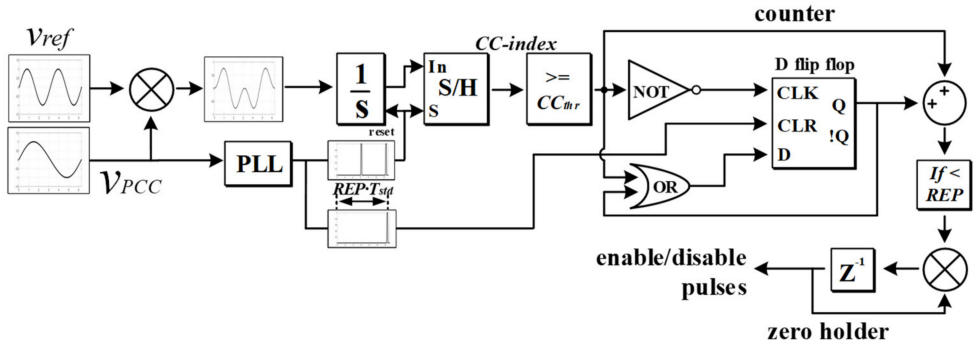


Figure 4. The anti-islanding technique that has been proposed in reference [2].

3.2. Description of the Issue That Arises by the Parallel Operation of Multiple Grid-Tied Inverters

Regarding the harmonic injection-based techniques, the induced harmonic voltage component that is induced by each inverter is compromised, as synchronous injection (injection at same time-intervals) among the inverters cannot be reassured. As such, the anti-islanding detection is jeopardized, risking being unable to detect an islanding incident. To better explain this problem, we will use some key equations coming from the operation of a single inverter. We will start by uing the active power of a single inverter, operating in a load-matching condition (keep in mind that in (2) P_{tot} is referring to the total power of a single-inverter):

$$P_{tot} = \hat{V}_{PCC,1}{}^2 \Big/ (2R_L) \, . \tag{2}$$

Based on the anti-islanding technique used in reference [2], the induced harmonic component of the PCC voltage, which is provoked by a single inverter under load-matching conditions is given by ("i" was assigned for the islanded or grid mode of operation):

$$\hat{V}_{PCC,i,h} = \hat{V}_{PCC} \cdot K \cdot Gain_i \cdot \zeta_{i,h} \, . \tag{3}$$

The CC_{index} in the islanded and in the grid-tied operation can be approximated (assuming a relatively large S-value) by [2]:

$$CC_i = \frac{\hat{V}_{ref} \hat{V}_{PCC,i,h}}{2} S \cdot T_{CC} \cdot \cos(\Delta\varphi_{CC,i}). \tag{4}$$

Please note that T_{CC} should be an integer multiple of T_b, otherwise the calculated CC_{index} will deviate from the theoretical value in Equation (4). When considering Equation (4), a threshold can be set—as in reference [2]—that is based on the load-matching condition of a single inverter:

$$CC_{thr} = CC_{grid\max} + \left(CC_{isl\min} - CC_{grid\max}\right) \cdot W\%. \tag{5}$$

Now let us assume that N current-source inverters (of P_N $[n]$ nominal power each) that utilize the anti-islanding technique in reference [2], as well as M other DER-inverters (that may or may not utilize the anti-islanding technique) of a total nominal power P_{Mtot} that might be potentially installed are connected to the same PCC, and that $P_{tot} = P_{Mtot} + P_{Ntot}$. According to the analysis that is conducted in reference [9], the magnitude of the induced voltage that is caused by each inverter of the N-subgroup can be expressed by the following equation:

$$\hat{V}_{PCC,i,h}[n] = \hat{V}_{PCC} \cdot K[n] \cdot Gain_i[n] \cdot \zeta_{i,h} \cdot P_N[n]/P_{tot}, \tag{6a}$$

whereas the induced harmonic voltage that is generated by the synchronous (simultaneously) harmonic injection of l-inverters (assuming that the N-subgroup consists of inverters of the same type) is given by [9]:

$$\sum_{n=1}^{l} \hat{V}_{PCC,i,h}[n] = \hat{V}_{PCC} \cdot K[n] \cdot Gain_i[n] \cdot \zeta_{i,h} \cdot \sum_{n=1}^{l} P_N[n] \Big/ P_{tot}. \tag{6b}$$

Therefore, the CC_{index} that is calculated by (3) for a single inverter of nominal power P_{tot}, is reduced by a factor of $\sum_{n=1}^{l} P_N[n]/P_{tot}$ when multiple inverters are connected to the same PCC under the load-matching condition. Evidently, the initial selection of CC_{thr}, which has been made considering only a single grid-tied inverter, might fail to detect the islanding operation under multiple inverters, as the CC_{index} might fall below the initial CC_{thr} -value during the islanded operation. Therefore, only a limited power upgrade (P_{Mtot}) is permitted for each installation, the value of which can be calculated by the following expression (assuming identical *Gain* and K values for each inverter) [9]:

$$P_{Mtot} < \sum_{n=1}^{l} P_N[n] \cdot \left(\frac{CC_{isl\min}}{CC_{thr}} - 1\right) - \sum_{n=l+1}^{N-l+1} P_N[n]\,. \tag{7}$$

According to reference [9], the upgrade factor of a given installation can be given by the following equation:

$$UF = \frac{P_{Mtot}}{P_{Ntot}}. \tag{8}$$

Evidently, *UF* provides an important feature of DER-installations that should be taken into account for the evaluation of the harmonic-based anti-islanding techniques (this factor will be even more significant in the near future when the penetration level of DERs is expected to be significantly increased). Using Equation (7) and Equation (8), we can either improve *UF* by increasing the number of overlapped inverters or by adjusting the CC_{islmin}/CC_{thr} ratio. It should be noted though that if the installation operates at a power lever lower than the nominal one (e.g., during a cloudy day at a PV-based DER installation), then the *UF* will be lower than the value that has been calculated by Equation (8). It should be noted that in Equation (8), we used the nominal power of inverters. In order to overcome this problem, we used a droop-controller for the magnitude of the harmonic injection, similar to the one used in reference [9]:

$$K*[n] = K[n]\frac{P_N[n]}{P_N*[n]}. \tag{9}$$

3.3. Description of the Proposed Modified Anti-Islanding Scheme for N Grid-Tied Inverters

In this work, we proposed to prolong the T_{CC} interval of each inverter in order to maintain a minimum overlapped harmonic injection between the inverters that represent the *N*-subgroup. This strategy has the advantage of being effortlessly implemented in the control scheme of each inverter, without requiring communications. The equation that defines the minimum injection duration (T_{CC}) of *N*-inverters such that at least *l*-inverters out of *N* perform an injection simultaneously, is:

$$N \cdot T_{CC} > T_{Std} \cdot (l - 1). \tag{10}$$

It was noted that T_{Std} should be the same among the *N*-inverters. Moreover, a beforehand synchronization agreement is required among the inverters (as in reference [9]), in order to avoid the harmonic cancellation effect. A synchronization agreement could entail that all inverters always inject harmonic current at the beginning of the positive/or negative grid voltage wave. This synchronization agreement can be made in advance and therefore it is not classified as a communication requirement.

The proposed strategy is demonstrated in Figures 5 and 6, where a set of *N*-subgroup inverters is considered. The CC_{index} is as well depicted in those figures, where 1 pu denotes the normalized CC_{index} that is generated by the overall of four inverters. Based on the presented results, the number, *l*, of inverters that overlap with each other, depends on the duration of their individual harmonic injection, denoted as T_{CC}. It should be noted that T_{CC} should be also the same among the inverters. For example, $l = 3$ implies that the harmonic injection of at least three inverters will overlap (see Figure 6a) with each other. It was noted that the proposed strategy indicates the minimum amount of overlapped inverters, even though there is a probability for more inverters to overlap as well.

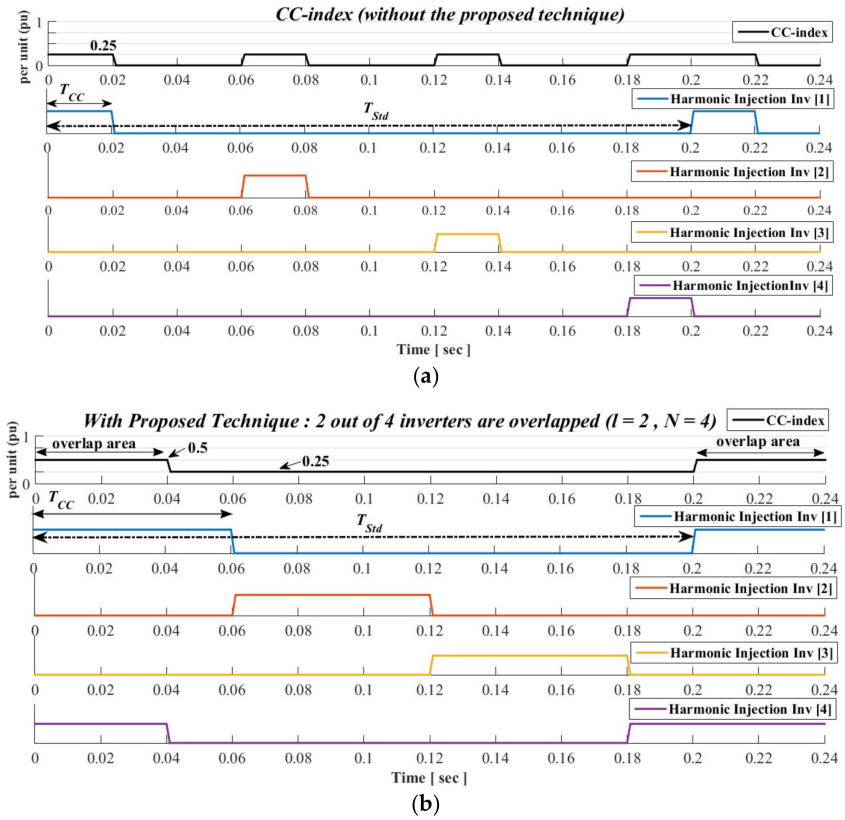


Figure 5. Injection pattern of the N-subgroup inverters and CC_{index} evolution in a time domain for, (**a**) $N = 4$ and $l = 1$, (**b**) $N = 4$ and $l = 2$ (implying that at least two inverters will be overlapped).

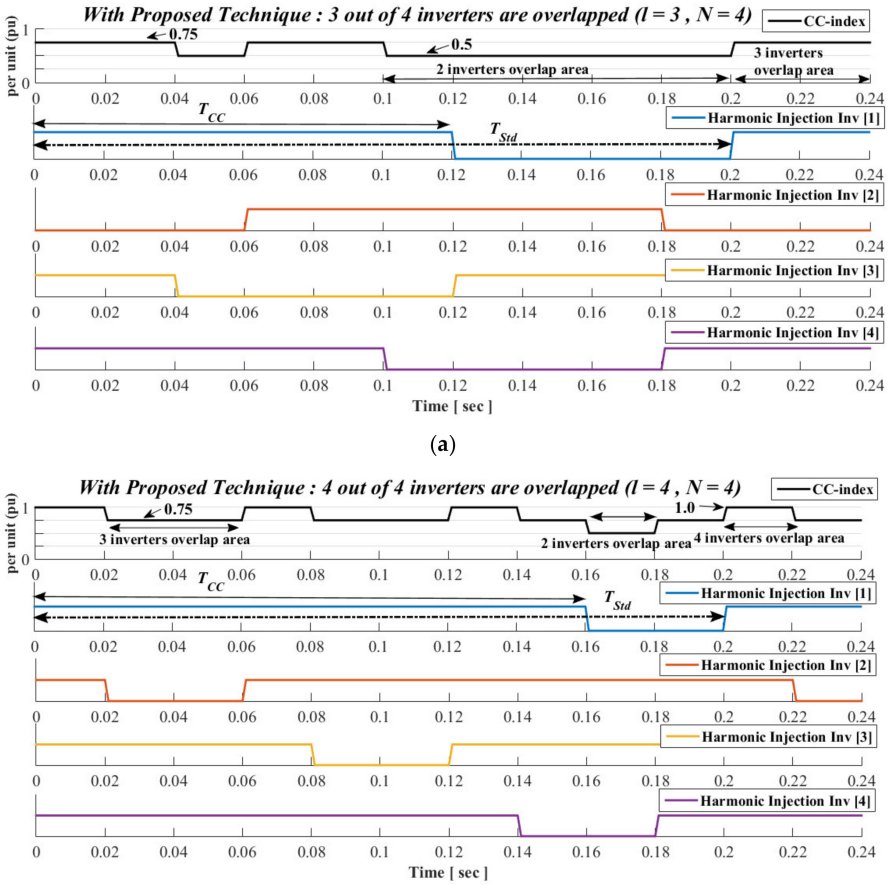


Figure 6. Injection pattern of the N-subgroup inverters and CC_{index} evolution in a time domain for, (**a**) $N = 4$ and $l = 3$ (implying that at least three inverters will be overlapped), (**b**) $N = 4$ and $l = 4$ (implying that at least four inverters will be overlapped).

3.4. Discussion on the Limitations of the Proposed Modification

According to the power quality limitations [16], the mean magnitude of the 2nd–order current harmonic component captured in 10 cycles (i.e., 0.2 s for 50 Hz systems) under rated power conditions has to be less than 1%, implying that:

$$Gain_{grid}[n] \cdot K[n] \cdot T_{CC}/0.2 \leq 1\%. \quad (11)$$

Combining Equations (9)–(11), the following equation was derived (assuming that $0.2 \geq T_{Std}$):

$$K[n] \cdot Gain_{grid}[n] \leq \frac{N}{l-1} 1\%. \quad (12)$$

According to Equation (12), higher l-values impose stricter limitations in the $K{\cdot}Gain$ product. This restriction is dictated by the power quality standards and it is associated with the upper limit of K. The $K{\cdot}Gain$ limitation is plotted in Figure 7, as a function of l, for five indicative N-values (i.e., $N = 4$, 6, 8, 10, 12). According to Figure 7, larger N-values enable the harmonic injection of the inverters to be overlapped with a lower limitation. For example, the limitation of $K{\cdot}Gain$ when two inverters are overlapped is 0.1 when the total number of inverters is 12, whereas it becomes 0.05 (much stricter) when less inverters are available. This happens because the same number of inverters can be overlapped with shorter injection durations when a larger total number of inverters is available. On the other hand, for the same l/N ratio, the $K{\cdot}Gain$ limitation gets stricter for higher N-values. Another notable factor

that can be seen in Figure 7 is the round-down of the *K·Gain* values. The round-down is caused by the obligation of T_{CC} being an integer multiple of T_b. Thus, various *l, N* combinations might lead to the same *K·Gain* limitation. For example, note that for *l* = 10 & N = 10, and for *l* = 12 & N = 12, the same limitation of 0.01 stands.

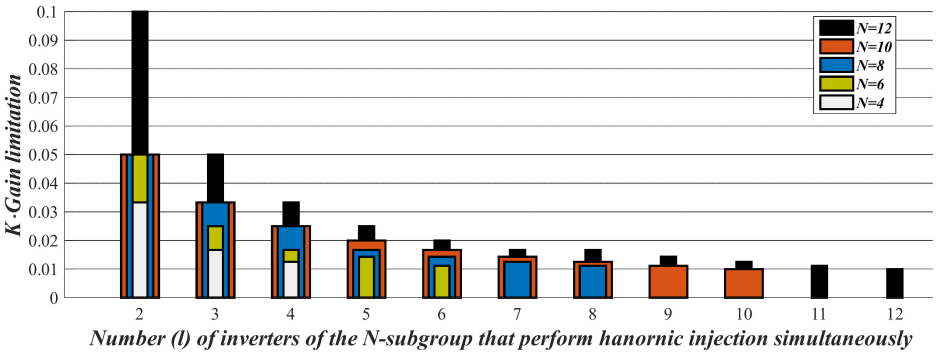


Figure 7. *K·Gain* limitation as a function of *l*, for five indicative *N*-values (i.e., *N* = 4, 6, 8, 10, 12).

On the other hand, the restriction associated with the bottom limit of *K*-value is dictated by the inverter microcontroller. For example, in reference [3] a 16-bit DSPIC30F4011 achieves a 4-bit accuracy over the generation of the harmonic signal with *K* = 4% and *Gain* = 2, whereas for *K* = 0.5%, its accuracy is limited to 1 bit. Therefore, choosing the *K*-value involves a compromise between the desired accuracy of the produced signal, the maximization of *UF* parameter, and the microcontroller cost.

Finally, it should be noted that the obligations of Equation (12) only concern the operation of the inverter under its rated power. Therefore, we do not have to take into account the further limitation that comes from the higher values of *K* * [*n*], forced by the proposed droop-controller of Section 3.2 when the inverter operates with a lower power.

4. Simulation Results

Two main case studies are examined in this Section to demonstrate the effectiveness of the proposed anti-islanding technique. For this reason, a DER-installation that consists of five grid-tied inverters has been simulated in a Matlab/Simulink environment. Specifically, the DER-installation under study comprises four current-controlled VSIs that utilize the proposed anti-islanding scheme (*N* = 4) and one current-controlled VSI that utilizes a passive under/over voltage/frequency (U/O-V&F) anti-islanding scheme (*M* = 1). The inverters rating as well as rest of the system parameters are presented in Table 1, while all case-studies have been simulated considering the load-matching condition, in accordance with the IEEE 1547.1 and IEEE 929-2000 islanding requirements.

Table 1. Electrical quantities/parameters of the system and parameters of the anti-islanding algorithm.

Electrical Quantity/Parameters	Value
V_{PCC}, f_b	200 V (peak), 50 Hz
X_g/R_g	1
Q_{Lmax}	2.5
S_{SC}	50 kVA
PL (it refers to the initial substation, P_{Ntot}*)*	4%
P_{Mtot}; $P_N[n]$; P_{Ntot}; *N*	5 kW; 500 W; 2 kW; 4
K; *REP*	0.5%, 2
T_{CC}; T_{Std}	6 or 8; 10 cycles
W(%); UF;	25; 2.5
CC_{islmin}*; $CC_{gridmax}$*; CC_{thr}*	0.2577; 0; 0.064
PCC-voltage (%) range for the U/O-V&F activation	85%, 110%

Note: * CC values are normalized for the initial power of the substation, i.e., 2 kW. When the 5 kW upgrade take place those values are expected to descend but withoud tripping the preset thresold of CC_{thr}.

4.1. Case I, Grid-Tied CSI Inverter Operates at Nominal Power While l Varies

Two subcases have been simulated for this case, considering the nominal inverters' power and maximum Q_L. Those cases consider three and four overlapping inverters, respectively (i.e., $l = 3$ and $l = 4$), implying that $T_{CC} = 6$ cycles, and 8 cycles, according to Equation (11).

Based on the simulation results that are presented in Figure 8, we can see that the island was progressively detected for the case of $l = 4$ (Figure 8b), whereas for $l = 3$ (Figure 8a) none of the inverters managed to detect the islanded operation. On the other hand, the U/O-V&F protection scheme of the remaining VSI inverter, was activated only after the disconnection of the *N*-Subgroup inverters where the PCC voltage had dropped below the limits defined in Table 1.

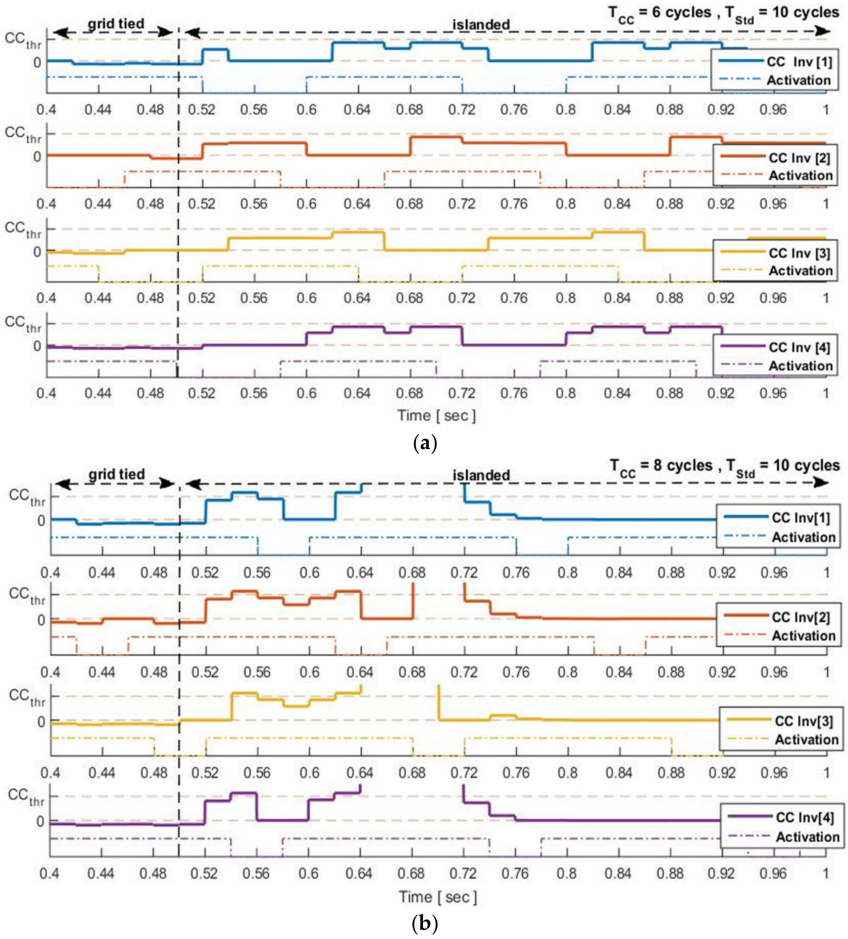
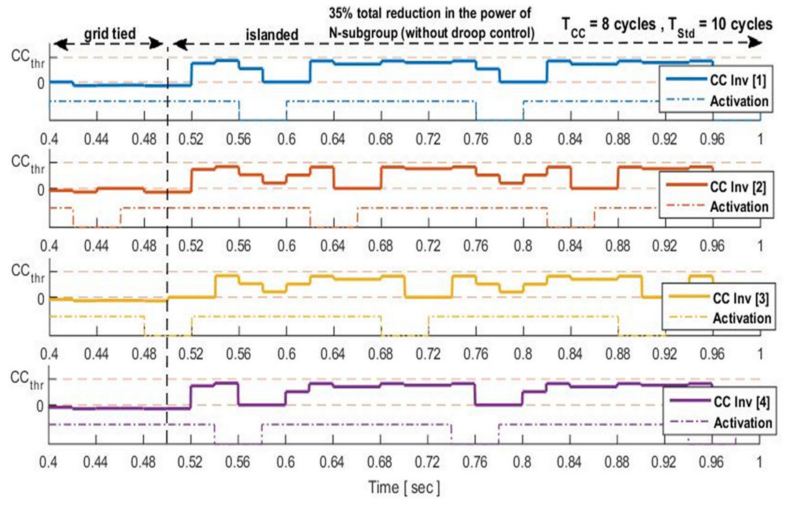


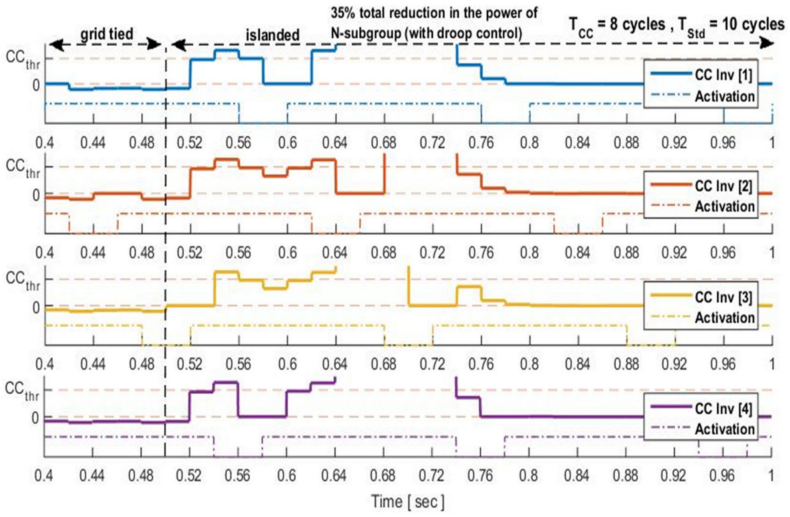
Figure 8. CC_{index} of inverters under nominal power operation, (**a**) $l = 3$ (T_{CC} = six cycles), (**b**) $l = 4$ (T_{CC} = eight cycles).

4.2. For Case II, l is Equal to 4, while the Power of CSI Is Reduced to 60%

In this subsection, the system undergoes a power reduction to investigate the impact of the inverter power and droop controller on the proposed technique. To do that, two subcases were simulated. In the first subcase the droop-controller was activated, whereas in the second one, the droop controller was inactive. According to the simulation results, the evolution of CC_{index} when the droop-controller is inactive (Figure 9a) was reduced by ~28% with respect to its initial value that is depicted in Figure 8, thereby failing to detect the islanded operation. On the other hand, the reduction of CC_{index} was effectively countered by the droop-controller (Figure 9b), leading to the successful detection of the islanded operation. Corresponding waveforms of inverters currents and PCC voltage are illustrated in Figure 10.

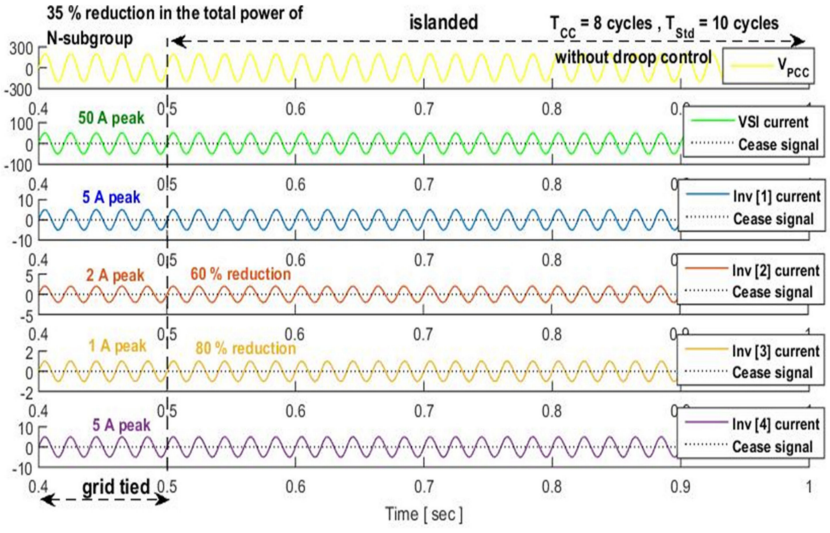


(**a**)



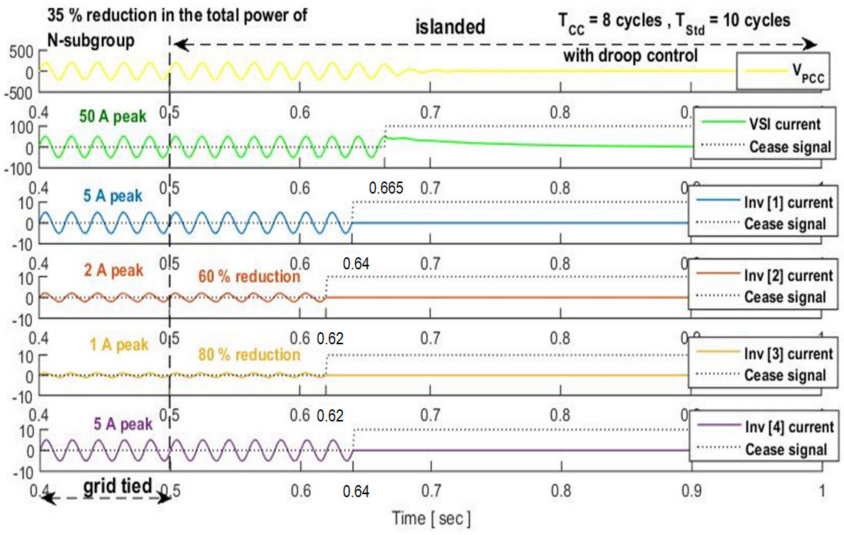
(**b**)

Figure 9. CC_{index} of inverters under reduced power operation (60% and 80% reduction for the inverters 2 and 3, respectively) for l = 4 (T_{CC} = 8 cycles), (**a**) without droop-controller, (**b**) with droop-controller.



(**a**)

Figure 10. *Cont.*



(**b**)

Figure 10. PCC voltage and inverter currents at reduced power levels (60% and 80% reduction for the inverters 2 and 3, respectively) and $l = 4$ ($T_{CC} = 8$ cycles), (**a**) without a droop-controller; (**b**) with a droop-controller.

5. Experimental Results

In order to examine the effectiveness of the aforementioned anti-islanding technique, a test bench of two CSI interleaved flyback inverters, operating in DCM, was constructed. The foremost components used in the inverters' circuitry, along with the system parameters and the parameters of the anti-islanding scheme, are recapped in Table 2. The inverters have been tested under a high quality factor ($Q_L = 2.5$) and load matching conditions. Moreover, two cases with different T_{CC} have been studied, i.e., $T_{CC} = 0.02$ s (1 cycle) and $T_{CC} = 0.12$ s (6 cycles). Finally, corresponding results, supporting the effectiveness of the proposed modified scheme are presented in Figures 11 and 12.

Table 2. System parameters and anti-islanding algorithm parameters of the experimental setup.

Electrical Quantity/Parameters	Value
Inverters Rating	$V_{dc} = 25 - 50$ V; $V_{ac\_rms} = 133$ V
Primary inductance; Turns ratio	30 μH; 1
R_L; L_L; C_L; Q_L	235 Ω; 290 mH; 35 nF; 2.5
X_g/R_g; PL	1; 17%
L_g; R_g	28.9 mH; 9.1 Ω
N	2
P_{Ntot} ($P_N[1] = P_N[2]$)	75 W
$CC_{isl\text{-}min}$; $CC_{grid\text{-}max}$; CC_{thr}	0.5; 0.14; 0.47
T_{Std}; T_{CC}	0.2 s (10 cycles); 0.02 s (1 cycle for the conventional method) or 0.12 s (6 cycles for the proposed method)

In Figure 11, the CC_{index} of both cases in an islanded-operation is illustrated. In the first case, the CC_{index} does not surpass the predefined CC_{thr} as a result of the lack of power in the second harmonic, meaning the anti-islanded method fails. In second case, when inverters are overlapped, the CC_{index} surpasses CC_{thr} and the method detects the islanded-operation.

Figure 12 illustrates the evolution of CC_{index} along with V_{PCC} and V_{ref}, in both islanded and grid-tied operation, and the evolution of the integration in the case of overlapping inverters. Finally, in accordance with the aforementioned standards, the island was detected in less than 10 fundamental cycles.

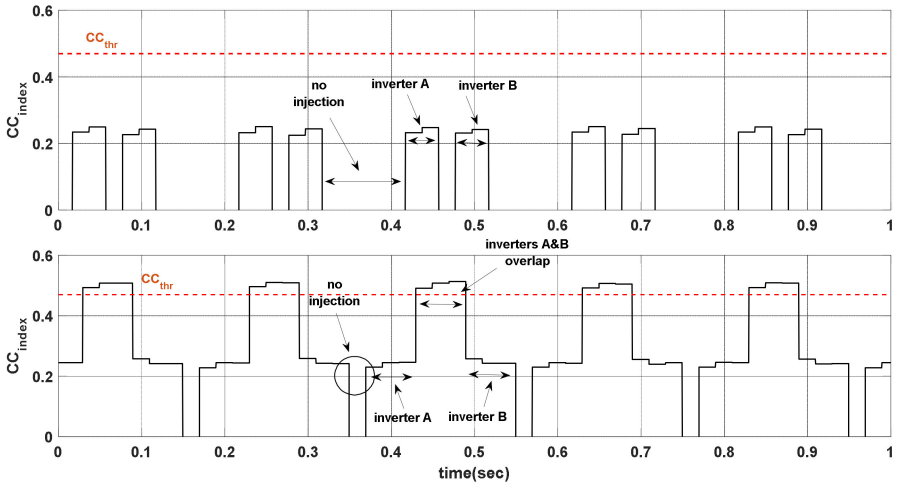


Figure 11. Evolution of CC_{index} in an islanded operation for the two injection patterns, (**top graph**) 1/10 cycles, (**bottom graph**) 6/10 cycles.

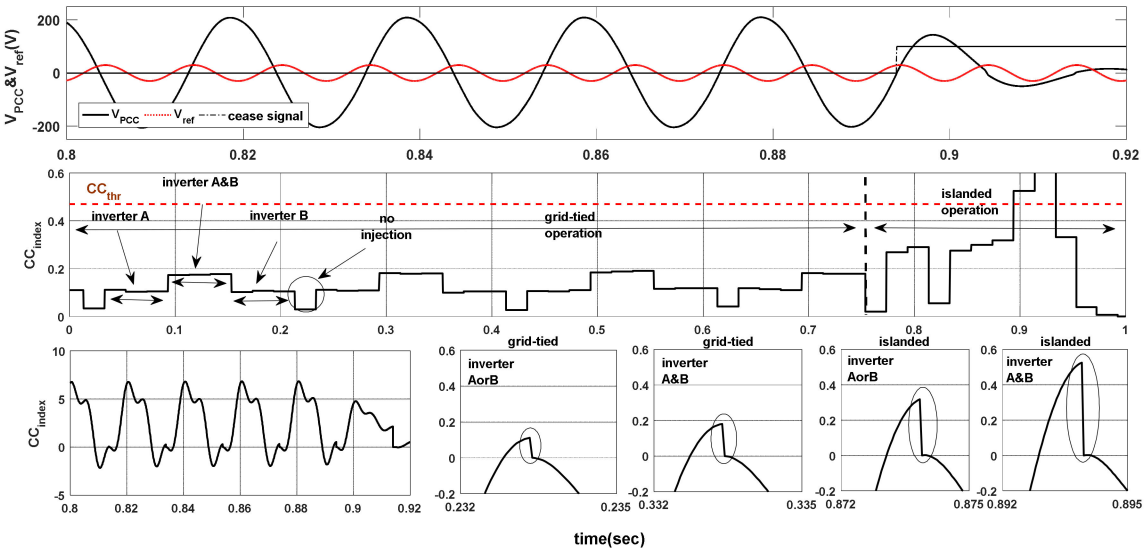


Figure 12. (**top graph**) V_{PCC} along with V_{ref}, (**middle graph**) evolution of CC_{index} in grid tied and islanded operation, (**bottom graph**) evolution of the CC_{index} calculation.

6. Conclusions

In this work, a strategy was proposed that enables the harmonic injection scheme that was presented in reference [2] to be implemented in multiple grid-tied inverters. Furthermore, a generalized mathematical model for the case of multiple grid-tied inverters was presented. Extensive simulation and experimental results were presented that verify the above outcomes. It was shown that the islanded operation can be detected, even when multiple grid-tied inverters are connected to the same node. The detection time has been recorded, within 10 fundamental cycles (from the activation of the algorithm), coping with all relevant anti-islanding as well as power quality standards. In conclusion, the proposed anti-islanding technique provides a very promising solution for the anti-islanding protection of grid-tied inverters that are connected to the same node, as well as a low computation cost solution with a reduced NDZ.

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Nomenclature

PV	Photovoltaic generator
PCC	Point of Common Coupling
NDZ	Non- detection zone
FDZ	Fault-detection zone
THDi	Total harmonic distortion of the inverter output injected current
DPF	Displacement power factor
MPPT	Maximum power point tracking
PLL	Phase locked loop
CSI, VSI	Current and Voltage Source Inverter
DER-CSI	Distributed energy resource current source inverter
CC	Cross-correlation
N	Initial number of inverters that are using the proposed anti-islanding technique
M	Additional number of inverters that can be installed at PCC without compromising the effectiveness of the proposed anti-islanding technique
l	Minimum number of the inverters of the N-subgroup, which perform the harmonic injection, and are required to in order to achieve the desired overlap
m	Number of M-subgroup inverters that may (or may not) use the proposed anti-islanding technique
DCM	Discontinuous conduction mode
REP	Consecutive times that the anti-islanding threshold must be surpassed before the identification of islanded-operation
R_L, C_L, L_L	Equivalent resistance, capacitance, and inductance of the islanded network
S_{SC}	Short circuit power at PCC (VA)
ω_b. f_b, T_b	Utility base angular frequency, utility base frequency, and utility base period
X_g, R_g	Equivalent grid internal impedance (at base angular frequency ω_b) and resistance at PCC
Q_L	Quality factor of islanded network
i	Islanded ($i = isl$) or grid-tied ($i = grid$) operation
$H_{i,h}$, $e_{i,h}$	Index and evaluation function of the anti-islanding technique
V_{PCC}, $\hat{V}_{PCC}$	Instantaneous and peak value of PCC voltage
$\hat{V}_{PCC,i,h}$	Peak value of the h-order harmonic component of PCC voltage in islanded or grid-tied operation; it refers to the component that is induced by the islanding-scheme and not to the pre-existing harmonics of the grid-voltage
$\hat{V}_{PCC,i,1}$	Peak value of the fundamental component of PCC voltage

$\hat{I}_{i,h}$	Peak value of the harmonic current component which is injected by inverter (imposed by the anti-islanding technique), in grid-tied or islanded operation
K	Rated ratio of the fundamental-harmonic current components of the inverter
K^*	Actual value of K (activated during the droop control mode)
$Gain_i$	Inverter gain in in grid-tied or islanded operation
T_{Std}, T_{CC}	Periodicity and duration of the harmonic injection
$Z_{i,h}$	Impedance at the output stage of the inverter (at h-order), in grid-tied or islanded operation
$\zeta_{i,h}$	$= \|Z_{grid/isl,h}\|/R_L$
$\hat{V}_{ref}$	Peak value of the reference that is used in the proposed scheme [2]
S	Number of samples that is used to calculate the CC_{index} according to (3)
$\Delta_{\varphi CC,i}$	Phase angle between $\hat{V}_{PCC,i,h}$ and the reference signal
CC_{index}	Cross-correlation index
CC_{grid}, CC_{isl}	Cross-correlation sequence index of the PCC voltage during the grid-tied operation or islanded operation
$CC_{gridmax}$	Maximum value of CC_{grid} [2]
CC_{ilsmin}	Minimum value of CC_{isl}, [2]
CC_{thr}	Threshold-value that is used in the proposed method ($CC>CC_{thr}$ for islanded operation)
W%	Margin between the islanded and grid-operation (as a percentage)
$P_N[n]$	Nominal power of each inverter of the N-subgroup
$P_N^*[n]$	Actual power of each N-subgroup inverter
P_{Ntot}	Total nominal power of N-subgroup
$P_M[m]$	Nominal power of each inverter of the M-subgroup
P_{Mtot}	Total nominal power of M-subgroup
P_{tot}	Total nominal power of the installation (including both the N-subgroup and the M-subgroup inverters)
PL	$= P_{Ntot}/S_{SC}$, penetration level of PV-units that are connected at the same node and utilize the proposed anti-islanding method
UF	$= P_{Mtot}/P_{Ntot}$, upgrade factor of the installation
U/O-V&F	Under/Over Voltage & Frequency, it is a widely used passive anti-islanding technique

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