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Phase-Based Fractional-Order Repetitive Control for Single-Phase Grid-Tied Inverters

Qiangsong Zhao [1], Hao Dong [1,2], Guohui Zhou [2] and Yongqiang Ye [2,*]

[1] The School of Automation and Electrical Engineering, Zhongyuan University of Technology, Zhengzhou 450007, China; zhaoqiangsong@zut.edu.cn (Q.Z.); bx2503514@nuaa.edu.cn (H.D.)
[2] The College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 211106, China; zhouguohui@zut.edu.cn
* Correspondence: melvinye@nuaa.edu.cn

Abstract

A novel fractional-order repetitive control based on phase angle information interpolation is proposed for single-phase LCL-type inverters in this paper. Conventional fractional-order repetitive control typically relies on inaccurate grid frequency information detected by a phase-locked loop or the frequency-locked loop, which may result in a potential degradation in harmonics suppression capability. To address this issue, phase information is investigated to implement the fractional order of the repetitive controller through the linear interpolation method. A major advantage of the proposed scheme lies in that it avoids explicit frequency calculation and reduces sensitivity to frequency estimation fluctuations compared with conventional fractional-order repetitive control, enhancing its frequency adaptability. The stability analysis and the design process for the proposed scheme based on a plug-in-type repetitive control are given. Experimental results support the efficacy and advantages of the proposed control strategy.

Keywords: grid-tied inverters; fractional-order repetitive control; harmonics suppression; frequency adaptation; phase angle

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1. Introduction

In recent decades, distributed power generation systems (DPGSs), such as solar energy and wind energy, have experienced rapid growth and grid-tied inverters have emerged as an important interface that connects DPGSs to the power grid [1]. To minimize grid pollution, it is essential to maintain a minimal level of total harmonic distortion (THD) while ensuring a significantly high power factor. Therefore, the quality of the injected current is crucial.

Many current control schemes, such as proportional-integral (PI) control [2], resonant control [3], sliding mode control [4,5], and model predictive control [6], have been proposed for grid-tied inverters to deal with low-frequency harmonics stemming from nonlinear elements, including dead-time in pulse width modulation (PWM) inverters and nonlinear loads. Among these schemes, multi-resonant control for harmonic compensation can eliminate the selected harmonic components in the injected current [7]. However, it demands more design efforts and computational resources [8]. With a simple form, repetitive control (RC) allows for precise tracking of periodic signals with zero steady-state error or effective suppression of multiperiod disturbances due to its high gains at harmonic frequencies [9–11]. By introducing a phase-lead compensator, the phase lag caused

by the plant can be effectively mitigated, making the controlled plant closer to the ideal characteristics required by RC, characterized by unity gain and zero phase shift within the specified bandwidth [12]. Moreover, with a plug-in repetitive controller, additional harmonics suppression performance can be achieved on the top of the base feedback controller [13]. In addition, a high-order repetitive control (HORC) [14] strategy has been explored for mitigating time-varying periodic disturbances.

For practical applications, RC is commonly employed in the discrete-time domain. The conventional RC (CRC), represented by $z^{-N}/(1-z^{-N})$, can achieve zero steady-state error only when $f_s/f_g = N \in \mathbb{N}$, where f_s refers to the sampling frequency, f_g is the grid frequency of the inverter system, and N is the RC order. However, variations in grid frequency compromise the integer order of RC, thereby reducing open-loop gains at harmonic frequencies. To address this issue, two common approaches are employed: adjusting the sampling frequency and adopting frequency-based fractional-order filters. In particular, the time-varying sampling frequency method changes the sampling frequency online in response to fluctuations in grid frequency, thereby maintaining a consistent integer order for RC [15]. In [16], a multi-rate repetitive control is employed, precisely synchronizing the signal and control periods by adjusting the controller's sampling time. In [17], a spatial RC, which utilizes the phase sampling technique to sample the grid voltage's phase angle, has been proposed. Although it achieves a consistent number of samples in each cycle, it faces similar challenges as the previously mentioned method involving varying sampling rates. Ref. [18] implements a Gaussian process for the interpolation and extrapolation in the spatial RC to maintain a fixed sampling rate even though the scheme is a bit complex.

Moreover, the fractional-order RC (FORC) strategy is adopted to approximate the actual fractional order of RC. This method is especially pertinent when the grid frequency experiences variations, as delineated in several works. In [19], Escobar et al. pointed out that the order of RC could be a fraction when the grid frequency fluctuates and the sampling frequency is limited. They presented a solution to compensate for fractional delay with a finite impulse response (FIR) filter. In [20], a third-order FIR filter is used to approach the fractional order of RC for a programmable ac source. In [21], an infinite impulse-response (IIR) filter with a phase compensator can also achieve frequency adaptivity for grid-tied inverters. In [22], Valdez-Fernández et al. proposed a 6 h $\pm$ 1 repetitive scheme for a three-phase CHB seven-level converter in shunt APF applications, where a Farrow structure was introduced to compensate the variable fractional delay (VFD) induced by grid frequency deviations.

The grid frequency of the power grid from a phase-locked loop (PLL) or frequency-locked loop (FLL) is used to calculate the order of RC in the above-mentioned conventional FORC (CFORC). However, the detected frequency of the power grid may exhibit fluctuations in single-phase inverters. For instance, the output frequency of the PLL based on the second-order generalized integrator (SOGI) varies, even though these fluctuations can be mitigated to some extent with more advanced numerical techniques [23]. The voltage distortions at the point of common coupling (PCC) further exacerbate the situation. While more advanced PLL schemes are available to detect the grid frequency in three-phase inverters, single-phase inverters face greater challenges and increased complexity because of the limited availability of the grid voltage information. The undesired fluctuation of the estimated grid frequency leads to an imperfect order of RC, thus deteriorating the harmonics rejection performance of the CFORC schemes [24].

To tackle this challenge, the angle information from the PLL can be used to ascertain the grid frequency, and then deriving the order of RC. The contributions presented in this paper are as follows.

(1) The output frequency of the second-order generalized integrator (SOGI)-based PLL naturally fluctuates, resulting in an inaccurate order of RC in a single-phase inverter, and then affecting the performance of RC. To solve this challenge, a novel phase-based fractional-order repetitive control (PFORC) scheme is developed in this paper.
(2) Based on the linear interpolation method, the different weights are employed for the phase angles from PLL to determine the order of RC, which enhances the frequency adaptability of the PFORC scheme by mitigating the impact of fluctuations in the estimated grid frequency.
(3) A detailed PFORC design procedure and the real-time comparative experimental validation on the single-phase *LCL*-type grid-tied inverters are presented, in which both performance and robustness are considered.

2. Conventional Frequency-Based Fractional-Order Repetitive Control

The structure of a plug-in RC system is shown in Figure 1. In Figure 1, $C(z)$ is the base controller, $P(z)$ is the plant. $r(z)$ and $y(z)$ are the reference and feedback signals, respectively. $e(z)$ is the error and $u_{RC}(z)$ is the control output of RC, k_{RC} is the gain of RC, $Q(z)$ is a constant within $(0, 1)$ or a zero-phase low-pass filter in the form of $d_1 z + d_0 + d_1 z^{-1}$ satisfying $2d_1 + d_0 = 1$, aimed at boosting the system's stability margin, and $G_f(z)$ is a compensation filter written as

$$G_f(z) = G_i(z) z^m \tag{1}$$

where $G_i(z)$ is typically a low-pass filter, and z^m is a phase lead compensator with m lead steps.

The transfer function of CRC is

$$G_{CRC}(z) = \frac{u_{RC}(z)}{e(z)} = k_{RC} \frac{z^{-N} Q(z)}{1 - z^{-N} Q(z)} G_f(z). \tag{2}$$

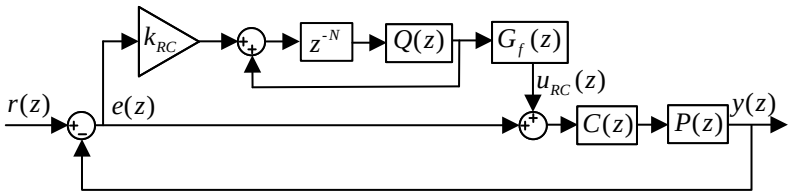


Figure 1. Block diagram of the plug-in RC system.

When $N \in \mathbb{N}$, $G_{RC}(z)$ has high gains at harmonic frequencies, and therefore, it can effectively attenuate harmonic signals.

However, the open-loop gains at harmonic frequencies will decay when the fundamental frequency fluctuates, resulting in a deteriorated harmonics suppression performance of CRC. In [20], a CFORC is proposed to solve this problem. The order of RC (N), which is calculated by f_s/f_g, can be segmented into two components: an integer portion N_i and a fractional portion N_F, as shown in Figure 2. Then, an FIR filter is employed to approximate the fractional part z^{-N_F} as follows:

$$z^{-N_F} \approx G_{FIR}(z) = \sum_{k=0}^{n} A_k z^{-k} \tag{3}$$

where n is the order of FIR filter, $k = 0, 1, ..., n$, and A_k can be calculated by

$$A_k = \prod_{i=0, i \neq k}^{n} \frac{N_F - i}{k - i}. \tag{4}$$

Typically, a larger n leads to less magnitude attenuation at low frequencies, which better approximates the unit gain. However, a high-order FIR fractional filter will increase the implementation complexity and change the closed-loop zeros of the system, and, the zeros may affect the dynamic response speed as well as the harmonic rejection ability. Therefore, in practice, the order of the adopted FIR fractional filter in the CFORC system is within the third order [24,25]. When a plug-in CFORC is employed, the stability conditions are of the same form as those of CRC [26]:

1. The closed-loop transfer function without RC, $T(z) = \frac{C(z)P(z)}{(1+C(z)P(z))}$, is stable;
2. $|Q(z)G_{FIR}(z)[1 - k_{RC}G_f(z)T(z)]| < 1$.

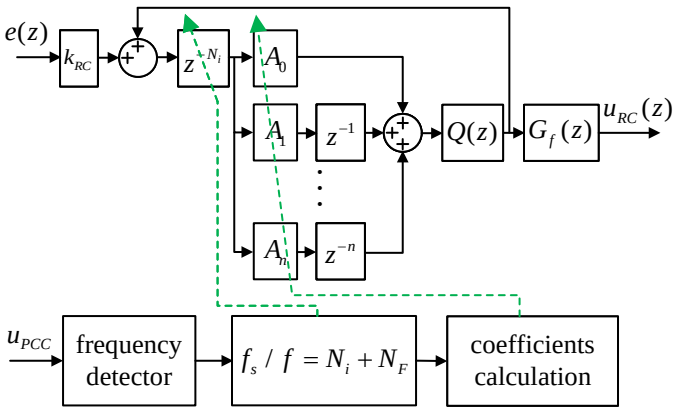


Figure 2. Block diagram of CFORC.

In practice, even if a narrow bandwidth of PLL or FLL is selected, the detected frequency from a typical SOGI-based PLL can fluctuate [27]. And then, the order of CFORC based on the frequency information will fluctuate, resulting in a degradation in harmonics suppression when the grid frequency remains fixed and a fixed order of RC is expected.

3. Proposed Phase-Based Fractional-Order Repetitive Control

3.1. Principle

The underlying principle of PFORC is to implement a repetitive controller based on phase angle information. In short, the order of RC can be determined by the number of interval samples of the same phase angle value. However, in practice, it is not possible to find the exact same phase angle in an adjacent fundamental wave period. Therefore, a linear interpolation method is needed for approximating the order of RC, with the interpolation coefficient calculated from the phase angle values. At time step k, it is appropriate to get a phase angle closest to the output current phase angle from the previous cycle. It is sufficient for the difference between these two phase angles to be less than $2\pi * f_{min}/f_s$, where f_{min} is the lower limit frequency of the varying grid frequency.

The order of RC can be categorized into two parts: the integer part $N(\alpha)$ and the fractional part N_f. Notably, the order of RC can be calculated by identifying the two time steps $\bar{k}$ and $\bar{k}-1$, where $\bar{k}$ and $\bar{k}-1$ are the sampling time steps of the last repetitive period in which corresponding the phase angles $\alpha_{\bar{k}}$ and $\alpha_{\bar{k}-1}$ are closest to the current phase angle α_k, which is typically the adjacent sampling point of the same phase angle $N(\alpha)$ of last repetitive period. α_k lies between $\alpha_{\bar{k}}$ and $\alpha_{\bar{k}-1}$, as shown in Figure 3a. Therefore, the integer part can be formulated as

$$N(\alpha_k) = k - \bar{k}. \tag{5}$$

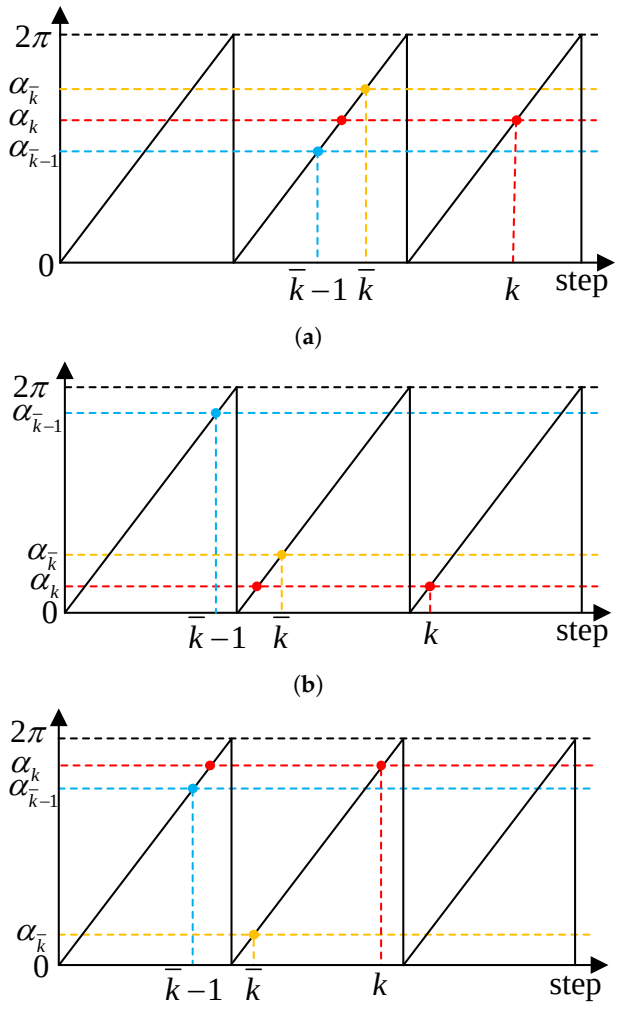
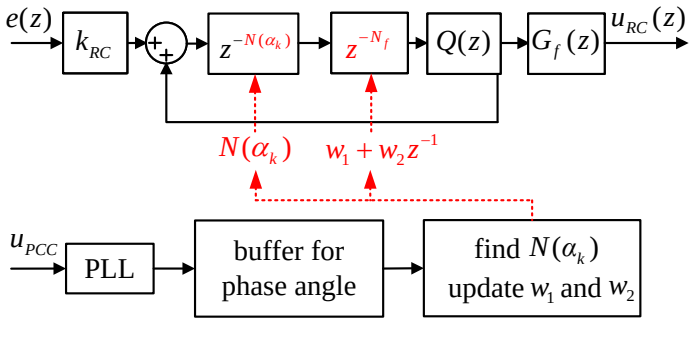


Figure 3. Phase angle versus sampling time step: (**a**) $\alpha_{\bar{k}-1} < \alpha_k < \alpha_{\bar{k}}$, (**b**) $\alpha_k < \alpha_{\bar{k}} < \alpha_{\bar{k}-1}$, and (**c**) $\alpha_{\bar{k}} < \alpha_{\bar{k}-1} < \alpha_k$.

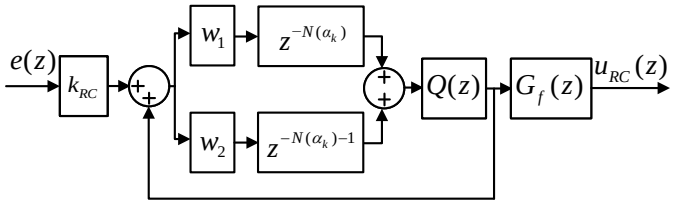
Based on the Lagrange interpolating method with the first order, the fractional part of the order can be derived from the weighting of phase angle differences between $\alpha_{\bar{k}}, \alpha_k, \alpha_{\bar{k}-1}$. The linear interpolation of PFORC is shown in Figure 4a, where w_1 and w_2 represent the linear interpolation weights to approximate the ideal RC order. As a consequence, the delay line of RC can be written as

$$z^{-N} = z^{-(N(\alpha_k)+N_f)} = z^{-N(\alpha_k)} \cdot (w_1 + w_2 z^{-1}). \tag{6}$$



(**a**)

Figure 4. *Cont.*



(**b**)

Figure 4. Diagram of PFORC: (**a**) PFORC with linear interpolation, (**b**) simplified diagram.

In practice, the phase angle of the reference current is restricted within $[0, 2\pi)$. Figure 4 illustrates the correlation between the phase angle of the phase around 2π and the sampling time step in all three cases. In the case of Figure 3a, where $\alpha_{\bar{k}-1} < \alpha_k < \alpha_{\bar{k}}$, the weights w_1 and w_2 can be expressed as follows:

$$\begin{cases} w_1 = \dfrac{\alpha_k - \alpha_{\bar{k}-1}}{\alpha_{\bar{k}} - \alpha_{\bar{k}-1}}. \\ w_2 = 1 - w_1 \end{cases} \tag{7}$$

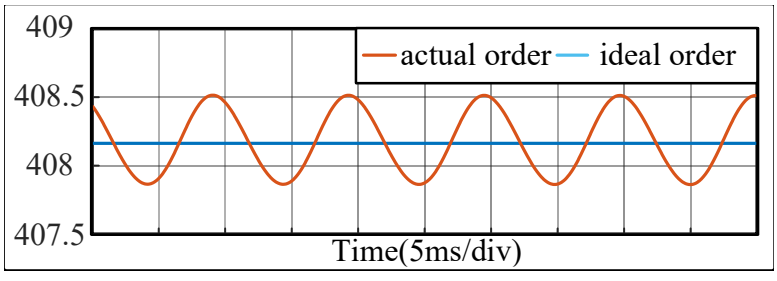
In the case of Figure 3b, where $\alpha_k < \alpha_{\bar{k}} < \alpha_{\bar{k}-1}$, the weights w_1 and w_2 can be given as follows:

$$\begin{cases} w_1 = \dfrac{\alpha_k + 2\pi - \alpha_{\bar{k}-1}}{\alpha_{\bar{k}} + 2\pi - \alpha_{\bar{k}-1}}. \\ w_2 = 1 - w_1 \end{cases} \tag{8}$$

In the case of Figure 3c, where $\alpha_{\bar{k}} < \alpha_{\bar{k}-1} < \alpha_k$, the weights w_1 and w_2 can be given as follows:

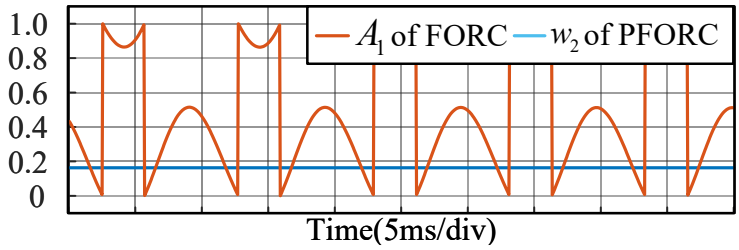
$$\begin{cases} w_1 = \dfrac{\alpha_k - \alpha_{\bar{k}-1}}{\alpha_{\bar{k}} + 2\pi - \alpha_{\bar{k}-1}} \\ w_2 = 1 - w_1. \end{cases} \tag{9}$$

As shown in Figure 5a shows, when a SOGI-based PLL is used for frequency detection, the order of CFORC fluctuates, leading to the fluctuation of weight A_1, as illustrated in Figure 5b when $n = 1$. The fluctuation in the calculated order of RC can deteriorate the performance of harmonics suppression when the grid frequency remains stable and a integral order of RC is expected. However, the fluctuation of the weights is mitigated, as depicted in Figure 5b, where w_2 remains almost constant at a steady state.



(**a**)

Figure 5. *Cont.*



(**b**)

Figure 5. Simulation results under 49 Hz sinusoidal grid voltage at a steady state: (**a**) order N of CFORC, (**b**) value of weight coefficients: A_1 and w_2.

Remark 1. *The phase information of PLL can be used in the design of RC to circumvent the fluctuation problem in frequency detection. Compared to frequency-based CFORC, PFORC in the angular domain is more advantageous when the repetitive features of the reference or disturbance signals are reflected in the distribution of angular positions.*

3.2. Implementation

At each sampling step, the updated phase angle is used to calculate the interpolation weights and stored in a memory buffer for subsequent period calculations. The buffer size for phase angle α should hold at least the maximum number of points per period, denoted as $N_{\max}$. Thus, $N_{\max} = \max[N(\alpha_k)] + 1$. For example, if the grid frequency varies in the range of 49 Hz to 51 Hz while the system samples and updates at a frequency of 20 kHz, then $\max[N(\alpha_k)] = floor(20,000/49) = 408$, $N_{\max} = \max[N(\alpha_k)] + 1 = 409$.

The simplified diagram of PFORC is presented in Figure 4b, where $\omega_1 + \omega_2$ serves as an online mechanism for updating the RC order. Actually, PFORC exhibits an equivalent structure to CFORC during steady-state operations when the detected grid frequency remains constant, and the order of the fractional delay filter in CFORC is set to 1, (indicating the use of a linear interpolation polynomial). Thanks to the delay internal model, the structure of RC in Figure 4b can be implemented, as shown in Figure 6, where $W(z) = w_1 + w_2 z^{-1}$. In the transformed structure, $z^{-1}Q(z) = d_1 + d_0 z^{-1} + d_1 z^{-2}$ is physically realizable.

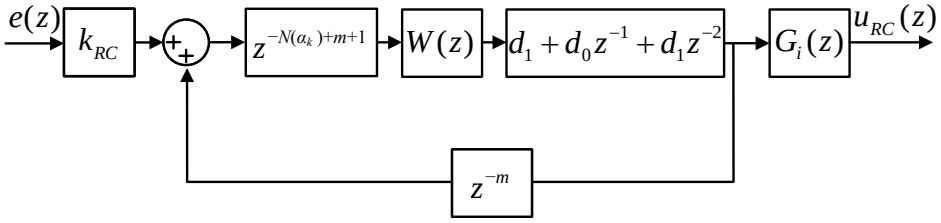


Figure 6. Structure for implementation.

3.3. Stability Conditions

In the implementation of PFORC, the phase angle of PLL is directly used for interpolation. An SOGI-based PLL is employed in this paper. High-order discretization of integrators leads to less ripple but more implementation efforts and computational burden [23]. Thus, integrators are discretized by feed-forward and backward Euler methods for simplicity. Phase from other types of PLL can also be used to calculate the weights w_1 and w_2. It is noted that a narrow bandwidth of PLL is preferred for system stability [28]. Actually, considering that the maximum fluctuation rate of A is constrained [25], and the bandwidth of PLL is narrow, the online updating weights w_1 and w_2 only change slightly. So even though strict and conservative stability conditions have been proposed in [29], the stability conditions of the PFORC system are consistent with CFORC [20]:

① The system without RC is stable: $T(z)$ is stable;
② $|Q(z)W(z)[1 - k_{RC}G_f(z)T(z)]| < 1$.

4. Application to a Single-Phase *LCL*-Type Grid-Tied Inverter

4.1. Modeling of the Single-Phase LCL-Type Grid-Tied Inverter

Figure 7 shows a single-phase *LCL*-type grid-tied inverter controlled by a plug-in RC, in which L_1, L_2, and C refer to the inverter-side filter inductor, grid-side filter inductor, and filter capacitor, respectively; I_{ref} is the amplitude of the reference current i_{ref}; i_2 is the current of L_2, respectively; i_c is the capacitor current; u_g is the grid voltage; u_{PCC} is the voltage of the PCC; u_{dc} is the dc bus voltage; L_g is the grid inductor. A PLL is employed to synchronize i_{ref} with the phase angle of the grid. The phase angle from PLL α is fed into G_{RC} for buffering. The capacitor current plays a role in actively damping the resonance peak, where K_d is the active damping gain.

Figure 8 illustrates the system's control diagram. The gain of the inverter bridge is represented by K_{pwm}, and $G_h(s)$ symbolizes the zero-order-hold of PWM. This can be closely represented approximately as a time delay, specifically $0.5T_s$, as suggested in [30]. Taking into account the digital control delay, the discrete transfer function of the open-loop gain without G_{RC} is derived (see Appendix A) as follows:

$$H(z) = \frac{G_{PI}(z)}{\omega_r(L_1+L_2)(z-1)} \times \frac{\omega_r T_s(z^2 - 2z\cos\omega_r T_s + 1) - (z-1)^2 \sin\omega_r T_s}{\left[z(z^2 - 2z\cos\omega_r T_s + 1) + (z-1)\frac{K_d \sin\omega_r T_s}{\omega_r L_1}\right]} \tag{10}$$

where ω_r denotes the resonant angular frequency of the *LCL* filter, which is formalized as

$$\omega_r = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C}}. \tag{11}$$

The corresponding closed-loop transfer function with $k_{RC} = 0$ is

$$T(z) = \frac{H(z)}{1 + H(z)}. \tag{12}$$

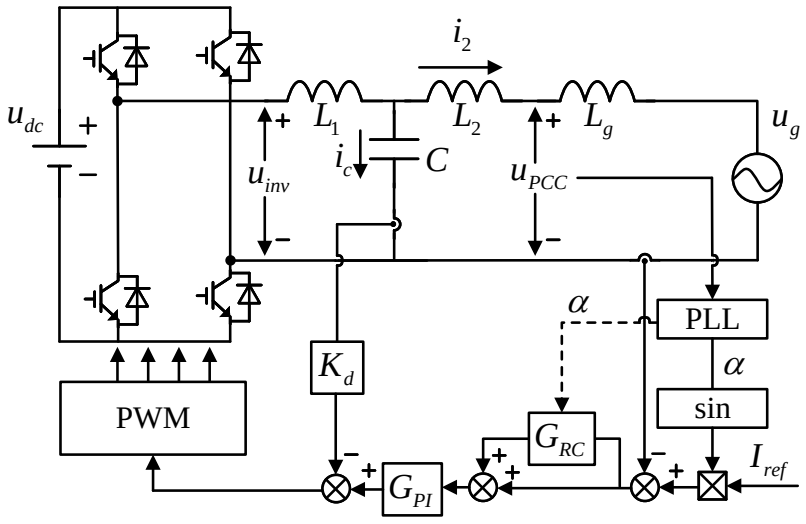


Figure 7. Plug-in RC of *LCL*-type single-phase grid-tied inverter.

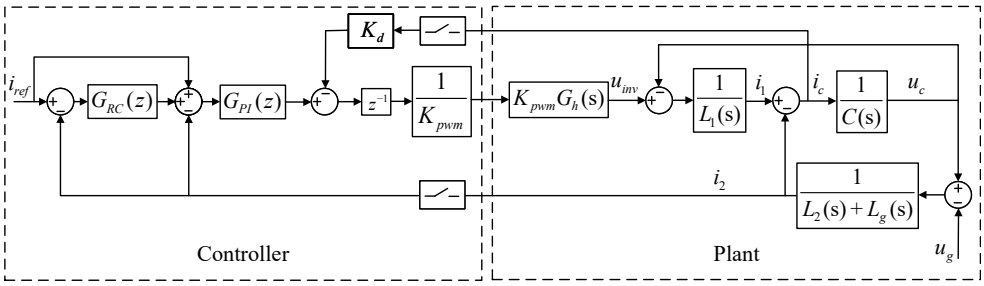


Figure 8. Control diagram of the single-phase *LCL*-type grid-tied inverter with grid inductance.

4.2. Controller Design

As depicted in Figure 8, $G_{PI}(z)$ is in the inner loop while $G_{RC}(z)$ is in the outer loop. Therefore, the PI controller, along with the active damping gain, should be tuned first considering system parameters. Then RC parameters can be determined based on the pre-tuned inner closed-loop.

4.2.1. PI Controller and Active Damping Gain

The base controller is used to ensure that the closed-loop function, $T(z)$, is stabilized. In this paper, a PI controller served as the base controller. The mathematical representation of a PI controller in discrete form is given by

$$G_{PI}(z) = k_p + \frac{k_i T_s}{z-1} \tag{13}$$

where T_s is the sampling period. Table 1 enumerates the system parameters utilized throughout this study. The selection of PI parameters and the active damping gain K_d should ensure a flat magnitude frequency response of $T(z)$ at the low frequency. Compared with unit gain, a flat closed-loop magnitude frequency response can reduce errors and be easily compensated by $G_f(z)$ (cf. the stability condition ② of PFORC). The selection of the system crossover frequency f_c is actually affected by the resonant frequency f_r. In instances where the resonant frequency f_r falls under one-sixth of the sampling frequency, the loop gain crosses -180° at f_r [31]. In this case, the crossover frequency f_c must be set lower than the resonant frequency f_r for system stability. The resonant frequency decreases as the grid inductance increases so that $f_{r\min} = \frac{1}{2\pi}\sqrt{1/L_1C} \approx 1.2$ kHz. An f_c of 650 Hz is selected, nearly half of $f_{r\min}$. Then k_p is calculated by [2]:

$$k_p \approx 2\pi f_c(L_1 + L_2) \approx 20. \tag{14}$$

Thus, $k_p = 20$ is selected.

Table 1. System parameters.

Symbol	Quantity	Nominal Value
u_{dc}	DC-link voltage	380 V
u_g	Grid voltage (RMS)	220 V
P_o	Output power	2 kW
C_{dc}	DC bus capacitor	1360 uF
L_1	Inverter side inductance	2.9 mH
C	Filter Capacitor	6 µF
L_2	Grid side inductance	2 mH
f_{sw}	Switching frequency	10 kHz
f_s	Sampling frequency	20 kHz
f_{bw}	PLL bandwidth	15 Hz
ζ_{PLL}	PLL damping ratio	0.707
K_{PWM}	PWM Gain	1

The integral term $k_i T_s/(z-1)$ is found to have a negligible impact on system stability [32], which allows for the subsequent determination of the active damping gain, K_d. Let $G_{PI} = k_p$, the magnitude frequency responses of closed-loop transfer function $T(z)$ with different damping coefficients K_d are illustrated in Figure 9. It can be seen that when $K_d = 25$, $T(z)$ exhibits the smoothest magnitude frequency response, which means $T(z)$ is nearly a unit gain at low frequency and provides a greater stability margin for RC. Hence, $K_d = 25$ is selected. As k_i increases, the gain of $H(z)$ at the low frequency rises while the phase margin of $H(z)$ decreases. To balance between phase margin and dynamic response, $k_i = 15{,}000$ is selected. The final phase margin and the gain margin of $H(z)$ are 50° and 4.7 dB, respectively.

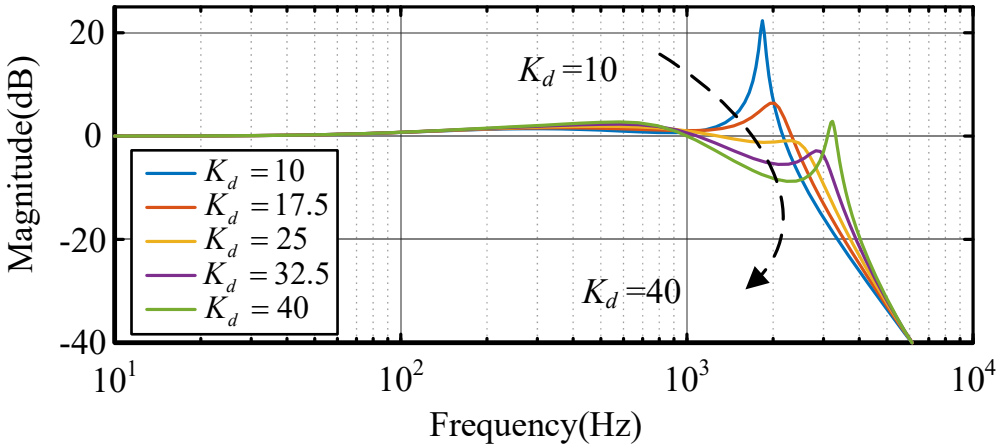


Figure 9. Magnitude frequency responses of $T(z)$ with different K_d.

4.2.2. $Q(z)$

$Q(z)$ is to ensure a safe margin with respect to stability condition ②. A low-pass filter with zero-phase characteristics significantly enhances the stability margin in the high-frequency range. Hence, $Q(z) = 0.05z + 0.9 + 0.05z^{-1}$ is chosen to provide enough gain in the low-frequency range.

4.2.3. $G_f(z)$

$G_f(z)$ functions as a compensation filter and approximates the inverse of $T(z)$ at low frequencies. As Equation (1) shows that the design of $G_f(z)$ can be categorized into two parts, $G_i(z)$ for high-frequency attenuation and z^m for phase compensation. For simplicity, a Butterworth low-pass filter with a second-order configuration is employed for its flat frequency response in the passband. The main harmonics are below the 20th harmonic, so a cutoff frequency of 1000 Hz is selected for the filter. $G_i(s)$ is then discretized with bi-linear transformation:

$$G_i(z) = \frac{0.01979z^2 + 0.03958z + 0.01979}{z^2 - 1.565z + 0.6437}. \tag{15}$$

After the filter $G_i(z)$ has been designed, the lead step m should be selected to compensate for the phase lag of the system at the low frequency. Figure 10 displays the phase–frequency responses of $T(z)G_i(z)z^m$ with different m. As shown in Figure 10, increasing m enhances the maximum phase lead but narrows the effective bandwidth. Specifically, $m = 8$ provides only limited phase improvement, whereas $m = 13$ yields a larger phase lead at the expense of a significantly narrower bandwidth. The phase–frequency curves indicate that $m = 11$ achieves a phase of $T(z)G_f(z)$ closest to 0°. Thus, $m = 11$ is selected

in conjunction with the designed $G_i(z)$ to compensate $T(z)$ and approximate unit gain in the low-frequency range.

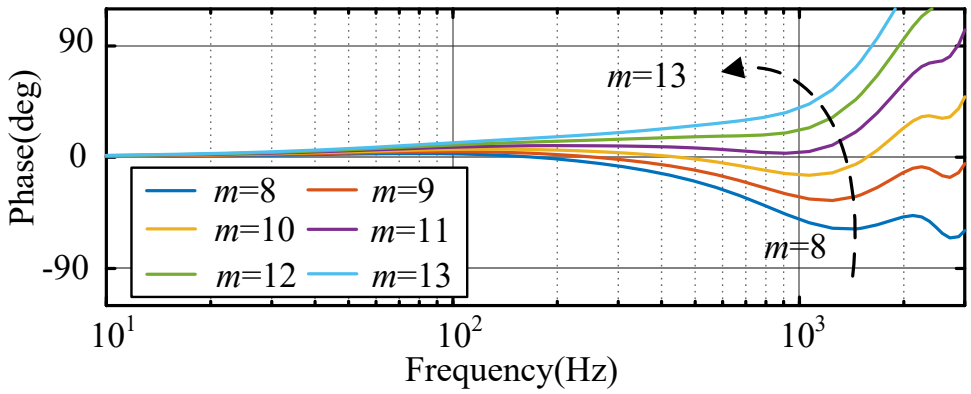


Figure 10. Phase frequency responses of $T(z)G_f(z)$ with different m.

4.2.4. k_{RC}

It is revealed that the larger the value of k_{RC}, the better the steady-state response and dynamic performance. But it can also deteriorate the stability of the system. Let

$$M = \max(|1 - k_{RC}T(z)G_i(z)z^m|). \tag{16}$$

If $20\lg(M) < 0$ dB, system stability is ensured. System stability is assessed while varying L_g up to 0.1 PU, corresponding to a short-circuit ratio of about 10 [32], and

$$L_{g_{\max}} = \frac{u_g^2}{2\pi f_g 10 P_o} \approx 7.7\,\text{mH}. \tag{17}$$

Thus, 8 mH is selected as the upper bound of L_g. Figure 11 shows the distribution of $20\lg(M)$ concerning k_{RC} and L_g. As grid inductance L_g increases, the stability region for k_{RC} decreases. When $L_g = 8$ mH, the stability region for k_{RC} is about $(0, 1.5)$. Therefore, $k_{RC} = 1$ is selected as a compromise between dynamic performance and system stability.

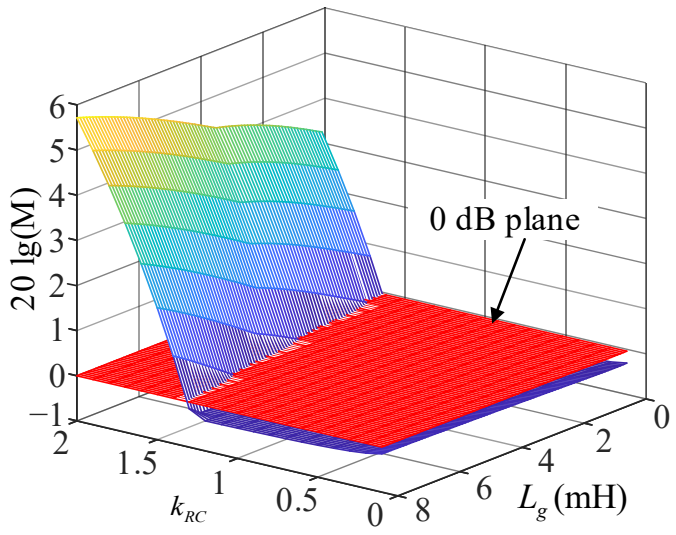


Figure 11. Amplitude of M versus 0 dB plane with different k_{RC} and L_g.

5. Experimental Verification

To substantiate the validity of the proposed scheme, a 2 kW single-phase *LCL*-type grid-tied inverter has been established in the laboratory. The experimental setup is depicted

in Figure 12. A TMS320F28335 digital signal controller (Texas Instruments, Dallas, TX, USA) is employed in the setup and the PM50RLA060 intelligent power module (Mitsubishi Electric, Tokyo, Japan) is adopted. A Chroma 62100H-1000 programmable DC power supply (Chroma ATE Inc., Taoyuan, Taiwan) provides the necessary DC bus voltage. System parameters are listed in Table 1. It is worth mentioning that a double-sampling double-load mode was employed to reduce the time delay [33]. The PI controller, RCs and PLL all update twice within a switching period.

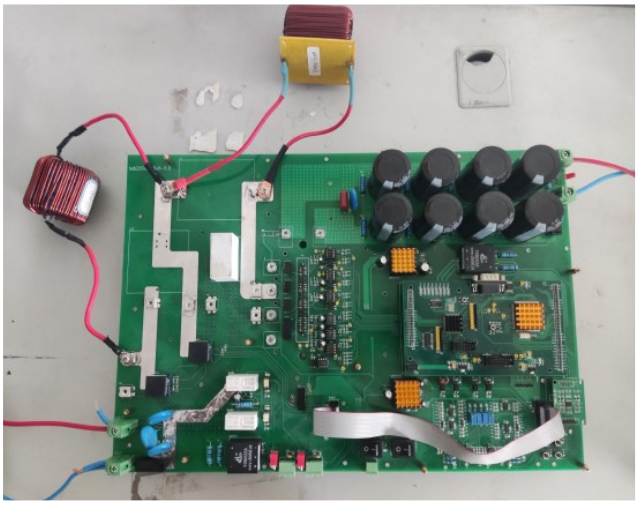
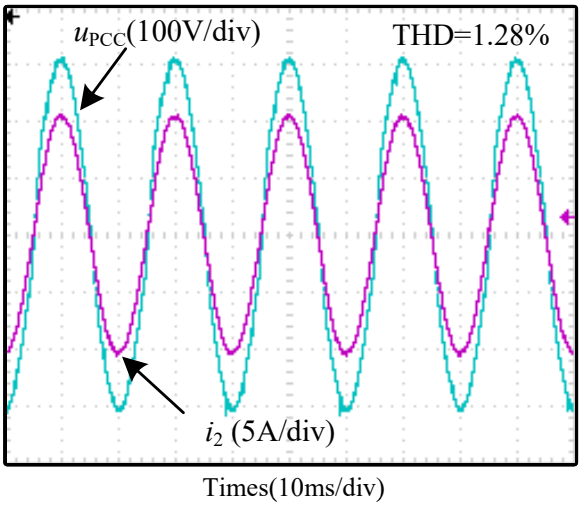


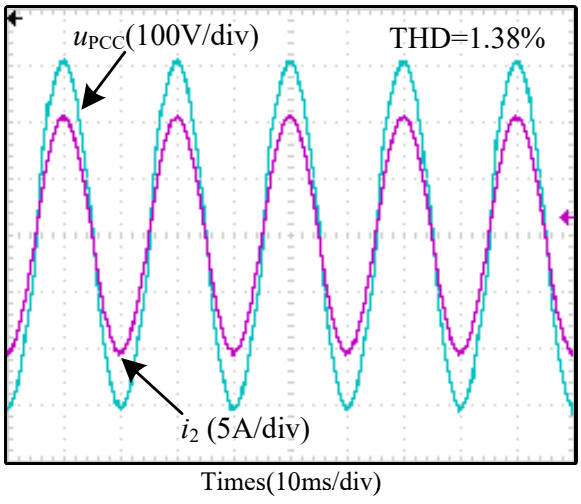
Figure 12. Grid-tied inverter hardware built for experiments.

5.1. Steady State Response

The reference current amplitude is 10 A, which is synchronized to the grid voltage via an SOGI-based PLL. When f_g is 50 Hz, the waveforms of the injected current i_2 with varying RCs are shown in Figure 13. The THD results of i_2 under CRC, CFORC and PFORC are almost identical, measuring 1.28%, 1.38% and 1.31%, respectively. The THD results under different RCs and grid frequencies are summarized in Figure 14. When f_g is set to 49.6 Hz, CRC still maintains the order of RC as N = 400, and the THD of i_2 rises to 1.77%. However, the THDs of i_2 with CFORC and PFORC are 1.42% and 1.29%, respectively. when f_g is set to 50.4 Hz, CRC achieves a THD of 3.09%, while CFORC and PFORC achieve 1.47% and 1.27%, respectively.

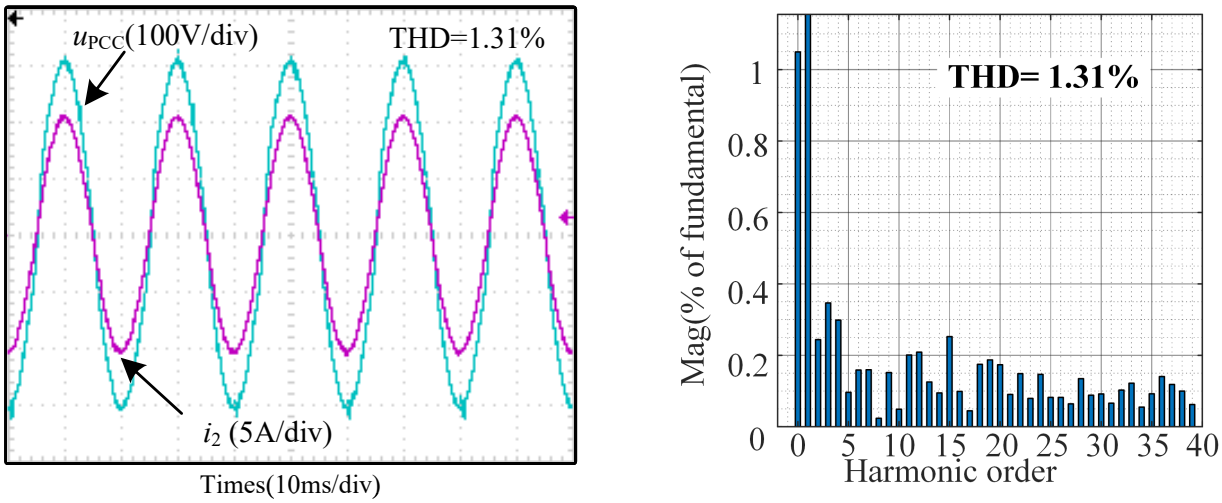


(**a**)



(**b**)

Figure 13. *Cont.*



(**c**) (**d**)

Figure 13. Experimental results (continued): (**a**) CRC, (**b**) CFORC, (**c**) PFORC, (**d**) the spectrum analysis of grid current of the proposed PFORC.

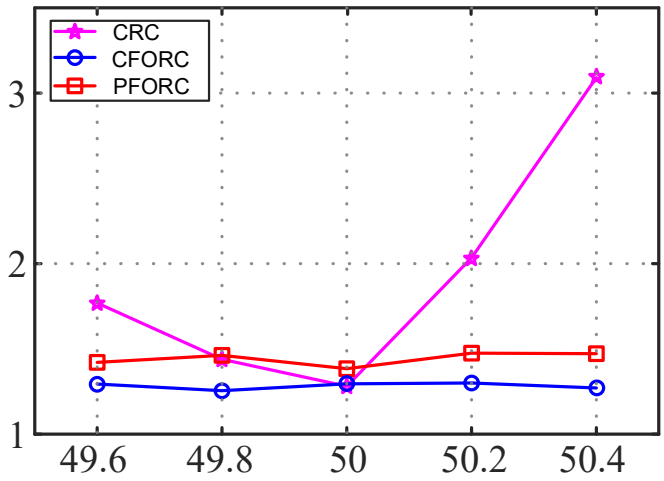
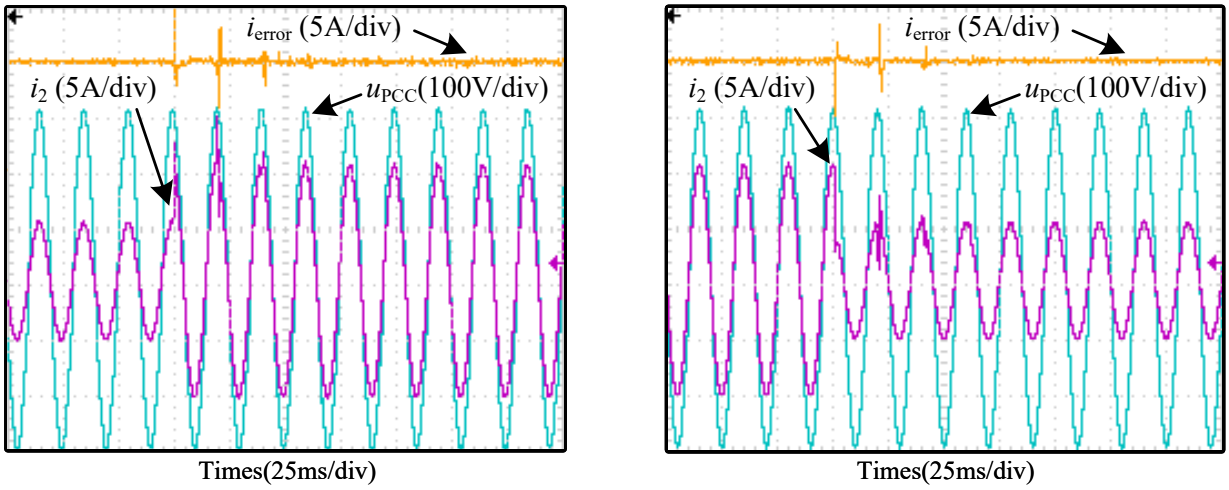


Figure 14. THD of i_2 of different schemes under grid frequency variation.

Obviously, when the grid frequency varies, the THD results of CRC deteriorate while the THD results of CFORC and PFORC remain stable thanks to their frequency adaptivity. Moreover, PFORC achieves lower THD results than CFORC, which validates PFORC's adaptivity to frequency fluctuations.

5.2. Transient Response

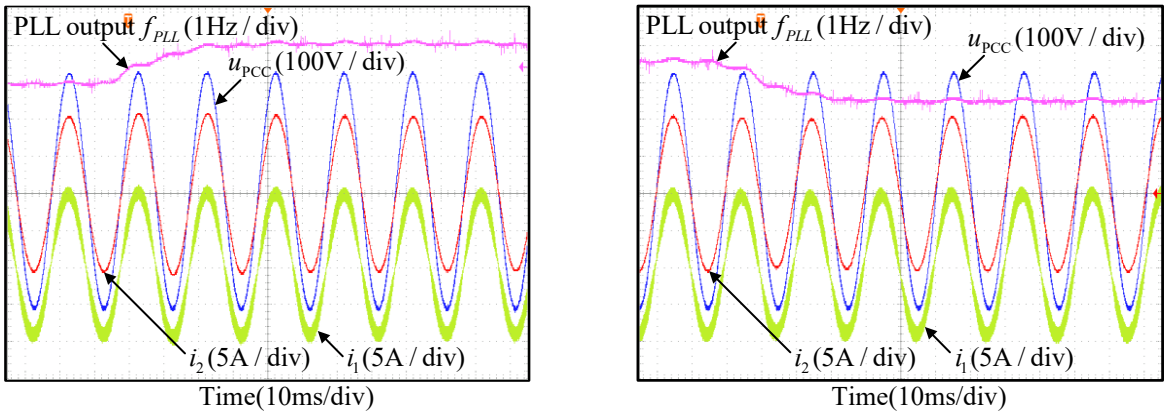
The injected current's response regarding the current amplitude step change is illustrated to test the proposed approach's transient response. Figure 15 presents the response of injected current i_2 and u_{PCC} while the reference current steps up and down at the peak of the sine wave, which corresponds to a phase angle of $\frac{\pi}{2}$. The step change in the reference current at the peak position causes glitches of i_2 starting from the same position in the following periods. However, the steady state is reached within 5 cycles. Therefore, the proposed approach can remain stable even with a step change in the reference current.



(**a**) (**b**)

Figure 15. Experimental transient waveform of reference step change. (**a**) Reference steps up. (**b**) Reference steps down.

To substantiate the adaptability of PFORC to different frequencies, a programmable power grid simulator Chroma 61512 (Chroma ATE Inc., Taoyuan, Taiwan) is employed to simulate the grid. The transient responses of the system under grid frequency step changes are shown in Figure 16. The detection of grid frequency step changes takes approximately 30 ms. With a fluctuating PLL output frequency f_{PLL}, PFORC maintains a sinusoidal injected current i_2.



(**a**) (**b**)

Figure 16. Responses to step changes in grid frequency. (**a**) From 49.5 Hz to 50.5 Hz. (**b**) From 50.5 Hz to 49.5 Hz.

The current tracking error with respect to the PLL output frequency under CRC, FORC, and PFORC control schemes is shown in Figure 17. Before f_{PLL} step change happens, PFORC has the smallest current tracking error. After the step change, the current tracking errors of PFORC rises to almost the same amplitude of FORC and CRC but soon converges after about 3 periods (0.06 s). It is concluded that during grid frequency change, the current tracking error of PFORC, FORC and CRC have almost the same amplitude. However, PFORC can achieve better tracking accuracy under steady-state conditions.

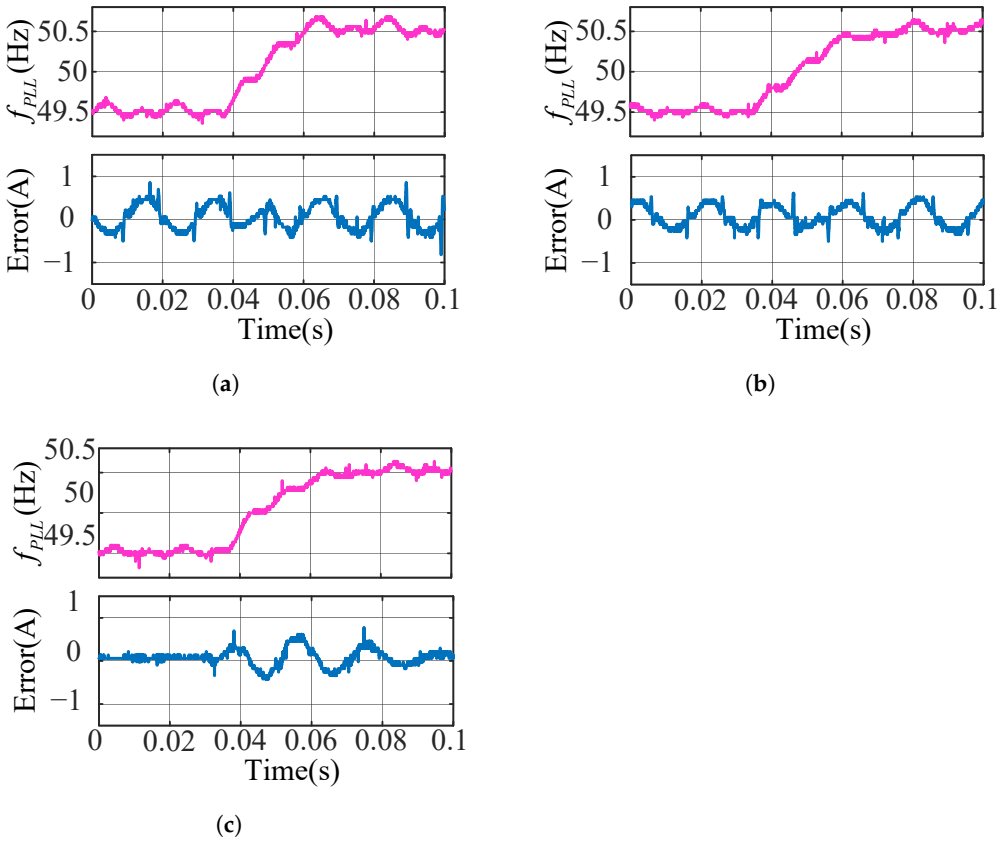
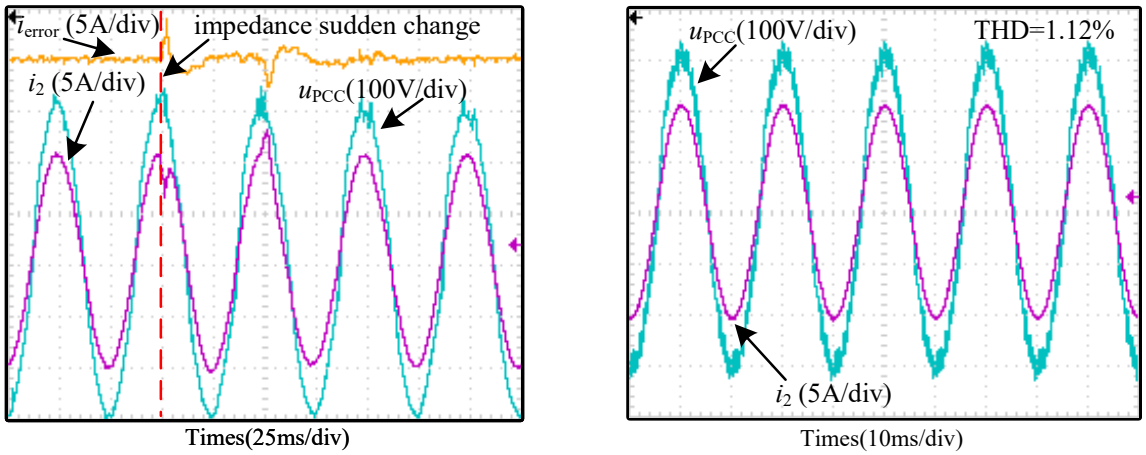


Figure 17. Current tracking error with stepping grid frequency (49.5 Hz to 50.5 Hz). (**a**) CRC. (**b**) FORC. (**c**) PFORC.

As shown in Figure 17, accurate frequency information is critical for the performance of the CRC and FORC. Frequency measurement errors can degrade the robustness of these controllers under frequency variations, thereby reducing harmonics suppression and increasing current deviations. The proposed PFORC achieves fractional delay by interpolating PLL phase-angle samples. Compared with the CRC and FORC, this approach is less sensitive to frequency estimation errors, allowing it to maintain small current deviations even under frequency fluctuations.

5.3. Robustness Experiments

The inverter works when the grid impedance sudden changes to test the robustness of the proposed scheme under the weak grid. Figure 18a shows the waveform of i_2 and u_{PCC} while the grid impedance suddenly changes to an inductor in parallel with a resistor. In this case, a 3.8 mH inductor is selected to simulate the grid inductance L_g. A resistor of 18 Ω and a breaker are in parallel with L_g. The breaker is initially closed-up, short-circuiting L_g and the resistor. The red dashed line in Figure 18a indicates the moment when the breaker is turned off, leading to the sudden change of the grid impedance. It can be seen from Figure 18a that the distortion of i_2 recovers within two periods. Thus, the proposed PFORC scheme demonstrates robust resilience to abrupt changes in grid impedance. To further validate the designed control parameters against grid inductance variation, an 8 mH inductor is used to simulate the grid inductance L_g. As Figure 18b shows, the system remains stable and the THD of i_2 is 1.12%. That is, the proposed scheme with designed system parameters performs well under grid inductance variation.



(**a**) (**b**)

Figure 18. Robustness experiments (**a**) Transient waveform of u_{PCC} and i_2 under sudden change of grid impedance. (**b**) Injected curent i_2 under PFORC with f_g = 50 Hz, L_g = 8 mH.

6. Conclusions

In this paper, a straightforward and effective PFORC based on the phase information is proposed to achieve frequency adaptation, which overcomes the problem of frequency fluctuations captured from the PLL faced by CFORC. The linear interpolation method that leverages the difference of phase angle serves to enhance the frequency adaptation capability of RC. An extra memory buffer for phase angles is needed for the practical implementation of this scheme. Insensitive to detected frequency fluctuations, PFORC demonstrates superior harmonics suppression performance at the cost of extra memory buffer usage for phase angle. Furthermore, the proposed scheme exhibits enhanced tracking accuracy in a steady state. Comparative experimental results demonstrate the proposed scheme's benefits and the robustness of the designed parameters in the face of grid inductance fluctuations.

Author Contributions: Conceptualization, Q.Z., H.D., and Y.Y.; formal analvsis, H.D.; methodology, H.D.; software, H.D.; validation, H.D.; writing—original draft, H.D.; writing—review & editing, H.D. and G.Z.; supervision, Y.Y. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: All data supporting the findings of this study are contained within the article. No additional data are available.

Conflicts of Interest: The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Appendix A

The derivation of Equation (10) proceeds as follows. First, the transfer function from the inverter output voltage u_{inv} to the inverter-side current i_1 can be expressed as

$$G_1(s) = \frac{i_1(s)}{u_{inv}(s)} = \frac{1}{L_1 + L_2} \cdot \frac{1}{s} + \frac{L_2}{L_1(L_1 + L_2)} \cdot \frac{s}{s^2 + \omega_r^2} \tag{A1}$$

The transfer function is subsequently discretized via a zero-order hold (ZOH) and can be written as

$$\begin{aligned} G_1(z) &= \frac{T_s}{(L_1+L_2)(z-1)} + \frac{L_2}{L_1(L_1+L_2)} \cdot \frac{z-1}{z^2-2z\cos(\omega_r T_s)+1} \cdot \frac{\sin(\omega_r T_s)}{\omega_r} \\ &= \frac{1}{L_1+L_2} \cdot \frac{T_s(z^2-2z\cos(\omega_r T_s)+1) + \frac{L_2}{L_1}(z-1)^2 \frac{\sin(\omega_r T_s)}{\omega_r}}{(z-1)(z^2-2z\cos(\omega_r T_s)+1)}. \end{aligned} \tag{A2}$$

There exists a small equivalent phase delay in the inverter during modulation and driving. After linearization, this delay manifests in the discrete domain as an additional term in the system denominator, proportional to $(z-1)$. This additional term can be parameterized

$$\alpha = \frac{K_d \sin(\omega_r T_s)}{\omega_r L_1} \tag{A3}$$

The delay block $M(z)$ represents the equivalent time delay in a discrete-time system caused by sampling, holding, or signal transmission. Its expression can be given by

$$M(z) = \frac{1}{K_{pwm}} \cdot \frac{z^{-1}}{1+\alpha \cdot \frac{z-1}{z}} = \frac{1}{K_{pwm}} \cdot \frac{1}{z+\alpha(z-1)}. \tag{A4}$$

Based on the above analysis and Figure 8, the discrete transfer function of the open-loop gain without G_{RC} is as follows:

$$\begin{aligned} H(z) &= G_{PI}(z)M(z)G_1(z) \\ &= \frac{G_{PI}(z)}{\omega_r(L_1+L_2)(z-1)} \times \\ &\frac{\omega_r T_s(z^2-2z\cos\omega_r T_s+1) - (z-1)^2\sin\omega_r T_s}{\left[z(z^2-2z\cos\omega_r T_s+1) + (z-1)\frac{K_d \sin\omega_r T_s}{\omega_r L_1}\right]} \end{aligned} \tag{A5}$$

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