

Article **Fractional PID Controller for Voltage-Lift Converters**

Luis M. Martinez-Patiño ¹, Francisco J. Perez-Pinal ¹, Allan Giovanni Soriano-Sánchez ², Manuel Rico-Secades ³, Carina Zarate-Orduño ⁴ and Jose-Cruz Nuñez-Perez ^{5,*}

- ¹ Tecnológico Nacional de México, Instituto Tecnológico de Celaya, Celaya 38010, Mexico; m2103034@itcelaya.edu.mx (L.M.M.-P.); francisco.perez@itcelaya.edu.mx (F.J.P.-P.)
- ² CONACYT, Instituto Tecnológico de Celaya, Celaya 38010, Mexico; allan.soriano@itcelaya.edu.mx
- ³ Escuela Politecnica de Ingenieria de Gijón, Universidad de Oviedo, 33204 Gijón, Spain; mrico@uniovi.es
- ⁴ Tecnológico Nacional de México, CRODE Celaya, Celaya 38020, Mexico; carina.zarate@crodecelaya.edu.mx
- ⁵ Instituto Politécnico Nacional, IPN-CITEDI, Av. Instituto Politécnico Nacional No. 1310, Tijuana 22435, Mexico
- * Correspondence: nunez@citedi.mx

Abstract: Voltage-lift is a widely used technique in DC–DC converters to step-up output voltage levels. Several traditional and advanced control techniques applicable to power electronic converters (PEC) have been reported and utilized for voltage-lift applications. Similarly, in recent years the implementation of fractional-order controllers (FOC) in PEC applications has gained interest, aiming to improve system performance, and has been validated in basic converter topologies. Following this trend, this work presents an FOC for a voltage-lift converter, requiring only output voltage feedback. A third-order non-minimal phase system is selected for experimentation to verify FOC implementations for more complex PEC configurations. A simple, straightforward design and approximation methodology for the FOC is proposed. Step-by-step development of the FOC, numerical and practical results on a 50 W voltage-lift converter are reported. The results show that PEC transient and steady-state responses can be enhanced using FOC controllers when compared with classical linear controllers. Extended applications of FOC for improved performance in power conversion is also discussed.

Keywords: control design; DC-DC power converters; fractional calculus; Luo converter

1. Introduction

To interconnect, in the best energy-efficient way, sources and loads from different capabilities and characteristics represent one fundamental purpose of power electronics (PE). Currently, there are elegant and remarkable solutions reported in the literature to achieve this purpose, where the application range usually varies from micro- to mega-watts, and it is foreseen that this tendency will remain over this decade. From the early days of PE, it was conceived as an interdisciplinary area combined with basic disciplines, i.e., circuits, communication, control, among others. However, in recent years PE's complexity has increased due to the appearance of new concepts such as renewable energy (RE), electrified mobility (E-mobility), Industry 4.0, digitalization, and digital twins. This paradigm shift has increased the demand for advanced solutions to satisfy these new necessities.

To provide an alternative to step-up the voltage to these new PE demands, there exist different configurations. For instance, there are non-isolated/isolated, unidirectional/bidirectional, voltage-fed/current-fed, hard switched/soft switched, non-minimum-phase, and minimum-phase PEs. In particular, there are different voltage boost techniques such as: switched capacitor, voltage multiplier, switched inductor and voltage lift, magnetic coupling, and multi-stage level. A comprehensive review on step-up DC–DC converters can be found in [1].

On the other hand, the development of controller techniques for PE is in a stage of constant development and improvement, where a recent impulse has been given to



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Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). fractional-order controllers (FOC). Therefore, this section will present a brief literature review, motivation, challenges and the main contributions of this work.

1.1. Literature Review

Over the years, considerable research has been conducted in control engineering, leading to the development of various control techniques aimed at improving system performance, stability, and robustness. Some notable control techniques adopted in the literature include proportional-integral-derivative (PID) control [2], model predictive control (MPC) [3], adaptive control [4], sliding mode control (SMC) [5], fuzzy logic control (FLC) [6], H-infinity control [7] and fractional-order control. Within this array of control techniques, FOC has emerged as a promising and innovative approach that departs from the traditional integer-order control paradigms. Although PID controls are widely adopted control techniques that use proportional, integral, and derivative actions to regulate a system by adjusting the control output based on the error, integral of error, and rate of change of error, they inherently suffer from limited adaptability to system changes and control flexibility [8]. Fractional-order control harnesses the mathematical concepts of fractional calculus to introduce non-integer-order derivatives and integrals into control system design. This novel approach offers several advantages, such as increased design flexibility, enhanced system response, and improved disturbance rejection [9].

Fractional-order controllers (FOC) have gained attention in control research for applications where precise system control is crucial due to its flexibility in adjusting the control behavior of a system. FOC has been successfully applied in various fields including power electronics (PE) [10], motor control [11], active power filters [12], process control [13], and chaos control [14]. A detailed review focused on FOC applied in power electronics was conducted in [15]. The study demonstrated that FOC offers advantages over integer-order controllers (IOC) in PE, such as robust performance, fast dynamic response, accurate tracking, quick transient responses, minimal overshoot, and low settling time for power converters.

In [16], a novel servomotor control mechanism for a permanent magnet synchronous motor system that utilizes specialized fractional-order PID (FOPID) controller together with a Bode's Ideal cutoff filtering system was proposed. The result of the application when compared with the optimized integer-order controller counterpart demonstrated better performance and improved control characteristics. In another study [17], the researchers proposed a distributed FOC compensation scheme to regulate the voltage deviation of a DC microgrid, establishing stability in the controlled system. In [18], an uncomplicated approximation procedure for FOPID was explored for a synthesizable bulk converter in regulating its output voltage. The basic configuration of this FOC and its integer-order counterparts were characterized and compared. The findings showed a fast step response in stabilizing the control parameter with an accompanying negligible steady-state error. Furthermore, in [19], an example of the application of cohort intelligence (CI) optimization technique to FOPID controllers for buck converters can be found. The obtained results were consistent with the characteristics reported in [18]. Moreover, the utilization of FOPID controllers was extended to other fundamental converter topologies such as boost [20], buck [21], and buck/boost converters [22]. However, in this manuscript, we aim to further validate the applicability of FOPID controllers by exploring their performance in more complex converter topologies.

1.2. Motivation and Challenges

Power electronic converters (PEC) are generally considered as nonlinear in their dynamics since the outputs of the systems do not exhibit linear relationships with their inputs. This nonlinear behavior can be attributed to the switching actions of the nonlinear semiconductor devices that are incorporated within the PEC systems which introduces abrupt changes in their voltage level and current flow. The nonlinearity behaviors of PEC models contribute to the complexity of controlling and stabilizing their intrinsic electronic quantities making it difficult for traditional control techniques to achieve optimal performance. Traditional control approaches for power electronic (PE) systems often require the incorporation of an additional current feedback loop to regulate and manipulate system behaviors [23]. However, this additional system can introduce more complexities to the overall system. As a result, the utilization of fractional-order controllers has gained significant attention and interest. Additionally, its feasibility to be implemented with analog or digital techniques represents another attraction. A standardized design procedure for FOC applied to PEC is yet to be clearly defined. Nevertheless, several proposals including conventional and optimization methods have been reported [24-26]. For instance, the authors in [27] proposed an improved optimization version of the well-known hunger game search optimization algorithm to appropriately tune the FOPID controller parameter for achieving optimal voltage control in the PE. Optimization techniques have shown good results in simulations and relevant performance characteristics such as smooth control signal, outstanding tracking performance and fast transient response have been demonstrated. However, some of these optimization techniques have constraints features which may be difficult to implement physically. Hence, this study focuses on exploring a simplified and direct approach for tuning fractional-order controllers in power electronic converters. The objective is to assess the performance of FOCs and encourage their application in various power electronics control systems.

1.3. Contributions

In this work, we investigate a traditional non-isolated voltage lift converter to step-up output voltage level from a low voltage input, using an FOC as a main controller. The main goal of this investigation was to experimentally compare a traditional and an FOC controller for a Luo converter, qualitatively and quantitatively. Thus, the following contributions to the state of the art are hereby highlighted:

- 1. A systematic generalized procedure to design FOC for PE is reported, which can be easily applied to fourth-order and higher-order converters.
- 2. Classical I, PID, lag-lead, sliding mode, and FOC were fully numerically implemented using an analog approach and a performance comparison was performed. It was found that FOC achieves a fast transient dynamic response, minimal overshoot, and low settling time. Certainly, the analog implementation of the 'I' and FOC controller were in harmony with the numerical simulation.
- 3. It was concluded that FOC is simple, has no hands-on difficulty, and accomplishes a higher performance compared with the other control techniques. Indeed, in the authors' opinion, FOC may become the principal PEC controller technique in the coming years.

1.4. Paper Organization

This paper is organized as follows: Section 2 presents the general considerations regarding the PEC as well as the FOC design. It includes the mathematical model, the steady-state equations and the design equations for the converter. The El-Khazali FOC method is introduced, a step-by-step process as well as a flowchart for the FOPID controller design is presented, including the electric circuit for analog implementation of the controller. In Section 3, the designed controller is presented as well as the obtained simulation and experimental results of the application of the controller in the third-order Super-lift Luo converter, and a comparison of the obtained performance with integer-order controllers is shown. A discussion about the obtained outcomes is provided in Section 4, and the most relevant conclusions are presented in Section 5.

2. Materials and Methods

In this section, the necessary preliminaries about the PEC and some of the control techniques commonly applied are presented.

2.1. Power Electronic Converter (PEC)

A notable example of the application of a voltage-lift technique is the Super-lift Luo converter series, whose elementary circuit is shown in Figure 1. It was introduced as an alternative to traditional voltage-lift techniques, in order to increase output voltage gain.

In traditional voltage-lift techniques, i.e., voltage-lift Luo converters [28], the output voltage increases with each stage in an arithmetic progression. In contrast, Super-lift Luo converters present an increase in output voltage in geometric progression, enhancing voltage gain in power series [29].



Figure 1. Elementary circuit of Super-lift Luo converter.

Super-lift Luo-converter main series consists of an elementary circuit and derived circuits constructed by adding additional stages of inductors, capacitors and diodes, i.e., Re-Lift, Triple-Lift, and higher-order lift circuits. An additional series is derived from the former, with additional voltage lifting capacities.

2.1.1. Operation

Super-lift Luo converter operation is well known [30,31] and can be briefly described as follows. When the switch Q_1 is in ON state, the diode D_1 is forward biased, causing current to flow through the inductor *L* and the capacitor C_1 , which is charged to the input voltage V_i . Output current is maintained by the discharge of the capacitor C_2 through the output load resistance *R*. Figure 2 shows an equivalent circuit of the PEC in this interval.



Figure 2. Super-lift Luo converter *t*_{on} interval.

Where i_L is the inductor current, i_{C_1} is the current through capacitor C_1 , i_{C_2} is the current through capacitor C_2 , i_0 is the output current, v_L is the inductor voltage, v_{C_1} is the capacitor C_1 voltage, and v_{C_2} is the capacitor C_2 voltage. Note that v_{C_2} is equal to the output voltage v_0 . When the switch Q_1 is turned off, diode D_1 is negative biased and D_2 is forward biased. Capacitor C_1 becomes discharged by inductor L current, thereby the current flows through both the capacitor C_1 and the inductor L to the output. Figure 3 shows the equivalent circuit of the PEC in this interval.



Figure 3. Super-lift Luo converter *t*_{off} interval.

Equations for the output capacitor voltage ripple Δv_{C_2} (1), inductor current ripple Δi_L (2), and relations between input and output voltage (3) and current (4) are presented below [29].

$$\Delta v_{C_2} = \frac{I_0}{C_2} (1 - D)T = \frac{V_{C_2}(1 - D)}{fC_2R} \tag{1}$$

$$\Delta i_L = \frac{V_i}{L} DT = \frac{V_{C_2} - 2V_i}{L} (1 - D)T$$
(2)

$$V_o = \frac{2-D}{1-D}V_i \tag{3}$$

$$I_i = \frac{2-D}{1-D}I_o \tag{4}$$

where I_i , I_o , V_i , V_o , D, V_{C_1} , V_{C_2} denote the input current, output current, input voltage, output voltage, duty cycle, capacitor C_1 voltage and capacitor C_2 voltage, at the operation point, respectively.

2.1.2. Design Equations

Solving (1) and (2) for C_2 and L, respectively, design equations for the PEC can be derived. The resulting design equations are displayed below (5) and (6).

$$L = \frac{V_i D}{\Delta i_L f} \tag{5}$$

$$C_2 = \frac{V_{C_2}(1-D)}{\Delta v_{C_2} f R}$$
(6)

To find an equation for the average duty cycle given input and output desired voltage values, (3) is solved for *D*. The resulting expression is displayed as follows (7).

$$D = \frac{V_{C_2} - 2V_i}{V_{C_2} - V_i} \tag{7}$$

2.1.3. Third-Order Model

To apply both classical linear control and FOC, it is necessary to obtain a mathematical model of the system to be controlled. In this case, a third-order model of the converter can be obtained if at least one parasitic element is supposed, specifically a series resistor for the capacitor C_1 , ESR_{C_1} . A third-order model with additional parasitic components can more accurately represent the system, as demonstrated in [31], therefore it was selected for this study. Alternatively, a second-order model can be found in Appendix A. For a full non-ideal model of the Super-lift Luo converter as well as dynamic differences to the ideal second order model, the interested reader is referred to [31].

By analyzing the circuit shown at Figure 4 using Kirchhoff's laws, assuming continuous conduction mode (CCM), the continuous averaged model can be obtained (8)–(10).

$$\frac{di_L}{dt} = -\frac{ESR_{C_1}(1-d)}{L}i_L + \frac{1-d}{L}v_{C_1} - \frac{1-d}{L}v_{C_2} + \frac{1}{L}v_i \tag{8}$$

$$\frac{dv_{C_1}}{dt} = -\frac{1-d}{C_1}i_L + \frac{d}{C_1 ESR_{C_1}}v_{C_1} + \frac{d}{C_1 ESR_{C_1}}v_i \tag{9}$$

$$\frac{dv_{C_2}}{dt} = -\frac{1-d}{C_2}i_L - \frac{1}{C_2R}v_{C_2} \tag{10}$$

where *d* stands for the averaged duty cycle. A small-signal average model with the following form (11) is created by linearizing by the small signal perturbation method around the equilibrium point $[I_L, V_{C_2}]$.

$$\frac{d}{dt}\hat{x}_{b} = A_{2}\hat{x}_{b} + B_{2}\hat{d} + C_{2}\hat{v}_{i}$$
(11)

where:

$$\hat{x}_{b} = \begin{bmatrix} \hat{i}_{L} \\ \hat{v}_{C_{1}} \\ \hat{v}_{C_{2}} \end{bmatrix}$$
(12)

$$A_{2} = \begin{bmatrix} -\frac{ESR_{C_{1}}(1-D)}{L} & \frac{(1-D)}{L} & -\frac{(1-D)}{L} \\ -\frac{(1-D)}{C_{1}} & -\frac{1}{C_{1}ESR_{C_{1}}} & 0 \\ \frac{(1-D)}{C_{2}} & 0 & -\frac{1}{C_{2}R} \end{bmatrix}$$
(13)

$$B_{2} = \begin{bmatrix} \frac{ESR_{C_{1}}}{L}I_{L} - \frac{V_{C_{1}}}{L} + \frac{V_{C_{2}}}{L} \\ \frac{1}{C_{1}}I_{L} - \frac{V_{C_{1}}}{C_{1}ESR_{C_{1}}} + \frac{V_{i}}{C_{1}ESR_{C_{1}}} \\ -\frac{I_{L}}{C_{2}} \end{bmatrix}$$
(14)
$$C_{2} = \begin{bmatrix} \frac{1}{L} \\ \frac{1}{C_{1}}ESR_{C_{1}} \\ 0 \end{bmatrix}$$
(15)

where \hat{i}_L , \hat{v}_{C_2} , \hat{d} , \hat{v}_i are the perturbation terms of i_L , v_{C_2} , d, v_i , respectively. Neglecting the perturbation terms of \hat{v}_i , the third-order model control-to-output voltage is obtained by the duty-to-output relation (16), and is shown as follows (17).

$$\frac{\hat{x}_b(s)}{\hat{d}(s)} = (sI - A_2)^{-1} B_2 = \begin{bmatrix} \hat{i}_L(s) & \hat{v}_{C_1}(s) & \hat{v}_{C_2}(s) \\ \hat{d}(s) & \hat{d}(s) & \hat{d}(s) \end{bmatrix}^T$$
(16)

$$\frac{\hat{x}_{b_2}(s)}{\hat{d}(s)} = \frac{\hat{v}_{C_2}(s)}{\hat{d}(s)} = \frac{\gamma_2 s^2 + \gamma_1 s + \gamma_0}{\delta_3 s^3 + \delta_2 s^2 + \delta_1 s + \delta_0}$$
(17)

where the coefficients γ_n and δ_n are shown in Table 1.



Figure 4. Super-lift Luo converter with one parasitic element.

	Table	1.	Coefficients	for	(17))
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Symbol	Value
γ_2	$RC_1 LESR_{C_1}$
γ_1	$R\{[(C_1 V_{C_2} - C_1 V_{C_1}) ESR_{C_1} + L I_L]d + (C_1 v_{C_1} - C_1 V_{C_2}) ESR_{C_1}\}$
γ_0	$R[(V_{C_2} - V_i)D^2 + (2V_i - (V_{C_2} + V_{C_1}))D + (V_{C_1} - V_i)]$
δ_3	$C_1C_2 L ESR_{C_1}R$
δ_2	$(C_1 C_2 ESR_{C_1}^2 + C_2 L) R D + (C_1 L ESR_{C_1} - C_1 C_2 ESR_{C_1}^2 R)$
δ_1	$(2C_2 + C_1)ESR RD^2 + (C_1 ESR_{C_1}^2 + L - (3C_2 + 2C_1)ESR_{C_1} R)D + ((C_2 + C_1)ESR_{C_1} R - C_1 ESR_{C_1}^2)$
δ_0	$R D^{3} + (2ESR_{C_{1}} - 2R) D^{2} + (R - 3ESR_{C_{1}}) D + ESR_{C_{1}}$

2.2. Control Techniques for Power Converters

As reported in the literature, several control strategies have been proposed and successfully applied to regulate PEC. Classical linear control, including lag-lead compensators and PID controllers are extensively used in PE applications due to a simple design and implementation process [32], but are only effective around an operating point and that the performance is influenced by a variety of factors, including parameter variations, non-linearities, and bandwidth restrictions [33]. Additionally, for non-minimal phase systems, a popular solution is to use a minimal-phase variable control, hence, a current loop is introduced. Output voltage is then achieved by using voltage loop [34,35], achieving stability and better performance at the cost of additional circuitry and current sensors. Thus, some strategies are being researched to avoid this approach [36].

Sliding mode control (SMC) is a nonlinear control strategy applicable to both linear and nonlinear systems, and has been extensively used in PECs [37]. A fast finite-time response and robustness against parameter variations are the most notable features of SMC. However, one of the main drawbacks of the technique is its variable switching frequency, leading to electromagnetic interference (EMI) filtering design problems as well as degradation in performance and switching losses [33]. Some solutions proposed in the literature show good results at the cost of regulation performance or requiring a costly, non-trivial implementation that might not be suitable for overall DC/DC converter applications [38–40].

Model Predictive Control (MPC) is applied in PEC due to its advantages over other control techniques, such as adaptability, fast response and tolerance of parameter variations [37,41]. This method's performance can be impacted by control loop delays, and model inaccuracies. MPC requires an accurate mathematical model of the process to predict, and demands more processing resources than other methods [33,42].

Intelligent control techniques such as fuzzy control and neural networks present key advantages, including immunity to parameter variations and noise, adaptability to operation conditions and non-linearities and do not require a complex model of the process [33,37]. However, these techniques tend to be computationally demanding and require expert knowledge for their design [43].

Fractional-Order PID Controller

In this work, FOC is selected as the control technique for this third-order PEC, due to its capacity for regulating non-linear systems being a linear control technique, and the advantages commonly attributed to FOCs, like robustness against parameter and gain variations, reduced levels of noise and straightforward implementation with fractal arrangements of electronic devices [21,44]. In this work, the purpose of using this technique is achieving an acceptable response using only one control loop, thus, avoiding the use of extra elements for current sensing and current control loop.

The FOPID controller is a generalization of the integer-order PID controller. A FOPID controller can be represented as follows (18) [15].

$$C(s) = K_p + K_i s^{-\alpha} + K_d s^{\beta}$$
⁽¹⁸⁾

where α and β are the non-integer orders of the integrator and differentiator [15], and K_p, K_i, K_d are the proportional, integral and derivative gains, respectively. These fractional orders give more flexibility when adjusting the controller gain and phase characteristics, acting as additional "tuning knobs", and thus, providing a more precise response.

Several tuning methods for the FOPID controller have been proposed in the literature, including conventional and optimal tuning [24–26]. In this work, the El-Khazali method is used. For insights into the use of optimization methods with restrictions to achieve implementable results, interested readers are referred to [45].

2.3. Approximation of the Fractional-Order Operator

Commonly, the solution of fractional-order equations via analytical or numerical methods is not simple or computationally demanding, and the software tools used to simulate control systems are usually designed to work with integer orders of s [46]. Moreover, fractional-order transfer functions contain irrational terms, resulting in infinite-dimensional filters [15]. For analog implementation of controllers, electronic components such as resistors, capacitors, and inductors are frequently employed. It is not clear and difficult to implement fractional-order controllers directly using these elements [46,47].

Numerous integer-order approximations for the fractional-order operator have been proposed in the literature. The El-Khazali method, the Continued Fraction Expansion (CFE) method, the Matsuda method, the Outstaloup method and the Carlson method are some of the commonly used approximation techniques [15]. Each approximation technique has unique qualities that might make it better suited for a specific application. Readers who are interested in a comparison of these approximation techniques are directed to [48].

2.4. FOPID Controller Design Procedure

In this section, the procedure used to design the FOPID controller is presented, as well as the necessary adaptation to use it with non-minimal phase systems. For practical implementation, schematic circuit diagrams are shown.

2.4.1. El-Khazali Method

El-Khazali proposed a simple method to approximate the fractional-order Laplacian operator s^{α} , and tuning the fractional-order controller [26]. Demonstration of this method's effectiveness can be found at [20–22,49]. The method can be summarized in the following steps [21,49].

- 1. Model the desired system.
- 2. Determine the uncontrolled plant phase contribution φ_p , as well as the desired phase margin of the controlled plant φ_{md} .

3. Compute the controller contribution φ_c as follows (19) [21,49].

$$\varphi_c = \varphi_{md} - \varphi_p - \pi \tag{19}$$

4. For the desired phase margin of the controlled plant, compute α , the required fractional order (20) [21,49].

а

$$\alpha = \frac{\varphi_{md} - \varphi_p - \pi}{\pi/2} \tag{20}$$

5. Compute s^{α} using (21) [21,49].

$$s^{\alpha} \approx \frac{a_0 s^2 + a_1 s + a_2}{a_2 s^2 + a_1 s + a_0} \tag{21}$$

where

$$_{0} = \alpha^{2} + 3\alpha + 2 \tag{22}$$

$$a_1 = 6\alpha \tan\frac{(2-\alpha)\pi}{4} \tag{23}$$

$$a_2 = \alpha^2 - 3\alpha + 2 \tag{24}$$

6. Determine the controller structure $G_c(s)$ (25) [21,49].

$$G_c(s) = k_p \left(1 + \frac{1}{T_i s^{\alpha}} + T_d s^{\mu} \right)$$
(25)

where k_p is the proportional gain, T_i and T_d are the integral and derivative time constants, respectively. Considering $\alpha = \mu$, expression (25) can be rewritten as (26):

$$G_c(s) = \frac{K_c (T_i s^{\alpha} + 1)^2}{s^{\alpha}}$$
(26)

where T_i and K_c can be initially approximated with the following expressions (27) and (28) [21,49]:

$$T_{i} = \frac{\tan(\frac{\varphi_{c}}{2}) + \tan(\frac{2+\mu}{\pi/4})}{\tan(\frac{\varphi_{c}}{2}) - \tan(\frac{2+\mu}{\pi/4})}; \quad \varphi_{c} \neq \frac{2+\mu}{\pi/8}$$
(27)

$$K_c = \frac{\frac{g_m}{g_p} [(a_0 - a_2)^2 + a_1^2]}{(a_0 - a_2)^2 (1 - T_i)^2 + a_1^2 (1 + T_i)^2}; g_p \neq \infty$$
(28)

where g_m is the desired gain margin, and g_p corresponds to the gain margin. Note that in case that g_p is not defined, the relation g_m/g_p can be substituted for a number, i.e., 1, and start tuning the variable k_c to obtain an acceptable response [26]. Tune *T* and *k* to obtain the desired effect from the proposed controller

7. Tune T_i and k_c to obtain the desired effect from the proposed controller.

2.4.2. Non-Minimal Phase Adaptation

In order to accomplish the control objective without the need for cascaded controllers, a modification of El-Khazali's approach for non-minimal phase systems was proposed in [20]. For a non-minimal phase system of the form shown in (29).

$$tf(s) = \frac{-as+b}{cs^2+ds+e}$$
(29)

where *a*, *b*, and *c*, *d*, *e* correspond to the coefficients of the numerator and denominator, respectively. The transfer function can be divided in two elements: Its minimal and non-minimal parts, respectively, as follows (30), (31) [20].

$$t_f(s) = (t_{f_m}(s)) (t_{f_{nm}}(s))$$
(30)

$$t_f(s) = \left(\frac{a(\frac{b}{a}+s)}{cs^2+ds+e}\right) \left(\frac{\frac{b}{a}-s}{\frac{b}{a}+s}\right)$$
(31)

where $t_{f_m}(s)$ and $t_{f_{nm}}(s)$ denote the minimal phase and non-minimal phase parts of the system, respectively. Note that the non-minimal phase part corresponds to the Padé approximation of the delay [20]. Working with the minimal phase part of the system allows El-Khazali's design method to be applied without additional controllers, as the condition $\alpha < 1$ is now fulfilled. Figure 5 presents a flowchart illustrating the overall process of FOC design.



Figure 5. FOC design methodology. PFE = Partial Fraction Expansion.

2.4.3. Analog Implementation

Several analog implementations for fractional-order controllers have been proposed in the literature [50,51]. In this work, an implementation design using capacitors, resistors and operational amplifiers was chosen due to its simplicity and proven efficacy for controlling PECs [20,49]. In this approach, the resulting non-integer order approximation (26) is represented in its partial fraction expansion as follows (32).

$$G_f(s) = K_1\left(\frac{1}{\psi_1 s + 1}\right) + K_2\left(\frac{1}{\psi_2 s + 1}\right) + K_3\left(\frac{1}{\psi_3 s + 1}\right) + K_4\left(\frac{1}{\psi_4 s + 1}\right) + K_5$$
(32)

where the terms $1/(\psi_n s + 1)$ correspond to a first-order system transfer function and ψ_n represents the time constant of each of these systems. This partial fraction expansion can be practically implemented via an RC circuit, as shown in Figure 6.



Figure 6. FOPID controller implementation circuit.

Where the component values of R_n , R_{in} , R_{fn} , R and C_n correspond to the resulting firstorder systems of (32). Component relations for the proposed controller are given in Section 4. Similarly, the arrangement illustrated in Figure 7 can be used to implement an "I" controller, where the R_{a2}/R_{a1} inverting Op-Amp configuration corresponds to the *Ki* constant, and the *Ci*, *Ri* integrator Op-Amp array corresponds to the 1/*s* integration operator.



Figure 7. 'I' controller implementation circuit.

3. Results

3.1. Implementation

In this section, the results of the design for the PEC and the FOPID controller are described, together with information on the electronic components used for the PEC and the FOPID controller's practical implementation.

3.1.1. PEC Design and Implementation

For the design of the PEC, continuous conduction mode (CCM) is proposed. For instance, the following parameters were considered: input voltage = 19 V, output voltage = 48 V, maximum converter power output = 50 W, proposed switching frequency = 45 kHz, maximum inductor current ripple $\Delta I_L = 40\%$ of I_L , maximum output voltage ripple $\Delta V_{C_2} = 1\%$ of V_{C_2} . Thus, from (5) and (6), elements can be calculated as follows. $L = 228.93 \mu$ H, $C_1 = C_2 = 33 \mu$ F. It was desired to achieve a robust converter able to withstand any possible overvoltage/overcurrent during experimentation. Thus, component selection reflects this design choice.

For the single inductor of the converter, a fixed inductor from Würth Elektronik was selected (part No. 74437529203221), with 220 μ H, a 4.1 A 10% saturation current and a 8.8 A maximum rated current, and typical series resistance of 36.45 m Ω . For the capacitor C_1 , a polypropylene metallized film capacitor from Kemet was selected (part No. C4AQCBW5400A3LJ), with 40 μ F capacitance at 5% tolerance, a maximum voltage rating of 650V, and a negligible ESR of 2.8 m Ω . For the capacitor C_2 , the part selected was an aluminum polymer capacitor from Cornell Dubilier (part No. 476AVG100MGBJ). with 47 μ F capacitance at 20% tolerance, and a ESR of 38 m Ω , this capacitor is able to handle up to 100 V. The selected switch is a IRF540NPBF MOSFET from Infineon Technologies, which can handle a maximum of 100 V and 33 A drain current, with an ON state resistance of 44 m Ω . The diodes selected were MUR820G from On Semiconductor, with a current capability of 8 A and a forward voltage of 975 mV.

3.1.2. FOPID Controller Design and Implementation

For the design of the FOC, the process shown in Section 2.4 is used, substituting the component values of the PEC as well as the parameter of desired phase margin. Numeric results were computed using MATLAB[®]. Following El-Khazali's FOPID design method, the first step consisted of modeling the system to be controlled. With the PEC parameters defined, a mathematical model can be obtained by substituting the selected PEC component values in (17) as follows (33).

$$G_{p_c}(s) = \frac{\hat{v}_{C_2}(s)}{\hat{d}(s)} = \frac{-3.384 \times 10^4 s^2 - 1.024 \times 10^{11} s + 5.664 \times 10^{15}}{s^3 + 3.082 \times 10^6 s^2 + 1.487 \times 10^9 s + 1.278 \times 10^{14}}$$
(33)

Using the non-minimal phase system adaptation for the procedure, (33) can be represented in the form (30). The minimal phase part is shown as follows (34).

$$G_{p_m}(s) = \frac{33.843 \times 10^3 (s + 54.317 \times 10^3) (s + 3.082 \times 10^6)}{s^3 + 3.082 \times 10^6 s^2 + 1.487 \times 10^9 s + 1.278 \times 10^{14}}$$
(34)

In a similar way, the non-minimal phase part is shown as follows (35).

$$G_{p_{nm}}(s) = \frac{54.317 \times 10^3 - s}{54.317 \times 10^3 + s}$$
(35)

To determine the required phase contribution, initially, a phase margin of at least 55° was proposed to ensure system stability before performance. The next step was computing alpha using (20), $\alpha = 0.1281$, which represents the required phase contribution of 11.53° to reach the desired phase margin. Then, s^{α} results as follows (36):

$$s^{\alpha} \approx \frac{3.153s^2 + 6.106 \times 10^5 s + 1.533 \times 10^{10}}{2.384s^2 + 6.106 \times 10^5 s + 2.028 \times 10^{10}}$$
(36)

Figure 8 shows the Bode plot of the biquadratic approximation of s^{α} .



Figure 8. Bode plot of s^{α} approximation.

The next step was to substitute (36) in the controller structure proposed by El-Khazali (26), obtaining the constants T_i and K_c with (27) and (28), respectively, and fine-tuning the parameters to obtain an implementable controller. Then, extensive testing of the resulting controller in simulation was performed to ensure it achieved an acceptable response with the desired system. Following this procedure, a working FOPID controller was found using the constants $K_c = 1.268$, $T_i = -1.845$. Note that even with a negative T_i constant, the resultant approximation is implementable since the negative sign is canceled by the structure of (26). As an alternative, a similar FOPID approximation can be obtained with $Wcf = 3.208 \times 10^4$, $\alpha = 0.5556$, $T_i = 8$, $K_c = 0.0073$. FOPID approximations for the controller $G_c(s)$ and the alternative $G_{ca}(s)$ are illustrated in Figure 9.



Figure 9. Bode plot of FOPID approximation.

Thus, the resulting FOPID approximation $G_c(s)$ obtained from the substitution of (36) in (26), using the obtained K_c and T_i constants is shown as follows (37), where, for a better presentation, the coefficients of the transfer function are given in Table 2.

$$G_c(s) = \frac{\kappa_4 s^4 + \kappa_3 s^3 + \kappa_2 s^2 + \kappa_1 s + \kappa_0}{\nu_4 s^4 + \nu_3 s^3 + \nu_2 s^2 + \nu_1 s + \nu_0}$$
(37)

Table 2. Coefficients for the FOPID Controller.

Parameter	Value
	1.989
<i>к</i> ₃	$5.977 imes 10^{5}$
κ2	$5.419 imes10^{10}$
κ_1	$1.395 imes10^{15}$
κ_0	$1.083 imes 10^{19}$
ν_4	1
ν_3	$4.498 imes 10^5$
ν_2	$6.297 imes10^{10}$
$ u_1$	$2.893 imes 10^{15}$
ν0	$4.136 imes 10^{19}$

Table 3 shows the component relations resulting from the partial fraction expansion (32).

The controller obtained an open-loop phase margin larger than the desired value of 55 degrees, as shown in Figure 10. Its proper functionality was confirmed by PSIM simulation. For the practical controllers, surface-mount technology (SMT) X7R capacitors and metal electrode leadless face (MELF) precision resistors were used to ensure a good approximation of the FOPID transfer function.

Relation	Value
R_1C_1	$4.578207 imes 10^{-6}$
R_2C_2	$2.537802 imes 10^{-5}$
R_3C_3	$6.117183 imes 10^{-6}$
R_4C_4	$3.401845 imes 10^{-5}$
R_{f1}/R_{i1}	1.441530
R_{f2}/R_{i2}	0.940274
R_{f3}/R_{i3}	0.262989
R_{f4}/R_{i4}	0.394079
R_{f5}/R_{i5}	1.989



Table 3. Component relations.

Figure 10. Open loop Bode plot of the minimal phase part of the system.

3.2. Numerical Simulation Results

PSIM simulation was used to compare the response obtained with the FOPID controller with other commonly used controllers. Simulation conditions are as follows: The selected solver was Fixed Step, with a simulation step time of 1×10^{-7} s, starting with a step response of the system at 0.0 s. Then, a -50% load variation is introduced at 0.06 s, and a +50% load variation is introduced at 0.08 s. 'I', 'PID' and Lag-Lead controllers were designed using MATLAB[®], control system designer. Figure 11a shows the complete PSIM simulation results for the output voltage.

Figure 11b shows the detailed initial step response of the PEC. The fastest response times were achieved by FOPID and sliding mode control, with 0.658 ms and 0.621 ms, respectively, while the other techniques settling times were all above 3 ms. FOPID controller overshoot was substantially larger than that of the other techniques, with 20.954% overshoot. The results are summarized at Table 4.



Figure 11. PSIM simulation of the Super-lift Luo converter. (**a**) Complete simulation results, (**b**) close up on step response.

Table	4.	Step	test	results.
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	Controller Type	Rising Time (ms)	Settling Time (ms)	Overshoot (%)	Steady State e. (%)
ч	Ι	21.7	33.5	0.0996	0.0756
tioı	PID	2.2	3.8	0.1771	0.005
лla†	Lag-Lead	1.2	3.4	0.178	0.2059
Ш	Sliding	0.202	0.621	4.679	0.1656
Z:	FOPID	0.191	0.658	20.954	0.0357
ac.	Ι	22.8	31.5	0.717	0.2538
Pre	FOPID	1.9	2.7	2.306	0.0941

Figure 12a,b show the response to a load variation, from 50 to 100% and from 100 to 50%, respectively. In this test, FOPID and Lag-Lead compensators exhibited the best performance, with a settling time at (2% criteria) of 0 ms, as the drop in voltage never surpasses this margin. The results are summarized in Table 5.



Figure 12. PSIM simulation, load variation response. (a) from 50 to 100%, (b) from 100 to 50%.

	Controller Type	Settling Time (ms)	Voltage Drop (%)
c	Ι	1.3	3.631
tion	PID	0.6	2.917
ulai	Lag-Lead	0	1.527
ш	Sliding	0.377	4.276
Si	FOPIĎ	0	1.667
2 2	Ι	2.6	4.474
Prê	FOPID	0	1.475

Table 5. Load variation test results.

3.3. Dynamic Experimental Results

For practical experimentation, the following equipment was used: A KETSIGHT DSOX1102A with voltage and current probes to measure the signals of the PEC. A BK PRECISION S129B, DC power supply for the control circuit as well as a GW INSTEC GPE-3323 DC power supply for the PEC, equipment available at Instituto Tecnologico de Celaya, Celaya, Mexico. The study was conducted on the implemented PEC, with component number parts specified in Section 3.1.1. Figure 13a shows the block diagram of the test set-up. Figure 13b shows the designed practical set-up. It consists of the oscilloscope, main power supply, controller power supply, load resistor, an input current probe, the Super-lift boost converter, the proposed FOC, an integral compensator for comparison, and a common base plate for both controllers. The mutual section is used to interchange both controllers, and consists of the sensor voltage divider, a voltage follower to increase the input impedance from the voltage feedback, the adding point between reference and feedback, a TL 494 PWM circuit, and bypass and decoupling capacitors. The overall efficiency at steady state of the designed converter is 91%.



Figure 13. Test setup for the Super-Lift Luo converter. (a) Practical set-up block diagram, (b) Practical set-up.

Figure 14a shows the FC's output voltage step response during turn-on. It can be noticed that the converter's output voltage starts from the input voltage due to the converter configuration. Furthermore, it can be seen that FOC's reaction is extremely fast, reaching the desired output voltage in less than two milliseconds with negligible overshoot. However, from Figure 14a an interesting response can be seen in the output current (green). Before turning on the converter, a constant current is drawn, because the load is connected to the converter the entire time. Once the system is active, during the transient time, the current reaches the maximum level allowed by the source; after that, the current has a small oscillation, reaching the steady-state value. This behavior is due to the fact that in the

proposed FOC only the voltage is controlled, and the current behaves without constraints. On the other hand, Figure 14b shows the integral's output voltage step response during turn-on (yellow). Contrary to FOC, the response is slow, reaching the steady state nearly twelve-times greater than FOC. Additionally, it can be seen that the current's reaction is also decelerated and smooth (green), arriving at the steady state in 33 milliseconds. Result of the step test for simulation and practical implementation are summarized in Table 4.



Figure 14. Step response for the Super-Lift Luo converter. (a) FOPID controller, (b) 'I' controller.

To evaluate both controller's performance during load changes; they were tested with a load variation from 50 to 100%, Figure 15a,b, respectively. It is necessary to mention that both controllers have a good transient response. However, once again the FOC controller achieves the best response achieving an almost insignificant setting time and voltage drop, less than 5%. Table 5 summarizes the results of the load variation test, which involved a load change from 50 to 100%.



Figure 15. Load variation response, from 50 to 100% load, for the Super-lift Luo converter. (**a**) FOPID controller, (**b**) 'I' controller.

3.4. Frequency Analysis Experimental Results

The experimental measurement of the frequency response for the FOPID controller and the PEC was obtained, in order to corroborate the controller design and implementation. The device used was the AP Instruments Model 310 Analog Frequency Response Analyzer.

Figure 16a,b show the result of the frequency response experimental analysis for the PEC and the FOPID controller, respectively. In these screenshots, both the magnitude (blue) and phase (red) response can be observed. In Figure 16b, it can be noticed that the controller approximation contribution is around 10 kHz, as expected from the approximation shown in Figure 8. The PEC response corresponds to the non-minimal phase model (33), as it was obtained from the physical converter.



(b)

Figure 16. Frequency response analysis screenshots (a) PEC, (b) FOPID controller.

4. Discussion

To achieve high-performance power electronic interfaces at different power levels represents a mandatory requirement in the development of sustainable solutions. As a possible alternative to achieve this goal, in this work the authors have proposed the combination of a third-order DC–DC converter and a fractional-order controller. The main highlights of this study can be summarized as follows:

- A simple, straightforward design process for the FOC as well as its analog implementation was validated for its application in PECs of higher complexity than the basic configurations previously reported. Specifically, the Super-lift Luo converter was selected for this study.
- FOC demonstrated superior performance in the studied PEC application, exhibiting an extremely fast reaction time, reaching the desired output voltage in less than two milliseconds, which is faster than the integer-order controllers. Negligible overshoot was also observed when using FOC.
- The load variation simulation test showed a similarly fast response between the non-linear SMC technique and the FOC, with the latter using only one feedback loop against the two of the SMC. Both FOC and integral controllers exhibited good transient response in the experimental load variation tests. However, FOC again outperformed the integer-order controller, showing an almost insignificant settling time and minimal voltage drop, less than 1.5%, against the 4.47% of the integral controller.
- The analog implementation of the FOC was validated by an experimental frequency analysis, confirming the expected controller contribution around 10 kHz.
- The obtained results showed an overall advantage for the use of FOC in PEC applications. Faster transient responses and a successful voltage regulation were observed.

Initially, a third-order model of the super-lift Luo converter is presented by considering only one parasitic in the lift capacitor. After that, a traditional small-signal average model is obtained, which is used to design the traditional and FOC converter. To design the FOC a variant of the well-known El-Khazali method is proposed, and a systematic procedure is provided so the FOC tuning can be adapted to some other high-order PEC. An advantage of the proposed FOC design, it is that it does not use any optimization method to find the parameters utilized. Please note that traditional Bode frequency response is used to design classical controllers (magnitude and phase). On the other hand, numerical results were reported using PSIM software for different controllers such as: integral, PID, sliding modes, and FOC. Finally, practical analog implementations by using operational amplifiers were reported. It is necessary to mention that digital implementation can also be realized, for more details, the interested reader is referred to [52].

As discussed in the previous section, the current study found that the FOC response is extremely fast, during start-up and load changes, compared with other controllers. Mainly, this response is due to the high gain in the FOC's structure and that no current limit is provided. This response is desired in applications such as data centers, distributed energy, traction, to name a few. However, in the authors' opinion, before FOC can be extended to other applications, some concerns arise that must be satisfied, which were observed during the implementation stage, including:

- Theoretical parameters achieved in the FOC's design must consider practical and feasible parameters to be utilized on the implementation stage. It was found that theoretical gains in the FOC's design are not always realistic.
- Care must be taken on power, ground, and signal routing in the PCB design. This
 is to reduce problems related with power integrity, signal integrity, electromagnetic
 interference (EMI), and electromagnetic compatibility (EMC).
- Analog implementation of FOC requires high-performance devices, i.e., instrumentation operational amplifiers (high bandwidth), precision resistors, and capacitors with +/- 1% tolerance. Inadvertence of this concern generates a significant discrepancy between theoretical and practical results.
- Although FOC's response is extremely fast because no current limit is considered in the design stage, two undesired behaviors were observed: (i) The source's current protection was reached during start-up and load changes. Therefore, a decrease in the overall gain of the FOPID controller was needed in the practical implementation, and (ii) the PEC's components almost reached their maximum working operation point. A possible research direction is to use the well-known cascaded structure. However, it seems that extension of classical decoupling is not straightforward (voltage loop = slow response, current loop = fast response), because if both loops use FOC they will have a fast response. Some insights in this research direction are reported in [53,54].

5. Conclusions

In this work, the application of an FOC for voltage regulation of a third-order, nonminimal phase Super-lift Luo PEC was investigated. A simple, straightforward design method based on frequency response for the FOC was selected and validated for PEC of higher order. The reported numerical and practical experiments confirmed that FOC has an extraordinary dynamic voltage response during start-up and load changes when compared with classical controllers, achieving settling times up to ten-times faster compared with the integral controller, and only 6% slower than the non-linear SMC technique, which requires an additional current feedback loop. It was also observed to exhibit 67% reduced voltage variations during load changes when compared to the integral controller. This performance is only limited by the maximum allowable current from source and practical devices.

This study has positively shown that by using FOC, implemented on analog operational amplifiers, it is possible to regulate the output voltage by using one single voltage feedback, despite the controlled converter exhibiting a non-minimal behavior.

For future work, the most significant findings to emerge from this study are that theoretical parameters must consider practical and feasible parameters utilized on the implementation stage, and a cascaded structure would be required if the converter's current exceeds the device's and source's limits. In the authors' opinion, these results add to the rapidly expanding field of fractional-order controllers in power electronic converters, and it is foreseen that this research area will increase in the coming years expanding FOC to renewable energy, E-mobility, Industry 4.0, digitalization, and digital twins.

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Appendix A. Second-Order Model

Assuming ideal components and continuous conduction mode (CCM), a secondorder model can be obtained analyzing the elemenrary Super-lift Luo converter circuit using Kirchoff's laws, with the assumption that capacitor C_1 charges at input voltage v_i . The continuous averaged model is shown as follows.

$$\frac{di_L}{dt} = -\frac{(1-d)}{L}v_{C_2} + \frac{2-d}{L}v_i$$
(A1)

$$\frac{dv_{C_2}}{dt} = -\frac{(1-d)}{C_2}i_L + \frac{1}{C_2R}v_{C_2}$$
(A2)

where *d* stands for the averaged duty cycle. Linearization is then realized by the small signal perturbation method. The small-signal average model of the Super-lift Luo converter around the equilibrium point $[I_L, V_{C_2}]$, is shown as follows.

$$\frac{d}{dt}\hat{x}_a = A\hat{x}_a + B\hat{d} + C\hat{v}_i \tag{A3}$$

where

$$\hat{x}_a = \begin{bmatrix} \hat{i}_L \\ \hat{v}_{C_2} \end{bmatrix} \tag{A4}$$

$$A = \begin{bmatrix} 0 & -\frac{(1-D)}{L} \\ \frac{1-D}{C_2} & -\frac{1}{C_2 R} \end{bmatrix}$$
(A5)

$$B = \begin{bmatrix} \frac{V_{C_2} - V_i}{L} \\ -\frac{I_L}{C_2} \end{bmatrix}$$
(A6)

where \hat{i}_L , \hat{v}_{C_2} , \hat{d} , \hat{v}_i are the perturbation terms of i_L , v_{C_2} , d, v_i , respectively. Neglecting the perturbation terms of \hat{v}_i , the control-to-output transfer functions are given by the relation shown in (A8).

$$\frac{\hat{x}_{a}(s)}{\hat{d}(s)} = (sI - A)^{-1}B = \begin{bmatrix} \hat{i}_{L}(s) & \frac{\hat{v}_{C_{2}}(s)}{\hat{d}(s)} \end{bmatrix}^{T}$$
(A8)

The second-order model control-to-output voltage is of the form shown as follows.

$$\frac{\hat{x}_{a_1}(s)}{\hat{d}(s)} = \frac{\hat{v}_{C_2}(s)}{\hat{d}(s)} = \frac{\epsilon_1 s + \epsilon_0}{\iota_2 s^2 + \iota_1 s + \iota_0}$$
(A9)

were ϵ_n and ι_n coefficients are shown at Table A1.

Table A1. Coefficients for (A9).

Symbol	Value	
ϵ_1	$-R L I_L$	
ϵ_0	$(V_{C_2} - V_i)(1 - D)$	
l ₂	$C_2 L R$	
ι_1	L	
ι ₀	$R(1-D)^{2}$	

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