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CMOS OTA-Based Filters for Designing Fractional-Order Chaotic Oscillators

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Abstract: Fractional-order chaotic oscillators (FOCOs) have shown more complexity than integer-order chaotic ones. However, the majority of electronic implementations were performed using embedded systems; compared to analog implementations, they require huge hardware resources to approximate the solution of the fractional-order derivatives. In this manner, we propose the design of FOCOs using fractional-order integrators based on operational transconductance amplifiers (OTAs). The case study shows the implementation of FOCOs by cascading first-order OTA-based filters designed with complementary metal-oxide-semiconductor (CMOS) technology. The OTAs have programmable transconductance, and the robustness of the fractional-order integrator is verified by performing process, voltage and temperature variations as well as Monte Carlo analyses for a CMOS technology of 180 nm from the United Microelectronics Corporation. Finally, it is highlighted that post-layout simulations are in good agreement with the simulations of the mathematical model of the FOCO.

Keywords: fractional-order chaotic oscillator; fractional-order integrator; CMOS technology; active filter; OTA; PVT analysis; Monte Carlo simulation

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1. Introduction

It is well known that chaotic systems can occur in various natural and man-made systems, and are known to have great sensitivity to initial conditions. On the one hand, as already mentioned in [1], according to the Poincaré–Bendixson theorem, autonomous and integer-order chaotic oscillators must have a minimum order of three for chaos to appear. The three ordinary differential equations (ODEs) can be associated to state variables that can be designed with complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) technology, as was done in [2], from three decades ago. On the other hand, fractional-order chaotic oscillators (FOCOs) do not follow the integer-order characteristic in which the number of state variables define the order. For example, if a FOCO is modeled by three ODEs and each derivate has a fractional-order equal to 0.9, then the fractional-order of the system is 2.7.

In the time domain, the majority of FOCOs can be simulated by applying approximations, such as Grüwnwald–Letnikov [3], Adams–Bashforth–Moulton and Adomian decompositions [4,5]. Those algorithms were implemented using embedded systems, such

as field-programmable gate arrays (FPGAs), but compared to analog solutions, they require huge hardware resources. For example, field-programmable analog arrays (FPAAs) and amplifiers were used to design FOCOs in [3,6], and fractional-order circuits were also implemented by a constant phase element, as shown in [7]. The authors in [8] showed cryptographic applications of a FOCO with high-effective analog computation, using amplifiers and two anti-parallel semiconductor diodes to provide a hyperbolic sine nonlinearity.

Some examples of the analog and digital implementations of commensurate (all derivatives have the same fractional order) or incommensurate (all or some derivatives have different fractional order) FOCOs are given in [3]. In the analog domain, and from a state-space point of view, the fractional-order derivative is solved by implementing a fractional-order integrator that can be designed using discrete amplifiers or FPAAs. The fractional-order integrator can be synthesized by fractances, fractal capacitors or other fractional-order topologies, as summarized in [3,9]. However, recently, the authors in [10] showed approximations of the fractional-order differentiator and integrator operators, using standard active filter transfer functions. Some CMOS realizations were validated via simulations, using CMOS technology of 350nm. More recently, a new category of fractional-order filters, realized without employing a fractional-order Laplacian operator, was introduced in [11], where the procedure resulted in a rational integer-order transfer function, and its implementation was possible, using conventional integer-order realization techniques. This is the focus of this work, following the design of FOCOs by cascading active filters, as shown in [12].

The operational amplifier (opamp) is the universal device used to implement chaotic systems [13], and hyper-chaotic [14], and multi-scroll attractors [15]. The voltage level of opamp-based implementations of FOCOs can be scaled down to allow FPAA implementations [12] but still, the silicon area is huge. In this manner, and as already demonstrated in [2], the CMOS operational transconductance amplifier (OTA) is helpful to reduce the silicon area when designing chaotic systems. Other CMOS amplifiers that are useful to design chaotic oscillators are summarized in [16], and others include the following: voltage differencing transconductance amplifier (VDTA) [17], current backward transconductance amplifier (CBTA) [18], operational trans-resistance amplifier (OTRA) [19], second-generation current conveyor (CCII), differential-input double-output transconductance amplifier (DOTA+), and differential voltage current conveyor (DVCC) [20]. Among them, the OTA shows advantages to develop cryptographic applications [21].

An incommensurate fractional-order Rössler system was implemented, using CMOS OTAs in [22]. The CMOS OTA was also used to design the fractional-order Newton–Leipnik chaotic system [23], and fractional-order neuron models [24,25]. In this manner, we show the CMOS OTA-based design of a fractional-order integrator that is approximated by a Laplace transfer function, as shown in [1]. The transfer function is synthesized herein by designing CMOS OTA-based first-order active filters, and the robustness of the CMOS FOCOs is verified by performing process, voltage and temperature (PVT) variations as well as Monte Carlo (MC) analyses [26]. The design of FOCOs using CMOS technology will improve applications in lightweight security [27], low-power and wireless secure communications [3], and Internet of Things [28].

The rest of this paper is organized as follows: Two FOCOs are the case study and are described in Section 2. Their block diagram descriptions in the Laplace domain and our proposed OTA implementations of the fractional-order integrator and FOCOs are shown in Section 3. Section 4 shows the design of OTAs, multiplier, saturated nonlinear function, and fractional-order integrator, using CMOS technology of 180 nm from the United Microelectronics Corporation (UMC). The layout design and post-layout simulations are given in Section 5, along with PVT and MC analyses to guarantee the robustness of the OTA-based CMOS FOCOs. Finally, the conclusions are given in Section 6.

2. Fractional-Order Chaotic Oscillators

Nowadays, fractional calculus is widely applied in many engineering areas; one of them was highlighted in the topic of fractional-order circuits and systems [3,9], where the main goal is the approximation of the fractional-order differentiator and integrator operators [10–12]. As emphasized in [29], the main advantage of fractional calculus is to extend the differential operators such that they exhibit non-integers orders. For instance, according to the Riemann–Liouville approach, the notion of a fractional integral of order $\alpha(\alpha > 0)$ is a natural consequence of the Cauchy formula defined in (1) for repeated integrals [30], where the gamma function is given in (2). Introducing the Laplace transform by the notation $\mathcal{L}\{f(t)\} = \int_0^\infty e^{-st} f(t)dt$ to (2), one can obtain (3), which is a generalization of the case with n-fold repeated integrals $(\alpha = n)$.

$$ {}_0I_t^\alpha f(t) \triangleq \frac{1}{\Gamma(\alpha)} \int_0^t (t-\tau)^{\alpha-1} f(\tau)d\tau \tag{1} $$

$$ \Gamma(\alpha) \triangleq \int_0^\infty e^{-t} t^{\alpha-1} dt \tag{2} $$

$$ \mathcal{L}\{{}_0I_t^\alpha f(t)\} = \frac{1}{s^\alpha}\mathcal{L}\{f(t)\} \tag{3} $$

Taking advantage of the Laplace transform, this section describes two representative FOCOs that are labeled as $FOCO_1$ and $FOCO_2$. $FOCO_1$ is taken from [31]; its scaled model in the Laplace domain, to allow the CMOS design, is given in (4), and it consists of three state variables: $X(s)$, $Y(s)$, and $Z(s)$, and one quadratic term x^2. From these equations, it can be appreciated that its implementation requires amplifiers, adders, subtractors, and one multiplier to design the quadratic term. The derivatives have a fractional order equal to 0.9, and it generates chaotic behavior by setting $a = 2.05$, $b = 1.12$, and $c = 0.42$, and using initial conditions equal to $x_0 = 0.1$, $y_0 = z_0 = 0$. Figure 1 shows the portraits of $FOCO_1$, which are obtained by plotting the state variables among them to appreciate the chaotic attractor.

$$ \begin{aligned} s^{0.9}X(s) &= Y(s) \\ s^{0.9}Y(s) &= Z(s) \\ s^{0.9}Z(s) &= -aX(s) - bY(s) - cZ(s) - 3X(s) * X(s) \end{aligned} \tag{4} $$

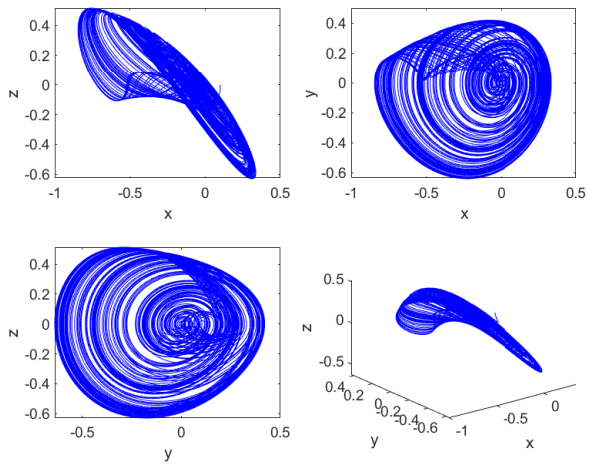


Figure 1. Portraits of the chaotic attractors of $FOCO_1$ given in (4). Each plot shows the attractor among two or three state variables x, y, z.

The second case study $FOCO_2$ has three derivatives of fractional-order 0.9 [32], and its model is given in (5). It consists of three state variables—$X(s)$, $Y(s)$, and $Z(s)$—and a nonlinear function denoted by $f(x)$ that can be approximated by saturated nonlinear

function (SNLF) series. From (5), one can observe that the design requires amplifiers, adders, and subtractors, and the SNLF is manipulated to generate multi-scroll attractors. For example, a two-scroll attractor can be implemented by modeling the SNLF by (6), where m is the slope of the linear segment in the ranges $-bp \leq x \leq bp$, with bp as a break-point, and the saturation level is given by k. It is simulated by setting $a = b = c = d_1 = 0.7$, $m = k/bp = 0.5/0.1$ for $f(x)$, and initial conditions $x_0 = y_0 = z_0 = 0.1$. Figure 2 shows the portraits of $FOCO_2$, which are obtained by plotting the state variables among them to appreciate the chaotic attractor.

$$\begin{aligned} s^{0.9}X(s) &= Y(s) \\ s^{0.9}Y(s) &= Z(s) \\ s^{0.9}Z(s) &= -aX(s) - bY(s) - cZ(s) + d_1 f(x) \end{aligned} \tag{5}$$

$$f(x) = \begin{cases} -k & \text{if} \quad x < bp \\ mx & \text{if} \quad -bp \leq x \leq bp \\ k & \text{if} \quad x > bp \end{cases} \tag{6}$$

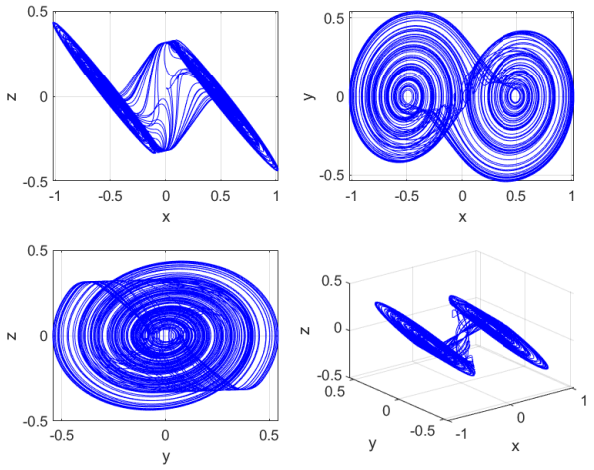


Figure 2. Portraits of the chaotic attractors of $FOCO_2$ given by (5). Each plot shows the attractor among two or three state variables x, y, z.

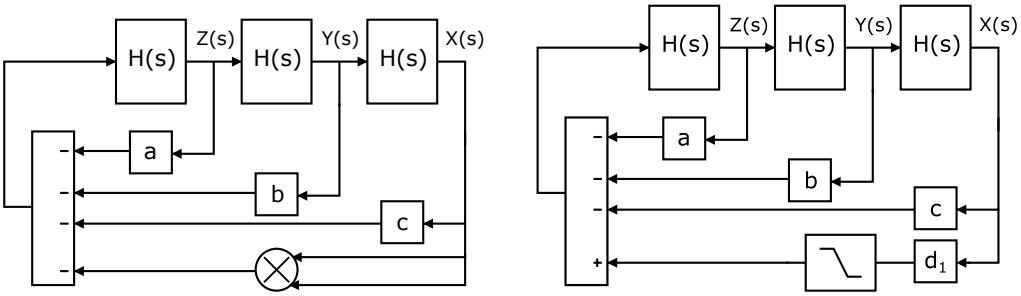
The amplitudes of the state variables of both FOCOs are lower than ± 1, so they are suitable to be implemented with CMOS technology of 180 nm from UMC, which is biased by ± 0.9 V.

3. Approximation of the Fractional-Order Integrator by OTA Filters

According to [1,3], the fractional-order integrator can be approximated by $H(s) = 1/s^{0.9}$, and therefore, Figure 3 shows the block diagrams of $FOCO_1$ and $FOCO_2$. In this paper, the fractional-order is set to 0.9, whose approximated transfer function is given in (7) [1]. The design of OTA-based active filter topologies can be performed by using first-order functions, as already shown in [33]. Henceforth, the transfer function of a fractional-order integrator $H(s)$ can be arranged to multiply first-order functions as given in (8). As one sees, $H_1(s)$ and $H_2(s)$ have one zero and one pole, and can be designed with first-order shelving equalizers, while $H_3(s)$ can be designed by one low-pass filter.

$$H(s) = \frac{1}{s^{0.9}} \approx \frac{2.2675(s + 1.292)(s + 215.4)}{(s + 0.01292)(s + 2.154)(s + 359.4)} \tag{7}$$

$$
\begin{aligned}
H_1(s) &= \frac{s+215.4}{s+359.4} \\
H_2(s) &= \frac{s+1.292}{s+2.154} \\
H_3(s) &= \frac{2.2675}{s+0.01292}
\end{aligned} \tag{8}
$$

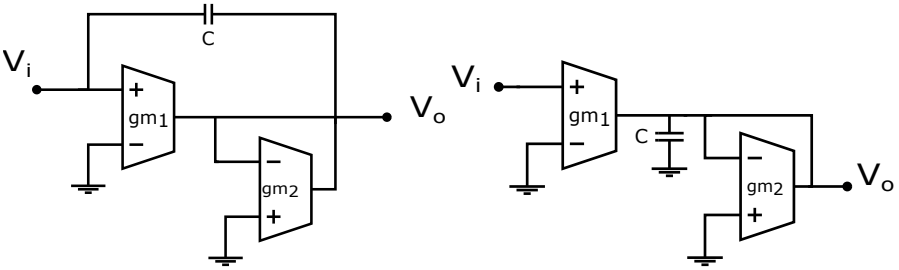


(**a**) $FOCO_1$ can be synthesized by three fractional-order integrators, amplifiers, one adder with 4 negative inputs, and one multiplier to evaluate X(s)*X(s) from (4).

(**b**) $FOCO_2$ can be synthesized by three fractional-order integrators, amplifiers, one subtractor with 1 positive input and 3 negative inputs, and a SNLF (placed after block d_1).

Figure 3. Block diagrams of the FOCOs, where $H(s) = 1/s^{0.9}$.

The first-order active filters are designed with the OTA-based topologies shown in Figure 4. As highlighted in [33], the shelving equalizer can independently adjust the pole and zero, and the transfer function from Figure 4a is given in (9), while that for the low-pass filter shown in Figure 4b is given in (10).



(**a**) Shelving equalizer

(**b**) Low-pass filter

Figure 4. OTA-based first-order active filters taken from [33], to implement: (**a**) $H_1(s)$ and $H_2(s)$, and (**b**) $H_3(s)$.

$$
\frac{V_{out}}{V_{in}} = \frac{s+gm_1/C}{s+gm_2/C} \tag{9}
$$

$$
\frac{V_{out}}{V_{in}} = \frac{gm_1/C}{s+gm_2/C} \tag{10}
$$

From (9) and $H_1(s)$, one can choose the value of gm_1 to evaluate C and the resistance generated by gm_2. Therefore, if $gm_1 = 500$ µA/V the capacitor value is obtained as $C = \frac{gm_1}{215.4} = 2.32$ µF. In this manner, $gm_2 = (2.32\ \mu F)(359.4) = 833$ µA/V. The same process is performed to evaluate all the transconductances of the OTAs and Cs associated to $H_2(s)$ and $H_3(s)$. For $H_2(s)$, $gm_1 = 500$ µA/V, $C = 386$ µF, and $gm_2 = 833$ µA/V. For $H_3(s)$, $gm_1 = 500$ µA/V, $C = 221$ µF, and $gm_2 = 2.93$ µA/V.

Our proposed OTA implementation of the fractional-order integrator is shown in Figure 5, where it is worth mentioning that the three first-order OTA filters are connected in cascade, considering that the filter with the largest zero and largest pole is placed at the input port, i.e., $H_1(s)$.

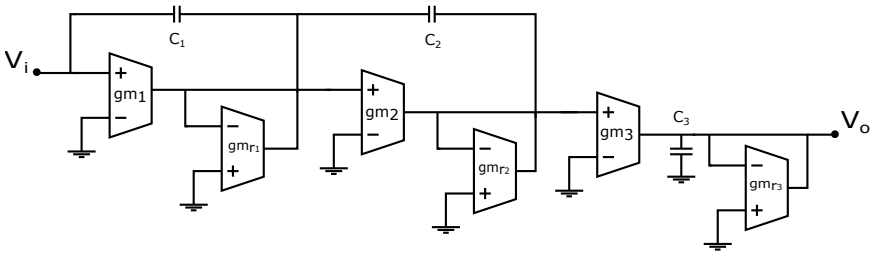


Figure 5. Proposed OTA design of $\frac{1}{s^{0.9}}$ that is approximated by (7), and designed by cascading $H_1(s)H_2(s)H_3(s)$.

The OTAs can be macro-modeled into the simulation program with IC emphasis (SPICE). That way, from Figure 3a our proposed OTA implementation of $FOCO_1$ is shown in Figure 6, where $H(s)$ is designed as shown in Figure 5. The HSPICE simulation of $FOCO_1$ is done by setting the transconductance values as follows: gm_a to gm_h are obtained to accomplish the values of the coefficients $a = 2.05$, $b = 1.12$ and $c = 0.42$ given in (4). For instance, if $gm_1 = 500$ µA/V, then gm_a must be 2.05 times gm_1. The same process is performed to obtain all the transconductance values so that $gm_a = 1025$ µA/V, $gm_b = 560$ µA/V, $gm_c = 210$ µA/V and $gm_g = 3000$ µA/V. $gm_h = 500$ µA/V, and is used to transform the sum of the output currents of each OTA into voltage.

The multiplier is implemented with the macro-model AD734. The simulation results of our proposed OTA-based $FOCO_1$ are shown in Figure 7.

From Figure 3b, our proposed OTA implementation of $FOCO_2$ is shown in Figure 8, where $H(s)$ is designed as shown in Figure 5. The HSPICE simulation of $FOCO_2$ is done by setting $gm_a = 350$ µA/V, $gm_b = 350$ µA/V, $gm_c = 350$ µA/V, $gm_d = 350$ µA/V and $gm_e = 1000$ µA/V. The SNLF block is macro-modeled by a piecewise-linear (PWL) function with breakpoints $bp = 0.1$ and $k = 0.5$. The simulation results of the OTA-based $FOCO_2$ are shown in Figure 9.

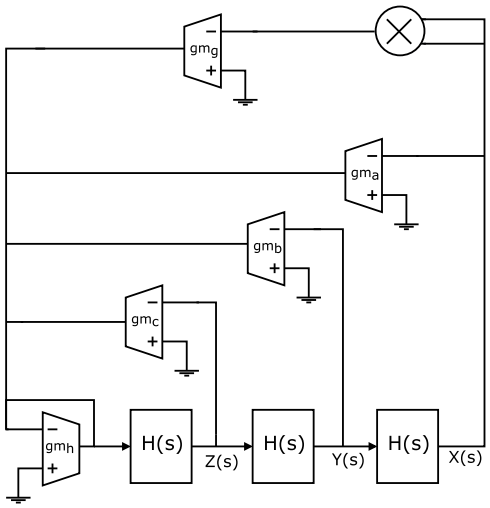
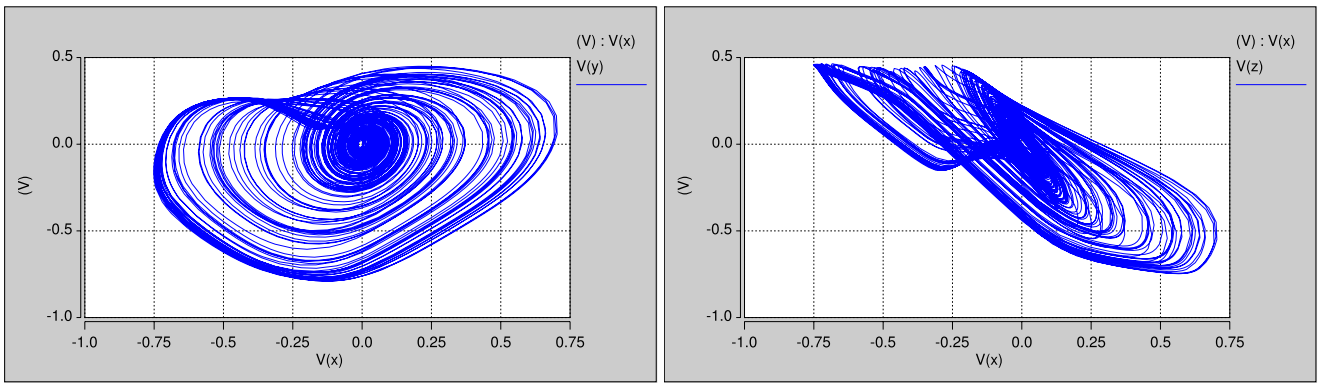
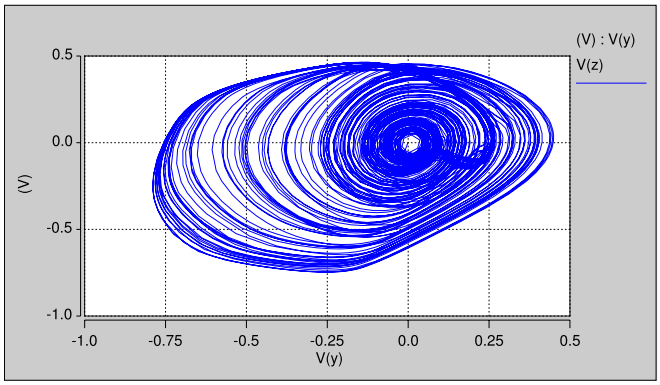


Figure 6. Proposed OTA implementation of the $FOCO_1$ given in (4).



(**a**) Attractor between states x vs y

(**b**) Attractor between states x vs z



(**c**) Attractor between states y vs z

Figure 7. Portraits of the HSPICE simulation of $FOCO_1$ from Figure 6.

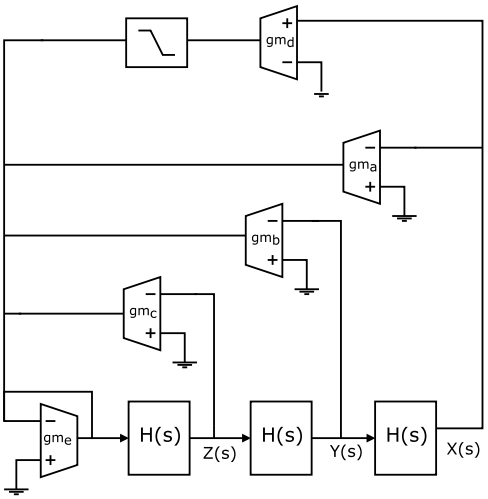
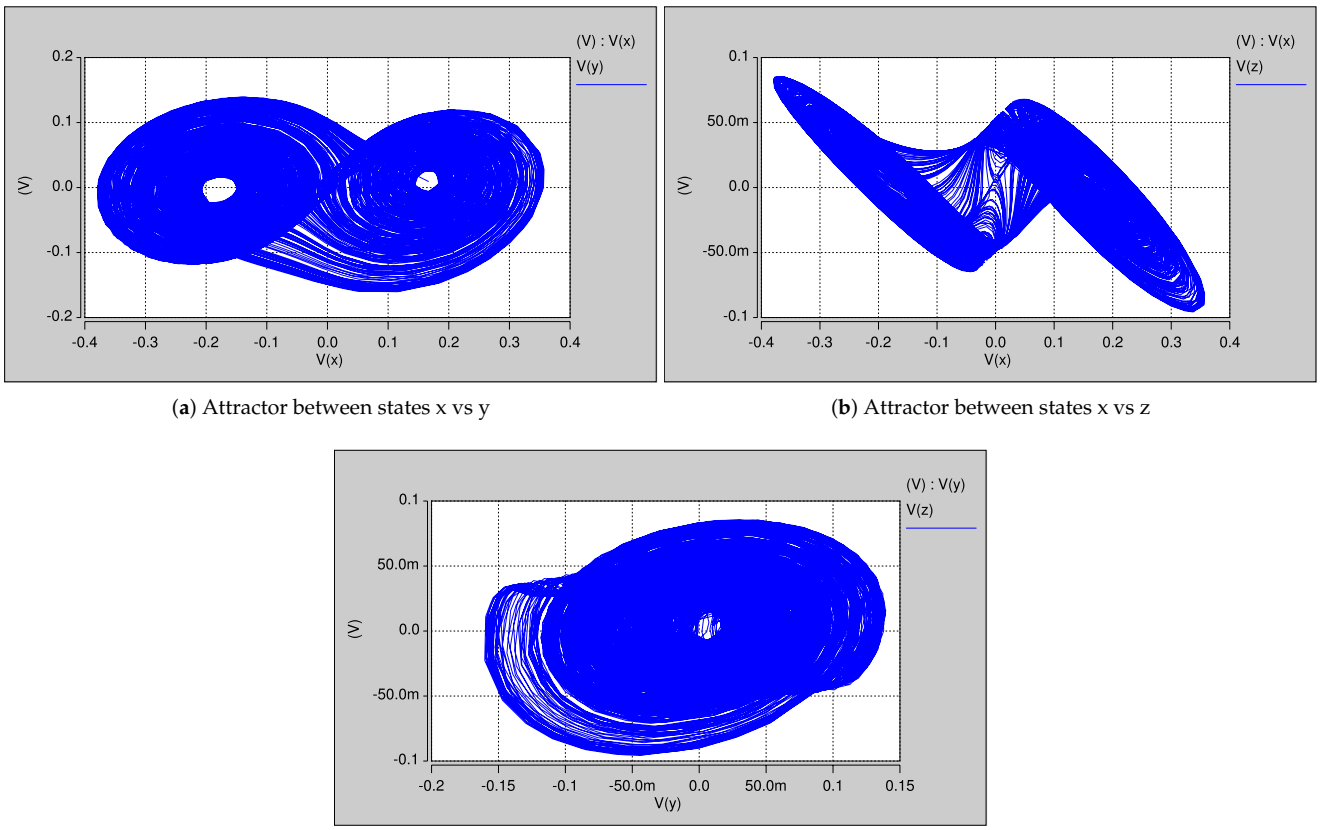


Figure 8. Proposed OTA implementation of the $FOCO_2$ given in (5).



(**a**) Attractor between states x vs y

(**b**) Attractor between states x vs z

(**c**) Attractor between states y vs z

Figure 9. Portraits of the HSPICE simulation of $FOCO_2$ from Figure 8.

4. CMOS Design of the OTAs, Multiplier, Nonlinear Function and Fractional-Order Integrator

The CMOS design of FOCOs becomes a challenge, due to the high level of accuracy required to accomplish the characteristics of the OTAs, the fractional-order integrator and nonlinear functions to create the attractor. For instance, the OTAs require high differential gain, high gain-bandwidth product, and the best linearity as possible [34]. In addition, an OTA must be robust to PVT and Monte Carlo variations [35]. This section details the design of the blocks required to implement the proposed OTA-based $FOCO_1$ shown in Figure 6 and $FOCO_2$ shown in Figure 8, by using CMOS technology of 180 nm from UMC.

4.1. CMOS Operational Transconductance Amplifier (OTA)

The OTA that is required to implement a FOCO must provide high linearity to accomplish the characteristics of the fractional-order integrator. A slight variation in the linearity may generate a fractional-order different from the desired one, and the response of the FOCO may be mitigated or be different from the desired one. The linearity of the OTA is characterized by its transconductance gm, which must be linear in the entire dynamic range.

As for the $FOCO_1$ the transconductances have values between 210 µA/V and 3000 µA/V, and since the range in which the gm of an OTA can be varied with the variable resistors is only ±150 µA/V, then the variable resistors are mainly used to improve the accuracy of the OTA. For this reason, this paper uses different sizes of the transistors and the OTA with programmable gm shown in Figure 10, where the transconductance is tuned by the resistors R connected in the sources of the differential pair. The Rs can be designed with MOS transistors, as detailed in [36], and the bias of the flipped voltage-followers are designed according to [37]. The sizes of the CMOS OTA, to provide a $gm = 500$ µA/V and $gm = 350$ µA/V, are shown in Table 1 by using a load capacitor of C_L = 220 pF. The table

lists the direct current (DC) gain in decibels (dB), gain-bandwidth (GBW) in kilo hertz (KHz), phase margin (PM) in degrees (°), common-mode rejection ration (CMRR) in dB, slew rate (SR) in volt/ µs, power supply rejection ratio (PSRR), power dissipation in milli-watts, the small and large-signal figures of merit (FoM) from [35], the width (W) and length (L) of the MOS transistors in micro-meters, and the bias current (Ib).

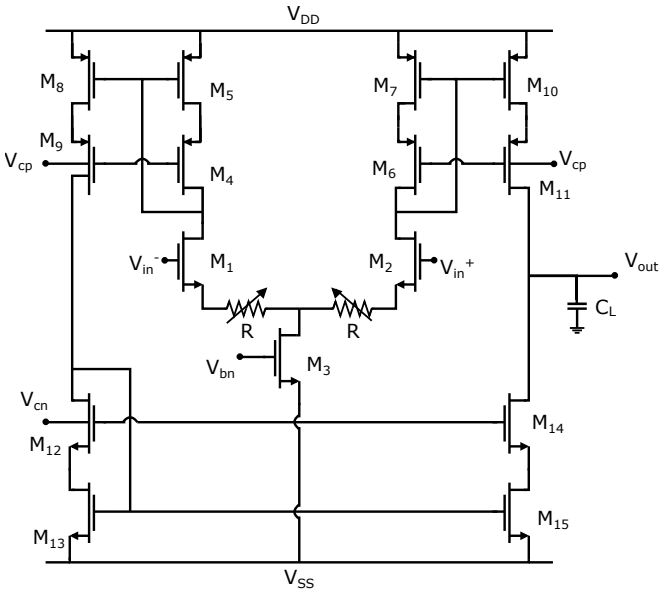


Figure 10. CMOS OTA taken from [36].

To design both FOCOs, other transconductances (gm) are required. Table 1 shows the sizes of the MOS transistors of two gm values, but for the complete design, seven gm values are required, namely, 2 µA/V, 200 µA/V, 350 µA/V, 500 µA/V, 800 µA/V, 1000 µA/V, and 3000 µA/V. These gms are obtained by designing the CMOS OTA with different bias currents and voltage controls of the degenerated resistors that are implemented by MOS transistors as shown in [36].

Table 1. Electrical characteristics and sizes of the CMOS OTA shown in Figure 10 to provide a $gm = 500$ µA/V and $gm = 350$ µA/V.

Parameter	gm = 500 u	gm = 350 u
DC GAIN (dB)	61.232	61.125
GBW (KHz)	425	419
PM (°)	88.96	88.943
CMRR (dB)	73	74
SR+ (v/µs)	0.098	0.095
SR- (v/µs)	0.106	0.105
PSRR+ (dB)	89	89
PSRR- (dB)	61	61
Power dissipation (mW)	3.19	3.18
FoM_s	1856.8	1843.6
FoM_l	431.2	418
W(M1,M2) (µm)	20.16	20.16
W(M3,M14,M15) (µm)	39.6	39.6
W(Mb,M12,M13) (µm)	19.8	19.8
W(M4-M9) (µm)	61.2	61.2
W(M10,M11)(µm)	122.4	122.4
L(µm)	1.8	1.8
Ib (µA)	50	50

4.2. CMOS Multiplier Design

To evaluate X(s)*X(s) in Figure 6, the CMOS multiplier is designed by using the topology shown in Figure 11. This CMOS circuit is a four-quadrant multiplier in which both the input and output signals fluctuate among positive and negative values, and it was introduced in [38].

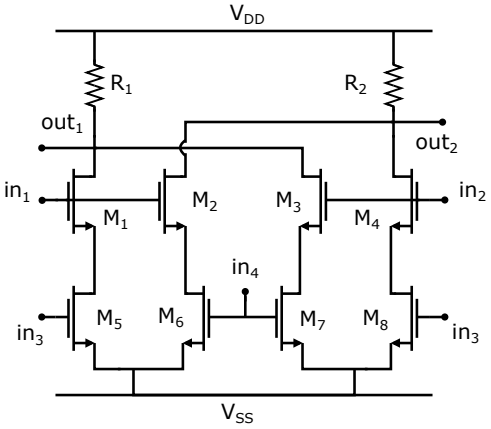


Figure 11. Fully differential four-quadrant multiplier taken from [38].

The sizes of the MOS transistors are found by considering that they are operating in the saturation region, as shown in [35]. The W/L ratios of all the MOS transistors from M_1 to M_8 are equal to 1.44 µm/0.18 µm. The resistance values are calculated to be $R_1 = R_2 = 3$ kΩ. The CMOS multiplier was tested with sinusoidal waveforms connected in the differential inputs $(V_{in1} - V_{in2})$ and $(V_{in3} - V_{in4})$, with the differential output taken as $(V_{out2} - V_{out1})$. The multiplication result is shown in Figure 12. This is worth mentioning since a single-ended output is needed in Figure 6. Then, we propose the addition of an OTA subtractor, as shown in Figure 13, to provide $V_{out} = V_{out2} - V_{out1}$, where $gm_a = gm_b = gm_c = 500$ µA/V.

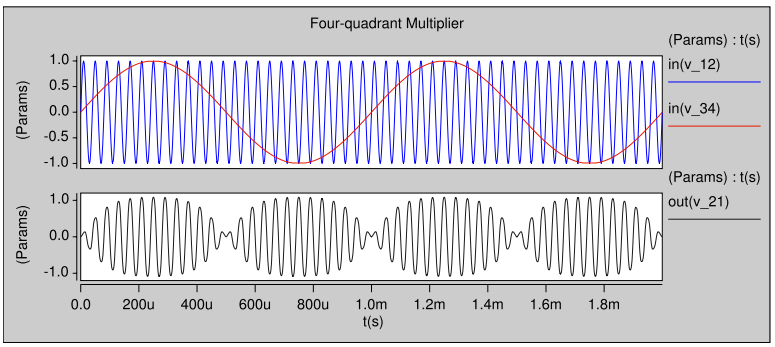


Figure 12. Multiplication of two signals using the CMOS design from Figure 11.

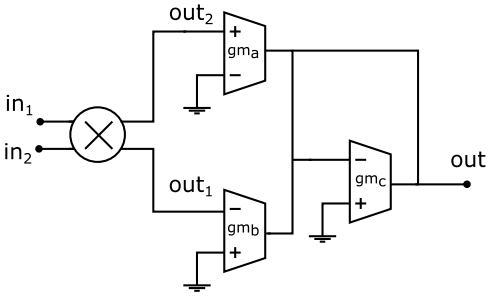


Figure 13. Proposed single-ended multiplier combining the fully-differential multiplier shown in Figure 11 and an OTA-subtractor.

4.3. Saturated Nonlinear Function (SNLF) Design

In the case of $FOCO_2$, it requires a SNLF block to design the PWL function shown in Figure 3b, which has three linear segments. This SNLF can be designed by the CMOS topology shown in Figure 14, which was proposed in [36]. This CMOS circuit presents advantages, such as programmability of the slope m, saturation level k, and break-points bp required in (6). The sizes of the MOS transistors are $W = 1.35$ µm for M_1, M_2, M_3, $W = 6.3$ µm for M_4, and all the lengths are set to $L = 0.18$ µm.

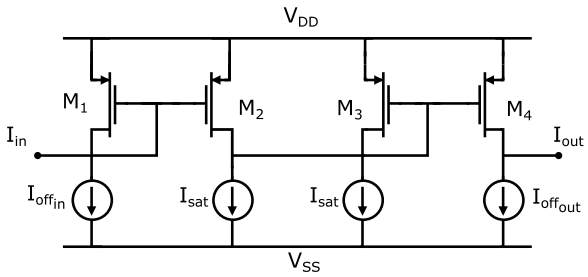


Figure 14. CMOS design of the SNLF block taken from [36].

4.4. Proposed CMOS Fractional-Order Integrator

As shown in Figure 5, our proposed OTA design of the fractional-order integrator $1/s^{0.9}$ needs the design of the CMOS OTAs, whose transconductances are set to 500 µA/V, 800 µA/V and 2 µA/V. Table 1 shows the sizes of the OTA to provide a $gm = 500$ µA/V, and Tables 2 and 3 show the W/L sizes of the OTAs to provide transconductances of 800 µA/V and 2 µA/V, respectively. The multiplicity value is necessary to design the layout, as shown in [35,36].

Table 2. Sizes of the OTA shown in Figure 10 to provide a $gm = 800$ µA/V.

Transistor	W(µm)	L(µm)	Multiplicity
M_1, M_2	5.04	1.8	4
M_3, M_{14}, M_{15}	9.9	1.8	4
M_b, M_{12}, M_{13}	9.9	1.8	2
$M_4 - M_9$	30.6	1.8	2
M_{10}, M_{11}	30.6	1.8	4

Table 3. Sizes of the OTA shown in Figure 10 to provide a $gm = 2$ µA/V.

Transistor	W(µm)	L(µm)	Multiplicity
M_1, M_2	1.26	1.8	4
M_3	2.52	1.8	4
$M_b, M_4 - M_{11}, M_{12} - M_{15}$	2.52	1.8	2

5. Layout Design and Post-Layout Simulation Results

The layout of the OTA with a $gm = 500$ µA/V is shown in Figure 15, which considers electromigration and symmetry, and a maximum height is determined for the final layout to implement the FOCOs in a reduced silicon area. The other OTAs, having different gm values, are designed in a similar manner. So, the layout of our proposed OTA-based fractional-order integrator is shown Figure 16, which consists of six OTAs (see Figure 5): three OTAs having $gm = 500$ µA/V, two OTAs of $gm = 800$ µA/V and the last and smallest (on the right side) having $gm = 2$ µA/V. The capacitors are set to: $C_1 = 2.5$ µF, $C_2 = 380$ µF and $C_3 = 220$ µF.

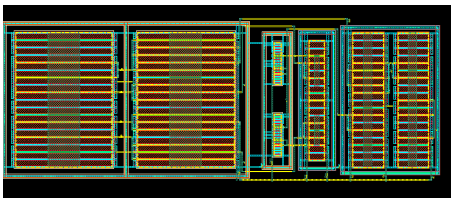


Figure 15. Layout of the CMOS OTA providing $gm = 500$ µA/V.

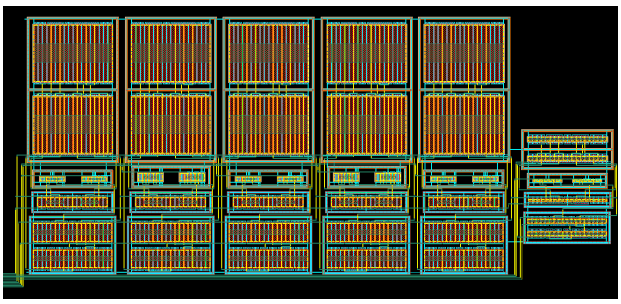


Figure 16. Layout of our proposed OTA fractional-order integrator to approximate $1/s^{0.9}$.

The post-layout simulation of our proposed CMOS fractional-order integrator $H(s) = 1/s^{0.9}$, has very low error compared to the ideal transfer function in the MatLab-evaluation from (7), compared to the OTA macro-model simulation from Figure 5, and compared to the HSPICE simulation using MOS transistor models, as shown in Figure 17. This guarantees exactness in the implementation of FOCOs.

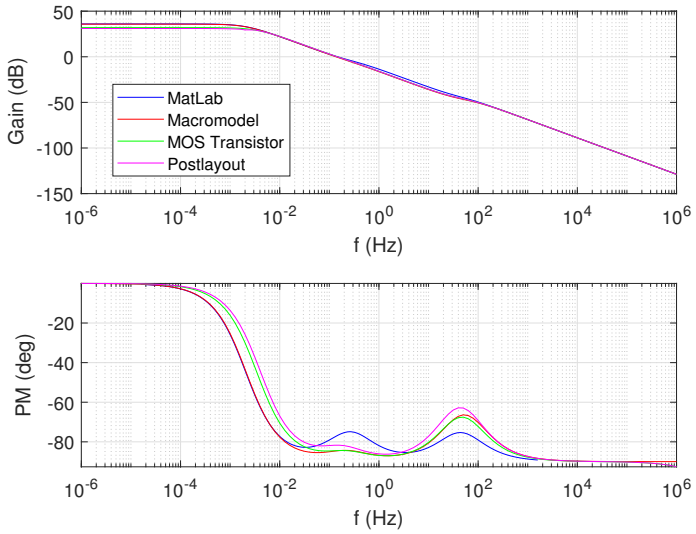
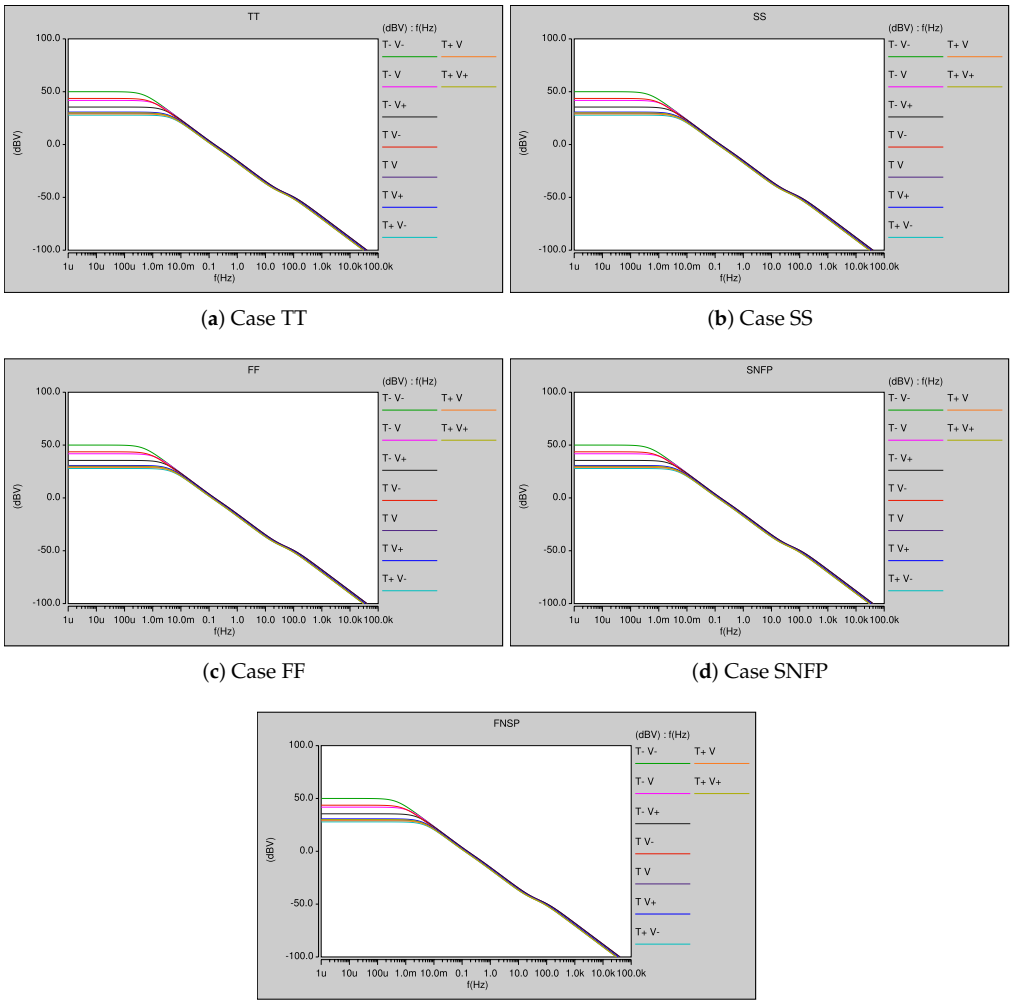


Figure 17. Comparison of the gain (up side) and phase margin (down side) responses of the fractional-order integrator $H(s) = 1/s^{0.9}$, considering the ideal transfer function approximation in MATLAB, macro-modeling the OTAs, HSPICE simulation using MOS transistor models, and post-layout simulation.

It is important to mention that the initial values of the CMOS fractional-order integrator, do have an effect on the power consumption. If the initial values are large, the power consumption of the CMOS circuit increases since both the transient time and the voltage on the capacitors increase. Using small initial values, the power consumption is 149.8 µW.

PVT variations analyses are performed to ensure robustness of the fractional-order integrator response. For instance, Figure 18 shows the AC response under PVT variations. Each of the five corners (typical–typical (TT), fast–fast (FF), slow–slow (SS), slowN–fastP (SNFP) and fastN–slowP (FNSP)) is simulated by varying 10% of the supply voltage and varying the temperature from $-20°$, $60°$, to $120°$. The variability due to matching

conditions of the MOS transistors is evaluated by performing Monte Carlo analysis for 1000 runs and assuming 10% deviation (with a Gaussian distribution) in W and L for all the MOS transistors, whose results are given in Figure 19. This ensures robustness of our proposed fractional-order integrator and demonstrates its suitability to design CMOS FOCOs.



(**a**) Case TT (**b**) Case SS

(**c**) Case FF (**d**) Case SNFP

(**e**) Case FNSP

Figure 18. Process–voltage–temperature (PVT) variation simulations of the CMOS fractional-order integrator shown in Figure 16.

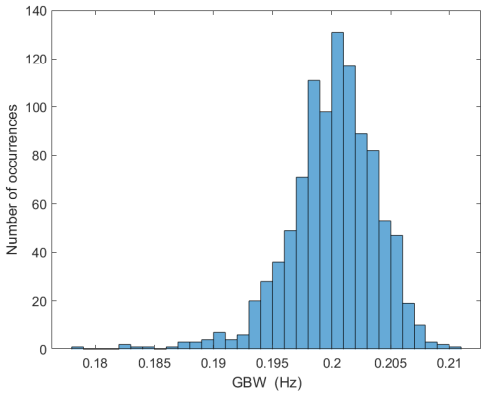


Figure 19. Monte Carlo simulation of our proposed CMOS fractional-order integrator shown in Figure 16.

The proposed OTA implementation of $FOCO_1$ given in (4) is shown in Figure 6. To save the CMOS silicon area, capacitors are scaled in frequency to have values in pF instead of μF [39]. So, the capacitor values are scaled to become $C_1 = 2.5pF$, $C_2 = 380pF$ and $C_3 = 220pF$. The layout of our proposed CMOS OTA-based $FOCO_1$ is shown in Figure 20, where it can be appreciated the layout of three fractional-order integrators on the left side, and the remaining circuitry on the right side. Finally, the post-layout simulation of $FOCO_1$ is shown in Figure 21, which shows good agreement with the dynamical behavior of its associated mathematical model shown in Figure 1.

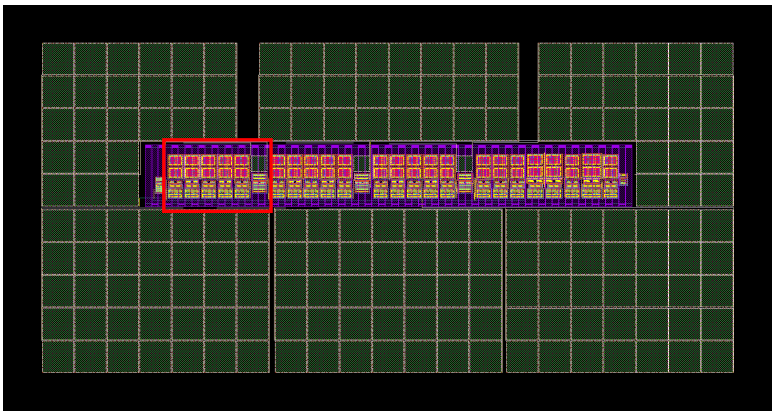
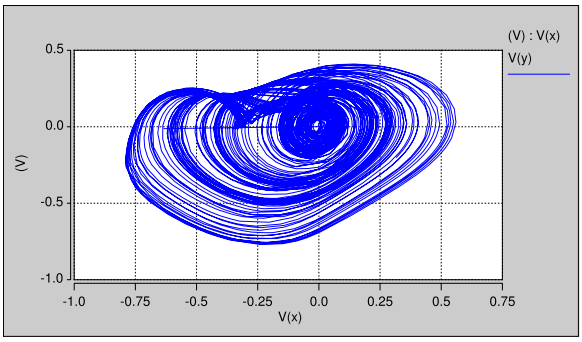
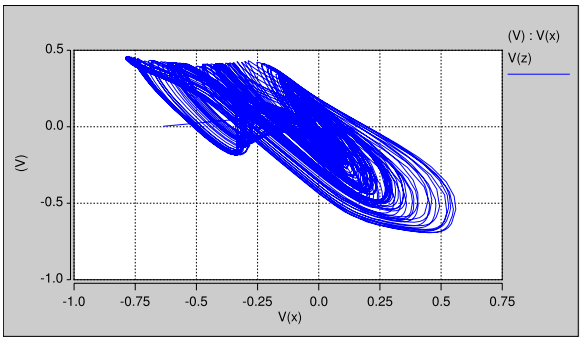


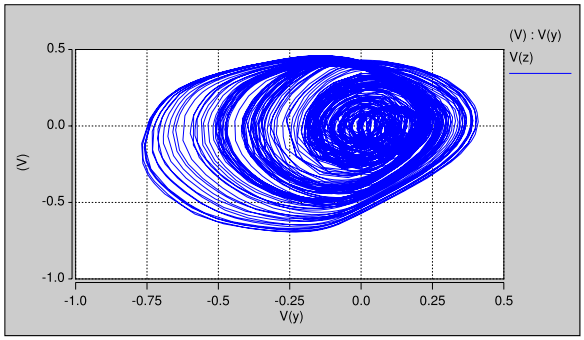
Figure 20. Layout of our proposed CMOS OTA-based $FOCO_1$ shown in Figure 6.



(**a**) Attractor between states x vs y



(**b**) Attractor between states x vs z



(**c**) Attractor between states y vs z

Figure 21. Portraits of the post-layout simulation of our proposed CMOS OTA-based $FOCO_1$.

6. Conclusions

It was shown that the fractional-order integrator, such as $1/s^{0.9}$, can be designed with CMOS IC technology in order to design CMOS FOCOs. In this manner, we proposed the CMOS design of the fractional-order integrator by cascading first-order active filter blocks that were implemented by OTAs. The CMOS OTAs were designed with IC technology of

180 nm from UMC; they allow programming of the transconductance gm. The robustness of our proposed CMOS OTA-based fractional-order integrator was verified by performing PVT and Monte Carlo analyses. The post-layout simulation results of the CMOS design of $FOCO_1$ were in good agreement with the mathematical model. One may use other CMOS technologies and also different fractional-orders just by synthesizing the corresponding Laplace transfer functions by cascading OTA-based first-order filters. As a conclusion, our proposed designs demonstrated the usefulness of the CMOS fractional-order integrators to design FOCOs that can be used to enhance applications in lightweight cryptography, low-power and wireless secure communications and Internet of Things.

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