

Article

Interconnections for Additively Manufactured Hybridized Printed Electronics in Harsh Environments

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Abstract: The ability to fabricate functional 3D conductive elements via additive manufacturing has opened up a unique sector of ‘hybridized printed electronics’. In doing so, many of the rigid standards (i.e., planar circuit boards, potting, etc.) of traditional electronics are abandoned. However, one critical challenge lies in producing robust and reliable interconnections between conductive inks and traditional hardware, especially when subjected to harsh environments. This research examines select material pairings for the most resilient interconnection. The method of test is wire bond pull testing that would represent a continuous strain on a connection and high acceleration testing of up to 50,000 g that would represent a sudden shock that electronics may experience in a drop or crash. Although these two environments may be similar to an overall energy exerted on the connection, the rate of force exerted may lead to different solutions. The results of this research provide insight into material selection for printed electronic interconnections and a framework for interconnection resiliency assessment, which is a critical aspect in realizing the production of next generation electronics technologies for the most demanding environments.

Keywords: conductive epoxy; conductive ink; harsh environments; high acceleration testing; interconnections; low temperature solder; printed electronics; wire bond pull testing

1. Introduction

The 3D fabrication of conductive materials via additive manufacturing (AM) and its integration with traditional hardware and processes has led to the field of hybridized printed electronics [1–6]. Although conventional electronics manufacturing has high integration density and resolution, it generally prohibits electronics fabrication in 3D space in terms of conformal, curved, or irregular objects, or is expensive and time consuming for part specific tooling that makes low production runs highly uneconomical [2,7–9]. This is where 3D structural printed electronics via AM are innovative and excel, even though their drawbacks consist of lower integration density/resolution and less conductive materials [10–14]; however, this margin is narrowing as AM process achieve finer resolution. Therefore, 3D printed electronics offer customizable electronic components in 3D space with reduced lead time and inventory in a less expensive—especially for low production runs—yet more streamlined manufacturing process [15–17]. To date, 3D printed electronics have been demonstrated in various forms including antennas, embedded electronics, smart devices, structural/health monitors, electronic textiles, and other passive electronic elements including RFID tags, coplanar waveguides, and capacitors [4,18–31].

One remaining challenge of 3D printed electronics is: what is the best way to interconnect printed electronic elements to commercial-off-the-shelf (COTS) components, especially if the electronics will be in an application that will be subjected to harsh environments? [32] In this work, an interconnection is defined as the electrical, mechanical, and thermal bond of the printed electronic element to a COTS component [33,34]. Conductive epoxies/adhesives have been explored for traditional electronic components [35–40], and more recently, for printed electronics [32,41–44] as an interconnection material, since conventional solders potentially cause local thermal damage to the heat sensitive printed electronic elements and low temperature substrates that typically have maximum temperatures less than 200 °C [1,45]. However, the resilience of conductive epoxy interconnection to printed electronic systems when subjected to high accelerations remains unknown. Additionally, the use of low temperature solders with melting points less than 200 °C is garnering interest for use in printed electronics, but there exists a gap in the literature for evaluating resilient interconnections (both conductive epoxy and low temperature solders) to printed electronic elements. The reduced temperatures of low temperature solders not only reduce the thermal impact to thermally sensitive materials, but also reduce energy cost/cycle time and are less toxic since they are lead free [45–51].

Common low temperature solders consist of tin (Sn) with varying compositions of bismuth (Bi) or indium (In). Bi soldering alloys tend to have higher strength but reduced ductility and susceptibility to thermal aging [52–58]. On the other hand, In is a much softer alloy, which reduces its strength, yet it has greater ductility. Alloys of In are also not as susceptible to thermal aging but it is significantly more expensive than Bi [53,57,59]. A small addition of silver (Ag) with typical weight composition less than 1% in Bi and In solder alloys can improve the reduced properties in both alloys [52,55,57,58,60].

This work evaluates the performance of conductive epoxy and low temperature solders composed of Sn, Bi, and In, with wire bond pull testing and high acceleration drop tower testing up to 50,000 g, to access the survivability of interconnections for 3D printed electronics in harsh environments, which was identified as a knowledge gap in the literature. The designs were made to maximize efficiency of sample testing and minimize materials while being relevant to printed electronics systems. High acceleration drop tower testing up to 50,000 g subjects the interconnections for printed electronics to an extremely harsh condition, thus elucidating how these interconnection materials may survive in the field and filling some of the knowledge gap for printed electronics interconnections.

2. Materials and Methods

2.1. Materials

Table 1 shows the selection of materials for interconnections to printed electronics in this work. The conventional ‘eutectic’ solder consisting of 63 weight % tin (Sn) and 37 weight % lead (Pb) was chosen to evaluate the influence of the much higher soldering tip temperature interconnection performance when comparing the low temperature Indium, Inc. solders. Indium solders were chosen with high weight compositions of both bismuth (Bi) and indium (In). As highlighted in the introduction, solder with high concentrations of Bi exhibit higher strength but are not as ductile as the softer and lower strength In alloys. A few of the Indium low temperature solders also have low weight compositions of silver (Ag) to evaluate if Ag enhances the solder performance as referenced in the introduction. Epo-tek H20E was selected for the conductive epoxy as it has a high loading of Ag (60–100% based on the manufacturer’s data sheet) and is cured at 100 °C for two hours after deposition.

The Indium low temperature solders range in density from 7.00 to 8.40 g/cc (from the manufacturer’s datasheet), while H20E conductive epoxy was measured to have a density of 2.92 ± 0.26 g/cc, which is less than 3× the density of the low temperature solders. On the other hand, the solders will have higher conductivity, since they are pure metal alloys, but this will not be major factor for most printed electronic components since the cross-sectional area is large and the length is small. Conductive epoxy also takes much longer as a post-process interconnection method as most conductive epoxies need around an hour to fully cure, whereas a soldered interconnection can be fabricated in seconds.

The rest of this work highlights the impacts of density, electrical resistance, and ease of use for resilient interconnections for printed electronics.

Table 1. Solder and conductive epoxy composition and soldering/curing temperatures.

Interconnection Material	Composition (wt%)	Solder Tip Temperature (°C)
Sn/Pb ‘Eutectic’ solder	63Sn/37Pb	370
Indium Inc. solder 281	58Bi/42Sn	245
Indium Inc. solder 282	57Bi/42Sn/1Ag	245
Indium Inc. solder 290	97In/3Ag	245
Indium Inc. solder 1E	52In/48Sn	220
Epo-tek H20E conductive epoxy	60–100Ag/0–40epoxy	Curing: 2 h @ 100 °C

2.2. Testing Methods

An nScrypt Tabletop 3D η system and SmartPumpTM was utilized to micro-dispense NovaCentrix silver conductive ink HPS-FG57B and DuPont copper conductive ink CB230. The designs were carefully chosen to enable efficient and repeatable sample production, as described in the following sections, for common interconnection of wire bonding or pin connecting. The conductive inks were deposited to a nominal thickness of $54.8 \pm 4.6 \mu\text{m}$ on 1.59 mm (1/16”) thick poly-ether-ether-ketone (PEEK) substrates (McMaster-Carr Part # 8504K21) into $5 \times 5 \text{ mm}^2$ conductive ink interconnection pads. Table 1 lists the variety of interconnection materials used with their respective weight composition and temperatures.

The soldering samples were manually soldered with various soldering iron tips (Table 1). The manual soldering process intended to minimize the local heat input to the conductive ink and substrate to reduce the risk of compromising the adhesion of the conductive ink. The soldering tip temperatures are higher than minimum temperatures to flow the solder, but the minimum temperatures require much longer dwell times and we posit this results in more heat transfer to the conductive ink and substrate than using higher temperatures with much shorter dwell times (a few seconds for the interconnections in this work). The excess flux was removed from the solder interconnection using two different methods for comparison. The first uses Miller-Stephenson Heavy Duty Solvent and Flux Remover MS-555 by spraying the aerosol on the interconnections, ink, and substrate for ~ 3 s, and then, letting the aerosol evaporate. The second flux remover method uses 20 ounces of water heated to 65 °C before putting it in an ultrasonic sonicator with the interconnection sample and 2 mL of Dawn dish soap. The sonicator was then turned on for 10 min at 20 kHz to remove the excess flux with the interconnection sample submersed. The first method is termed ‘solvent’ while the second method termed ‘solvent-free’ in the following sections.

The Epo-tek H20E conductive epoxy deposition was performed with a pneumatic pick-and-place, with single droplets using 14 psi and a syringe tip diameter of 1 mm (19 gauge). A vortex mixer was also used on a set of samples to increase the area of the H20E conductive epoxy, which was performed on a S0100A Cole Parmer vortex mixer on the max acceleration setting for 90 s.

Wire bond pull samples were fabricated by interconnecting the solders or H20E conductive epoxy to a 0.81 mm outer diameter (20 gauge) 100 mm long braided copper wire to the printed conductive ink (Figure 1). Each $50 \times 20 \text{ mm}^2$ PEEK substrate consisted of five wire bond pull samples spaced 10 mm apart. Two batches were fabricated and tested for a total of 10 samples per sample type. Once fabricated, the wire bond pull samples were tested according to MIL-STD-883F 2011.7 Bond Strength Condition H with an Admet tensile tester by clamping the free end of the substrate and the end of the wire while applying the force along the long axis of the wire at a ramp rate of 1 mm/min. Wire bond pull testing with conductive inks does not have a current standard but MIL-STD-2011.7 H permits testing adhesion and interfacial strengths of interconnection materials when loaded in shear. The minimum bond pull limits chart from the MIL-STD is presented in Appendix A, Figure A1, and compared with the wire bond pull testing results. The maximum force was recorded to calculate the maximum

interfacial stress using the measured area of the interconnection. Displacement was also recorded for each test.

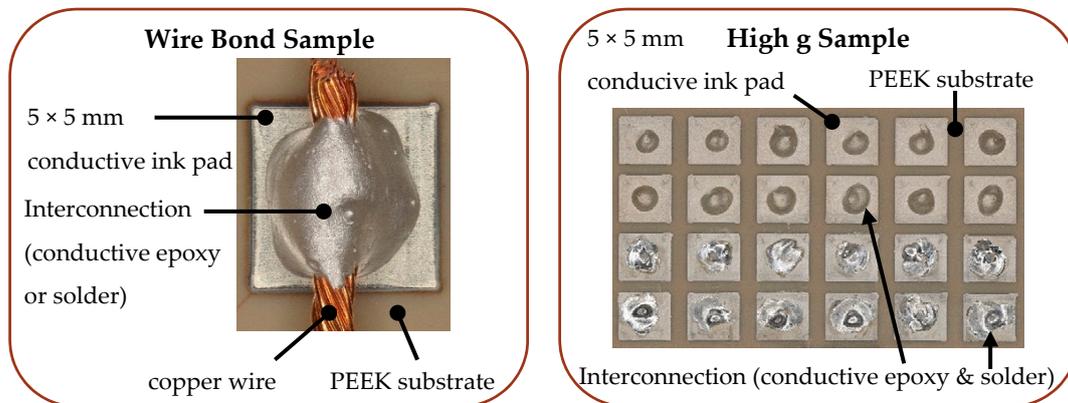


Figure 1. Diagrams of wire bond pull (left) and high g (right) electrical interconnection samples.

The area, volume, and height measurements for the interconnections throughout this work were measured with a Keyence VHX-7100 microscope having an x-y resolution of 2.6 μm and a z-height resolution of 1 μm at a magnification of 40 \times .

Figure 1 also shows a high g sample with a 4 \times 6 array of high g interconnection samples for a total of 24 interconnection samples per 45 \times 30 mm² PEEK substrate. In this case, the top two rows consist of H20E conductive epoxy interconnection samples, while the bottom two rows are low temperature Indium, Inc. solder 97In/3Ag. Two batches were tested for each high g interconnection sample set for a total of 24 high g samples tested for the silver conductive epoxy, while a smaller sample set of six was tested for the copper conductive epoxy.

Figure 2 shows the design of the high g interconnection samples. The PEEK and FR4 substrates were bonded together with epoxy. An electrical pin of 0.8 mm diameter was inserted from the backside of the PEEK substrate into a 0.8 mm hole drilled into both the PEEK and FR4 substrates and designed into the center of the high g testing interconnection pad. The pins were then soldered to the FR4 copper to make a common ground plane on the backside of the sample. After the pins were inserted, the lengths of the pins were cut and lightly sanded to a height of 0.46 \pm 0.02 mm unless otherwise noted as short pins. The short pin samples have a height of 0.24 \pm 0.02 mm. The pins were then interconnected to the printed conductive ink with solder or conductive epoxy to complete fabrication.

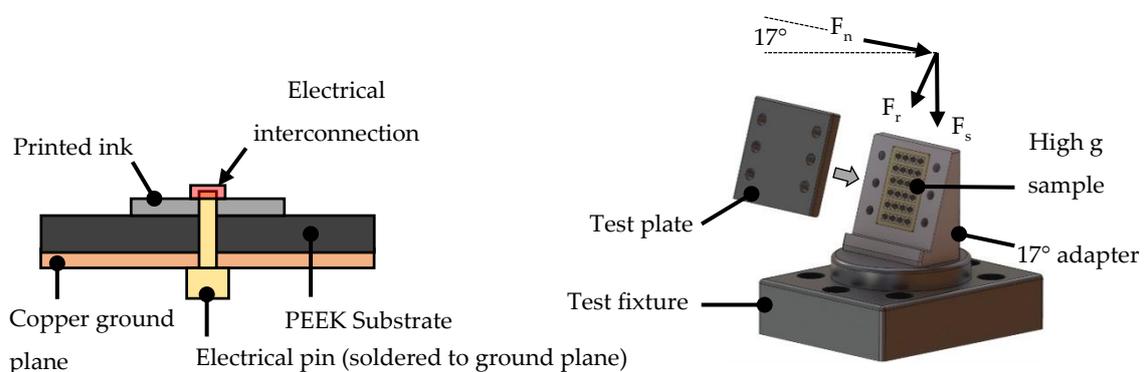


Figure 2. Design of electrical interconnection high g sample (left) and diagram of high g test fixture (right). The resultant impact force (F_r) is a combination of both shear (F_s) and normal (F_n) forces.

High g testing was performed using an MTS drop tower with accelerations up to 50,000 g and a pulse width of 0.1 ms, which fits the profile of MIL STD 883F Method 2002.4 Mechanical Shock Condition F and is more severe than condition G. The acceleration curve can be found in Appendix A as

Figure A2. High g testing was performed at 17° to induce both shear and normal forces, as depicted in Figure 2. The maximum acceleration and pulse width were recorded for each test. The resistance was measured before and after each high g test using a 4-point probing method with two of the electrical leads connected to the common ground plane on the copper side of the FR4 and the other two leads probing the top corners of the printed conductive ink interconnection pad.

3. Results

3.1. Wire Bond Pull Testing

Wire bond pull testing shows H20E conductive epoxy has higher strength than the solders regardless of flux remover method for both inks Tables 2 and 3, and Figure 3. The increased strength of H20E conductive epoxy does become marginal when comparing the solvent-free flux remover solder samples. Additionally, the solvent-free flux remover solder samples show a significant increase in toughness (up to 6×) when comparing the solvent flux remover samples in all cases besides one type of solder (CB230-57Bi/42Sn/1Ag). The reduced toughness of the solvent flux remover samples likely results from the solvent penetrating into the conductive ink and compromising the adhesion between the conductive ink and substrate. In addition, all interconnections for both inks from Tables 2 and 3, and Figure 3 surpass the minimum bond pull limit of the MIL-STD chart from Appendix A in Figure A1.

Table 2. Wire bond pull testing results for silver HPS-FG57B conductive ink.

Interconnection	Solvent Flux Remover			Solvent-Free Flux Remover			T _s /T _f
	Area (mm ²)	Max τ (MPa)	T _s	Area (mm ²)	Max τ (MPa)	T _f	
58Bi/42Sn	23.0 ± 2.9	2.76 ± 0.83	0.56	20.0 ± 1.2	3.31 ± 0.48	0.98	1.74
57Bi/42Sn/1Ag	22.7 ± 2.9	2.85 ± 0.63	0.27	21.6 ± 1.0	3.48 ± 0.56	1.02	3.83
97In/3Ag	22.4 ± 3.7	2.23 ± 0.54	1.05	19.2 ± 2.5	3.00 ± 0.69	4.75	4.52
52In/48Sn	21.7 ± 2.0	2.93 ± 0.58	0.37	23.3 ± 0.9	3.90 ± 0.35	1.59	4.29
H20E	–	–	–	19.36 ± 4.0	4.73 ± 1.06	1.08	–

* Note: T_s = toughness with solvent flux remover. T_f = toughness with solvent-free flux remover. The calculated toughness is the area underneath the stress vs. displacement curve for the representatives in Figure 3 from wire bond pull testing. Note also that this is not a true toughness, since it is calculated based on a stress vs. displacement curve instead of a stress vs. strain curve.

Table 3. Wire bond pull testing results for copper CB230 conductive ink.

Interconnection	Solvent Flux Remover			Solvent-Free Flux Remover			T _s /T _f
	Area (mm ²)	Max τ (MPa)	T _s	Area (mm ²)	Max τ (MPa)	T _f	
58Bi/42Sn	17.8 ± 1.3	2.58 ± 0.41	0.10	13.0 ± 1.6	3.30 ± 0.9	0.66	6.33
57Bi/42Sn/1Ag	19.8 ± 3.1	1.76 ± 0.98	0.34	15.7 ± 0.7	1.39 ± 0.56	0.22	0.65
97In/3Ag	18.2 ± 1.6	3.15 ± 0.46	0.66	15.9 ± 1.2	3.66 ± 0.35	0.93	1.42
52In/48Sn	14.2 ± 1.4	2.56 ± 0.52	0.14	14.3 ± 1.7	2.18 ± 0.30	0.26	1.91
63Sn/37Pb	17.2 ± 1.9	2.54 ± 0.54	0.17	14.0 ± 0.7	3.58 ± 0.22	0.58	3.33
H20E	–	–	–	20.0 ± 6.1	4.59 ± 1.48	0.78	–

* Note: T_s = toughness with solvent flux remover. T_f = toughness with solvent-free flux remover. The calculated toughness is the area underneath the stress vs. displacement curve for the representatives in Figure 3 from wire bond pull testing. Note also that this is not a true toughness, since it is calculated based on a stress vs. displacement curve instead of a stress vs. strain curve.

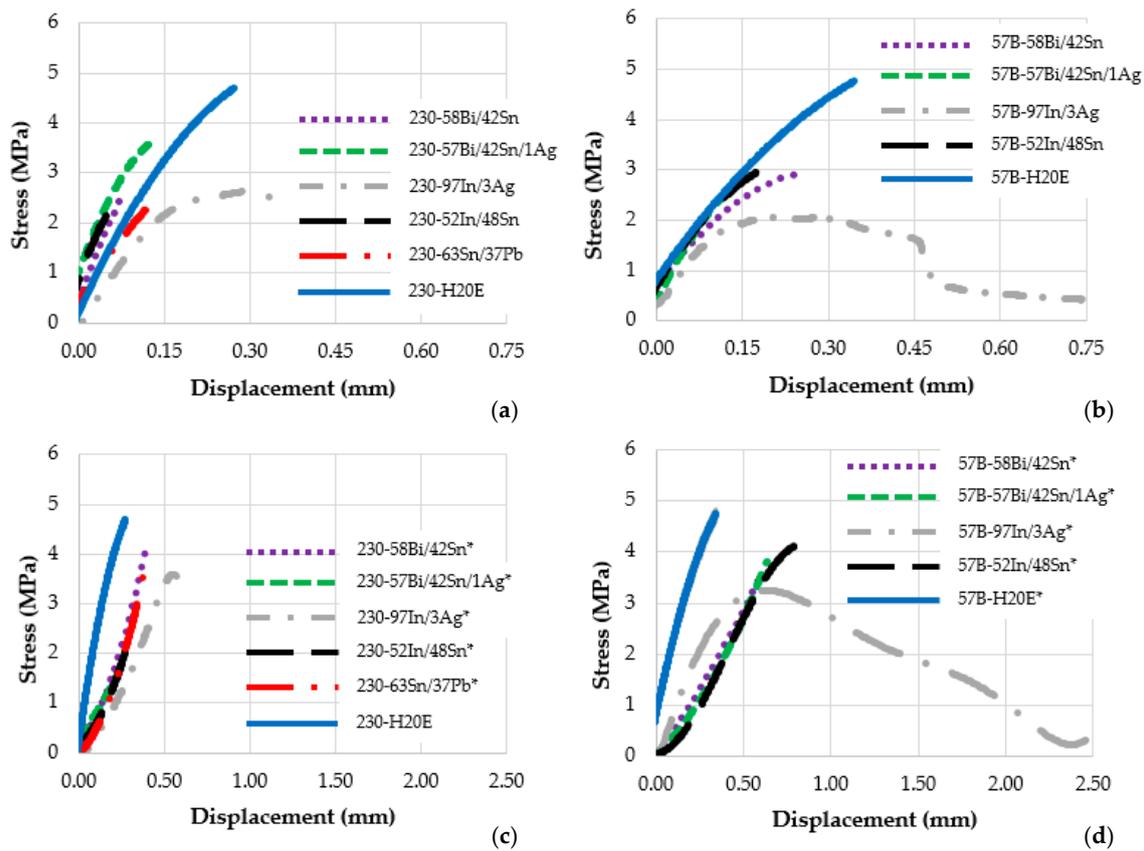


Figure 3. Representation of wire bond pull testing stress vs. displacement curves. (a) CB230 copper conductive ink with solvent flux remover, (b) HPS-FG57B silver conductive ink with solvent flux remover, (c) CB230 copper conductive ink with solvent-free flux remover, and (d) HPS-FG57B silver conductive ink with solvent-free flux remover. Note: the ‘*’ also indicates solvent-free flux remover in (c,d). Toughness was calculated as the area under these curves for a representative toughness to compare the area under the curves quantitatively from the wire bond pull test.

Low temperature solder 97In/3Ag in particular shows high ductility/toughness and the only samples to have a mix of wire pull out and adhesive failure, whereas all other sample types failed adhesively (Figure 4). The significant toughness of solder 97In/3Ag results from having a high composition of indium (97 wt%), which is a soft and ductile metal.

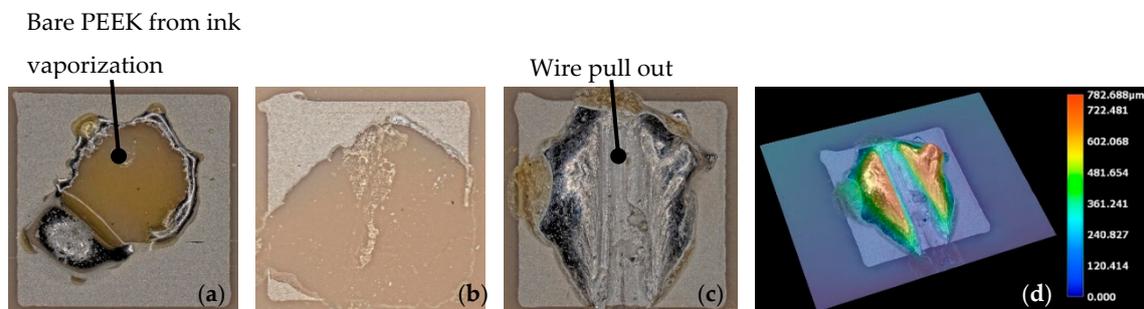


Figure 4. Failure modes of wire bond pull samples. (a) Printed ink vaporization, (b) adhesive failure of conductive ink, (c) wire pull out, (d) wire pull out colormap.

3.1.1. Silver HPS-FG57B Conductive Ink

Silver conductive ink HPS-FG57B shows the local heat input of the low temperature solders is likely also responsible for compromising the adhesion of the conductive ink and the reduced strength of the solders when comparing H20E conductive epoxy. Eutectic 63Sn/37Pb solder, for instance, vaporized HPS-FG57B silver conductive ink (Figure 4) when attempting to solder and did not permit a soldered connection. Therefore, even though the low temperature solders have a much lower soldering iron temperature (Table 1), the local heat input is likely still having an effect on adhesion of the conductive ink to the substrate.

3.1.2. Copper CB230 Conductive Ink

On average, the copper conductive ink CB230 shows marginally lower strength but significantly less toughness than the silver conductive ink HPS-FG57B for the low temperature solder interconnections. This may be due to the presence of intermetallic compounds created when soldering to copper. The formation of the intermetallic compounds has been shown in prior research to embrittle the bond and reduce adhesion [45,48,54,61]. Intermetallic compounds grow with thermal ageing [54].

3.2. High Acceleration Testing

3.2.1. Silver HPS-FG57B Conductive Ink

A down-selection was made after the wire bond pull testing results to focus on a larger sample group of conductive epoxy H20E and low temperature solder 97In/3Ag for silver HPS-FG57B conductive ink, since they showed a relatively high strength interconnection and high ductility interconnection, respectively. Vortex shaking the conductive epoxy was also added to this group to see the effect of increasing the area on high acceleration resilience as it was posited the stresses would be distributed over a larger area and increase the resilience.

Table 4 shows the solder interconnections have larger area, comparable volume, shorter max heights, and lower original resistances (R_0) when comparing H20E as deposited. H20E as deposited also shows a more repeatable deposition with less variation for area measurements in Table 4.

In terms of survivability, both solder 97In/3Ag and H20E as deposited show about 0.5 m Ω resistance change (ΔR) when subjected up to 25,000 g, but then about 40 m Ω with much more variance when subjected up to 50,000 g. The largely increased variance is due to damage of the electrical interconnection between the conductive ink and interconnection, the electrical pin and the interconnection, or both. Solder 97In/3Ag also has 2/24 open circuits, which results from severe damage to the interconnection during exposure to high accelerations. Vortex shaking does result in increased area for both standard and short pin sets, but with marginally increased original resistance and increased change of resistance when exposed to high accelerations. Figure 5 shows undamaged 97In/3Ag and H20E as deposited interconnections; perimeter cracking and ink removal damage that increases resistance and is the onset of more severe damage; complete interconnection and ink removal for severe damage and clear open circuit.

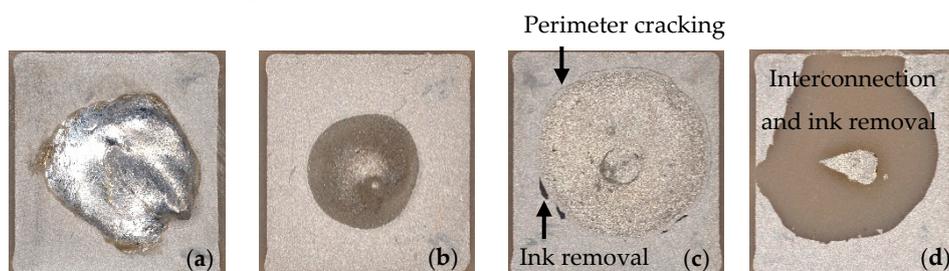


Figure 5. High g testing samples. (a) Intact 97In/3Ag solder interconnection, (b) intact H20E as deposited conductive epoxy interconnection, (c) perimeter cracking and ink removal damage of conductive epoxy interconnection, (d) severe damage and open circuit with complete removal of interconnection.

3.2.2. Copper CB230 Conductive Ink

As for the copper CB230 conductive ink, Table 5 shows the selection of interconnection materials for high acceleration testing based on a broad range of interconnection materials including H20E conductive epoxy, low temperature solders with high weight compositions of indium and bismuth, and the conventional tin-lead solder.

Table 5 shows low temperature solder 97In/3Ag has the best performance when subjected to both 25,000 and 50,000 g for CB230 copper conductive ink, but has significantly more resistance change when comparing HPS-FG57B silver conductive ink and 97In/3Ag interconnections and 2/6 open circuits when subjected to 50,000 g. H20E conductive epoxy also shows similar results for CB230 copper conductive ink. In comparison, low temperature solder 57Bi/42Sn/1Ag and 63Sn/37Pb solder showed increased resistance even when subjected to 25,000 g (Table 5).

Table 4. High g testing results for silver HPS-FG57B conductive ink.

Inter-Connection	Area (mm ²)	Volume (mm ³)	V/A (mm)	Max H (mm)	Ro (mΩ)	25,000 High g		50,000 High g	
						ΔR (mΩ)	OC	ΔR (mΩ)	OC
97In/3Ag	10.36 ± 1.64	2.09 ± 0.59	0.20	0.75 ± 0.17	3.1 ± 1.0	0.4 ± 0.8	0/24	37.5 ± 78.0	2/24
H20E-ad	6.39 ± 0.95	2.56 ± 0.60	0.40	1.05 ± 0.10	8.9 ± 2.0	0.6 ± 0.9	0/24	41.5 ± 105.9	0/24
H20E-v	12.16 ± 1.27	2.41 ± 0.20	0.20	0.53 ± 0.05	10.8 ± 3.1	9.7 ± 23.0	2/24	80.1 ± 154.1	4/24
H20E-v-s	9.62 ± 1.38	1.61 ± 0.23	0.17	0.42 ± 0.03	10.2 ± 2.3	8.9 ± 19.6	0/24	81.9 ± 152.3	8/24

* Note: H20E-ad = H20E as deposited, H20E-v = H20E vortex shaking, and H20E-v-s = H20E vortex shaking with short electrical pins.

Table 5. High g testing results for copper CB230 conductive ink.

Inter-Connection	Area (mm ²)	Volume (mm ³)	V/A (mm)	Max H (mm)	Ro (mΩ)	25,000 High g		50,000 High g	
						ΔR (mΩ)	OC	ΔR (mΩ)	OC
97In/3Ag	9.73 ± 0.66	3.30 ± 0.52	0.34	N/A	1.7 ± 0.4	11.0 ± 2.4	0/6	3000 ± 2000	2/6
H20E	5.02 ± 0.64	1.30 ± 0.13	0.26	N/A	8.3 ± 1.5	122.6 ± 201.8	0/6	9000 ± 4000	2/6
57Bi/42Sn/1Ag	7.14 ± 1.01	2.70 ± 0.58	0.38	N/A	3.9 ± 1.3	91.3 ± 89.9	2/6	20,000 ± 2000	5/6
63Sn/37Pb	7.16 ± 0.25	1.44 ± 0.12	0.20	N/A	2.3 ± 0.2	41.0 ± 25.2	1/6	5000 ± 3000	1/6

4. Discussion

This work shows interconnections for printed electronic elements can achieve survivability when subjected up to 50,000 g. A direct comparison of H20E conductive epoxy and low temperature solder 97In/3Ag from Figure 3, Tables 2 and 3 show H20E has higher strength but is also brittle, while 97In/3Ag has lower strength but greater ductility. These aspects were predicted to show differences during high g survivability testing, but for the most part, both interconnection materials show similar performance, especially for silver HPS-FG57B conductive ink. One aspect that should be acknowledged is the density of these materials. H20E has a measured density of 2.92 ± 0.26 g/cc; meanwhile, the density of all the solders used in this work range from 7.00 to 8.40 g/cc, which is 2.4–2.9× greater than the density of H20E. This implies a tradeoff for high g testing, in which ductile materials would generally be preferred. The reduced density—thus, mass and resulting forces under high g loading—of H20E conductive epoxy allows it to demonstrate adequate survivability up to 50,000 g, even though it is more brittle than 97In/3Ag low temperature solder.

H20E also has less variation for area and volume than many of the solders, which is expected since the conductive epoxy deposition for the high g samples utilizes a pneumatic pick-and-place, while the solder process was manual. Conductive epoxy also nullifies the concern of thermally damaging heat sensitive materials and components when interconnecting printed electronic elements and COTS components. On the other hand, vortex shaking the conductive epoxy after deposition but prior to curing hinders the performance in this work for the high g samples. The vortex shaking may be too aggressive and causing the epoxy to separate from the electrical pin. This creates a less continuous/uniform bond, which explains the increased original resistance when comparing the as deposited conductive epoxy samples. A less continuous/uniform bond between the electrical pin and conductive epoxy results in a weakened interconnection and higher susceptibility to damage when subjected to high accelerations.

In terms of implementing conductive epoxy or low temperature solder into a multi-staged AM process, conductive epoxy may have the advantage. Conductive epoxy can be deposited with a dispensing system in situ during a multi-staged digital manufacturing process. Soldering can be done in a multi-staged manufacturing process as well, but it would require a soldering robot that would be much more expensive. If the multi-tooled AM system was also equipped with an in situ curing tool (photonic curing or lasers), conductive ink deposition, curing, and conductive epoxy deposition could all be done within a single multi-tooled system. Another aspect for electronics that conductive epoxy might edge out solders is harsh environmental temperature cycling. Solders are prone to thermal ageing due to intermetallic compound growth and migration, which will reduce interconnection resiliency when the electronics endure heat cycling from normal operation. Thermal ageing studies for printed electronic interconnections are one area of future work.

The interfacial failure stresses from wire bond pull testing also seem to indicate conductive epoxy may be preferable for printed electronic interconnections. All of the wire bond pull test samples failed adhesively besides the mixed failure of ductile 97In/3Ag low temperature solder with wire pull out failure. However, Tables 2 and 3 show even the solder interconnections failed adhesively at a lower maximum interfacial stress than conductive epoxy. This implies the thermal input from the solder process affects the bond of the conductive ink to the substrate, even if the ink is not vaporized or showing obvious observable damage due to the polymer particles anchoring the colloidal conductive ink being deteriorated by the thermal input.

It is also noteworthy that different substrates/conductive inks or surface treatments will have different surface interactions that may improve adhesion of the conductive ink–substrate bond and allow increased interconnection strength. This work shows different performance requirements/material systems will influence the selection of interconnection materials for stable electrical joints. For instance, a low temperature substrate and conductive ink subjected to high accelerations with little deformation may benefit more utilizing conductive epoxy as the interconnection material, whereas a high

temperature substrate and conductive ink subjected to large deformations may benefit more from a solder with a high weight % of indium.

The silver conductive ink in this work shows superior performance compared to the copper conductive ink. It shows similar maximum interfacial stresses but greater toughness from wire bond pull testing and greater survivability during high g testing. Low temperature solders form intermetallic compounds during the soldering process and these compounds embrittle the interconnection when bonding to copper. Silver conductive ink and conductive epoxy may likely be the best selection for printed electronic and interconnection materials as they show adequate survivability up to 50,000 g of high acceleration exposure and do not have the formation of intermetallic compounds, like solders, that may affect electronics performance when heat cycling in normal operation. Additionally, wire bond pull testing of solders delineates an inexpensive and sufficient method to quickly screen soldering materials for printed electronics interconnections for high acceleration survivability. In this work, wire bond pull testing shows the greater the ductility of a soldered interconnection, the greater the resilience it has to high accelerations. In addition, these planar results should be translatable to true 3D structures, as the results are based on material properties including density, thermal resilience, and adhesion as opposed to geometry.

5. Conclusions

As a result of this research, the designs and procedures to evaluate interconnections for hybridized printed electronics were developed. For the particular materials studied here (i.e., PEEK substrate, printed silver or copper conductive ink, conductive epoxy or low temperature solders), both conductive epoxy and low temperature solder exemplify an effective interconnection for printed electronics applications when subjected up to 50,000 g of mechanical acceleration. However, wire bond pull testing demonstrates that conductive epoxy has higher maximum interfacial stress, but it is more brittle than the low temperature solders. Low temperature solder 97In/3Ag shows high ductility—as expected, with a high weight composition of soft and ductile indium—and the only interconnection material to have mixed failure with wire pullout. High acceleration testing shows both H20E conductive epoxy and 97In/3Ag low temperature solder survive harsh environments with ~40 mΩ of resistance change when exposed to up to 50,000 g on silver conductive ink.

The results indicate conductive epoxy may be a more robust interconnection for resilient printed electronics, primarily due to its low mass yet high strength, even though it is relatively brittle. Additionally, conductive epoxy may be more preferential for printed electronic applications as it is: (1) more feasible to integrate into a multi-tooled AM process, (2) does not have the potential for formation of intermetallic compounds that could embrittle/weaken the interconnection during thermal cycling from normal electronics operation, and (3) is less dense and therefore has reduced mass and resulting forces when subjected to high accelerations, which overcomes the brittle nature of the conductive epoxy. In addition, when soldering to a conductive ink, a solvent-free flux remover method should be utilized, as a flux remover with solvent(s) has a deleterious effect on the adhesion of the conductive ink. Silver conductive inks show better performance than copper conductive inks when soldering, as the formation of intermetallic compounds leads to an embrittled interconnection. In conclusion, these results begin to fill the gap in the literature to elucidate the most effective interconnections for hybridized printed electronics when subjected to harsh environments, and in doing so, propel the production of next generation electronics technologies for the most demanding environments.

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Appendix A

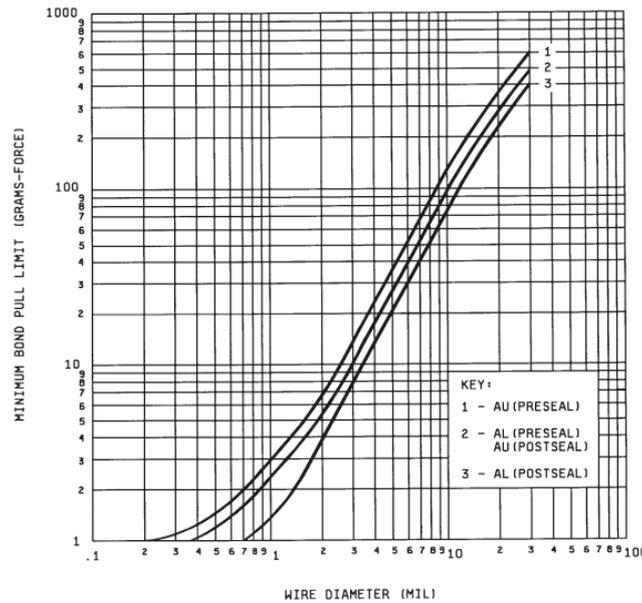


Figure A1. MIL-STD-883F Method 2011.7 Bond Strength (Destructive Bond Pull Test) minimum bond pull limits chart. Note wire diameter in this work was 32 mil (0.81 mm), which corresponds to a minimum bond pull limit of 6000 g-force. Even the weakest interfacial shear strength from Table 3 (1.39 ± 0.56 MPa for CB230-57Bi/42Sn/1Ag solvent-free) has a bond strength of 2260 g-force, which surpasses the minimum bond pull limit.

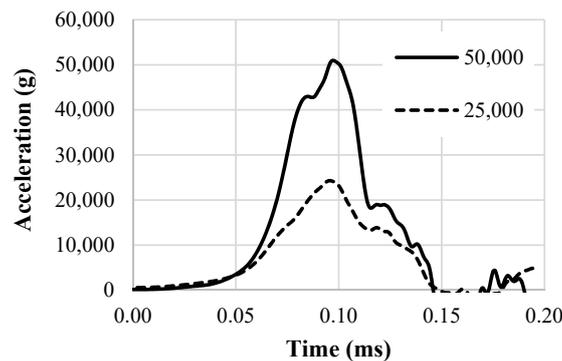


Figure A2. Acceleration curves from high g testing.

References

1. Church, K.H.; Crane, N.B.; Deffanbaugh, P.I.; Ketterl, T.P.; Neff, C.G.; Nesbitt, P.B.; Nussbaum, J.T.; Perkowski, C.; Tsang, H.; Castro, J.; et al. Multimaterial and multilayer direct digital manufacturing of 3D structural microwave electronics. *Proc. IEEE* **2017**, *105*, 688–701. [[CrossRef](#)]
2. Dickey, M.D.; Cormier, D.; Parekh, D.P. *Additive Manufacturing: Ch.8 Multifunctional Printing: Incorporating Electronics into 3D Parts Made by Additive Manufacturing*; CRC Press: Boca Raton, FL, USA, 2015.

3. Neff, C.; Crane, N.B.; Deffenbaugh, P.I.; Zunino, J.L.; Church, K.H.; Newton, M. Digital Manufacturing and Performance Testing for Military Grade Application Specific Electronic Packaging (ASEP). In Proceedings of the International Microelectronics Assembly and Packaging Society, Pasadena, CA, USA, 11–13 October 2016.
4. Rojas-Nastrucci, E.A.; Tsang, H.; Deffenbaugh, P.I.; Ramirez, R.A.; Hawatmeh, D.; Ross, A.; Church, K.; Weller, T.M. Characterization and Modeling of K-Band Coplanar Waveguides Digitally Manufactured using Pulsed Picosecond Laser Machining of Thick-Film Conductive Paste. *IEEE Trans. Microw. Theory Tech.* **2017**, *65*, 3180–3187. [[CrossRef](#)]
5. Beedasy, V.; Smith, P.J. Printed Electronics as Prepared by Inkjet Printing. *Materials* **2020**, *13*, 704. [[CrossRef](#)]
6. Liu, S.; Li, Y.; Xing, S.; Liu, L.; Zou, G.; Zhang, P. Structure Inheritance in Nanoparticle Ink Direct-Writing Processes and Crack-Free Nano-Copper Interconnects Printed by a Single-Run Approach. *Materials* **2019**, *12*, 1559. [[CrossRef](#)] [[PubMed](#)]
7. Cui, Z. *Printed Electronics: Materials, Technologies, & Applications*; John Wiley & Sons: Singapore, 2016.
8. LaPedus, M. EUV Tool Costs Hit \$120 Million. *EETimes*, AspenCore, 19 November 2010. Available online: www.eetimes.com/euv-tool-costs-hit-120-million/# (accessed on 8 May 2020).
9. Zant, P.V. *Microchip Fabrication*, 5th ed.; McGraw-Hill: New York, NY, USA, 2004.
10. Berman, B. 3-D printing: The new industrial revolution. *Bus. Horiz.* **2012**, *55*, 155–162. [[CrossRef](#)]
11. Espalin, D.; Muse, D.W.; MacDonald, E.; Wicker, R.B. 3D Printing multifunctionality: Structures with electronics. *Int. J. Adv. Manuf. Technol.* **2014**, *72*, 963–978. [[CrossRef](#)]
12. Ford, S.; Despeisse, M. Additive manufacturing and sustainability: An exploratory study of the advantages and challenges. *J. Clean. Prod.* **2016**, *137*, 1573–1587. [[CrossRef](#)]
13. Huang, S.H.; Liu, P.; Mokasdar, A.; Hou, L. Additive manufacturing and its societal impact: A literature review. *Int. J. Adv. Manuf. Technol.* **2013**, *67*, 1191–1203. [[CrossRef](#)]
14. Roberson, D.A.; Wicker, R.B.; Murr, L.E.; Church, K.; MacDonald, E. Microstructural and Process Characterization of Conductive Traces Printed from Ag Particulate Inks. *Materials* **2011**, *4*, 963–979. [[CrossRef](#)]
15. MacDonald, E.; Salas, R.; Espalin, D.; Perez, M.; Aguilera, E.; Muse, D.; Wicker, R.B. 3D Printing for the Rapid Prototyping of Structural Electronics. *IEEE* **2014**, *2*, 234–242. [[CrossRef](#)]
16. MacDonald, E.; Wicker, R.B.; Lopes, A.J. Integrating stereolithography and direct print technologies for 3D structural electronics fabrication. *Rapid Prototyp. J.* **2012**, *18*, 129–143.
17. Olivas, R.; Salas, R.; Muse, D.; MacDonald, E.; Wicker, R.; Newton, M.; Church, K. Structural Electronics through Additive Manufacturing and Micro-Dispensing. *Int. Symp. Microelectron.* **2010**, *2010*, 000940–000946. [[CrossRef](#)]
18. Mejias-Morillo, C.R.; Gbaguidi, A.; Kim, D.W.; Namilae, S.; Rojas-Nastrucci, E.A. UHF RFID-based Additively Manufactured Passive Wireless Sensor for Detecting Micrometeoroid and Orbital Debris Impacts. In Proceedings of the 2019 IEEE International Conference on Wireless for Space and Extreme Environments (WiSEE), Ottawa, ON, Canada, 16–18 October 2019.
19. Mejias-Morillo, C.R.; Rojas-Nastrucci, E.A. Z-Meandering Miniaturized Patch Antenna Using Additive Manufacturing. In Proceedings of the 2020 IEEE Radio and Wireless Symposium (RWS), San Antonio, TX, USA, 26–29 January 2020.
20. Adams, J.J.; Duoss, E.B.; Malkowski, T.F.; Motala, M.J.; Ahn, B.Y.; Nuzzo, R.G.; Bernhard, J.T.; Lewis, J.A. Conformal printing of electrically small antennas on three-dimensional surfaces. *Adv. Mater.* **2011**, *23*, 1335–1340. [[CrossRef](#)] [[PubMed](#)]
21. Arnal, N.; Ketterl, T.; Vega, Y.; Stratton, J.; Perkowski, C.; Deffenbaugh, P.; Church, K.; Weller, T.M. 3D Multi-Layer Additive Manufacturing of a 2.45 GHz RF Front End. In Proceedings of the 2015 IEEE MTT-S International Microwave Symposium, Phoenix, AZ, USA, 17–22 May 2015.
22. Church, K.H.; Chen, X.; Goldfarb, J.M.; Perkowski, C.W.; LeBlanc, S. Advanced Printing for Microelectronic Packaging. In Proceedings of the IPC APEX EXPO Conference Proceedings, Las Vegas, NV, USA, 23–27 March 2014.
23. Deffenbaugh, P.; Church, K.; Goldfarb, J.; Chen, X. Fully 3D Printed 2.4 GHz Bluetooth/Wi-Fi Antenna. *Int. Symp. Microelectron.* **2013**, *2013*, 000914–000920. [[CrossRef](#)]
24. Ketterl, T.P.; Vega, Y.; Arnal, N.C.; Stratton, J.W.I.; Rojas-Nastrucci, E.A.; Cordoba-Erazo, M.F.; Abdin, M.M.; Perkowski, C.W.; Deffenbaugh, P.I.; Church, K.H.; et al. A 2.45 GHz Phased Array Antenna Unit Cell Fabricated Using 3-D Multi-Layer Direct Digital Manufacturing. *IEEE Trans. Microw. Theory Tech.* **2015**, *63*, 4382–4394. [[CrossRef](#)]

25. Nassar, I.; Tsang, H.; Weller, T.M. 3D printed wideband harmonic transceiver for embedded passive wireless monitoring. *Electron. Lett.* **2014**, *50*, 1609–1611. [[CrossRef](#)]
26. Ramirez, R.A.; Rojas-Nastrucci, E.A.; Weller, T.M. 3D tag with improved read range for UHF RFID applications using additive manufacturing. In Proceedings of the 2015 IEEE 16th Annual Wireless and Microwave Technology Conference (WAMICON), Cocoa Beach, FL, USA, 13–15 April 2015.
27. Rojas-Nastrucci, E.A.; Ramirez, R.; Hawatmeh, D.; Lan, D.; Wang, J.; Weller, T. Laser enhanced direct print additive manufacturing for mm-wave components and packaging. In Proceedings of the 2017 International Conference on Electromagnetics in Advanced Applications (ICEAA), Verona, Italy, 11–15 September 2017.
28. Rojas-Nastrucci, E.A.; Ramirez, R.A.; Weller, T.M. Direct digital manufacturing of mm-wave vertical interconnects. In Proceedings of the 2018 IEEE 19th Wireless and Microwave Technology Conference (WAMICON), Clearwater, FL, USA, 9–10 April 2018.
29. Ramirez, R.; Rojas-Nastrucci, E.A.; Weller, T. Laser-Assisted Additive Manufacturing of mm-Wave Lumped Passive Elements. *IEEE Trans. Microw. Theory Tech.* **2018**, *66*, 5462–5471. [[CrossRef](#)]
30. Koshi, T.; Nomura, K.; Yoshida, M. Electronic Component Mounting for Durable E-Textiles: Direct Soldering of Components onto Textile-Based Deeply Permeated Conductive Patterns. *Micromachines* **2020**, *11*, 209. [[CrossRef](#)]
31. Guan, X.; Cao, L.; Huang, Q.; Kong, D.; Zhang, P.; Lin, H.; Li, W.; Lin, Z.; Yuan, H. Direct Writing Supercapacitors Using a Carbon Nanotube/Ag Nanoparticle-Based Ink on Cellulose Acetate Membrane Paper. *Polymers* **2019**, *11*, 973. [[CrossRef](#)]
32. Andersson, H.A.; Manuilskiy, A.; Haller, S.; Hummelgård, M.; Sidén, J.; Hummelgård, C.; Olin, H.; Nilsson, H.-E. Assembling surface mounted components on ink-jet printed double sided paper circuit board. *Nanotechnology* **2014**, *25*, 094002. [[CrossRef](#)]
33. Basaran, C.; Tang, H.; Dishongh, T.; Searls, D. Computer Simulations of Solder Joint Reliability Tests. *Electron. Packag. Lab. Adv. Packag.* **2001**, *1*, 17–22.
34. Johnson, R.W. Extreme temperature packaging: Challenges and opportunities. In Proceedings of the SPIE 9836, Micro- and Nanotechnology Sensors, Systems, and Applications VIII, Baltimore, MD, USA, 17–21 April 2016; p. 98360L.
35. Bai, G. Low-Temperature Sintering of Nanoscale Silver Paste for Semiconductor Device Interconnection. Ph.D. Thesis, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, 2005.
36. Berry, D.; Jiang, L.; Yunhui, M.; Luo, S.; Ngo, K.; Lu, G. Packaging of high-temperature planar power modules interconnected by low-temperature sintering of nanosilver paste. In Proceedings of the 2014 International Conference on Electronics Packaging (ICEP), Toyama, Japan, 23–25 April 2014.
37. Jang, K.-S.; Eom, Y.-S.; Choi, K.-S.; Bae, H.-C. Crosslinkable deoxidizing hybrid adhesive of epoxy–diacid for electrical interconnections in semiconductor packaging. *Polym. Int.* **2018**, *67*, 1241–1247. [[CrossRef](#)]
38. Lei, T.G.; Calata, J.; Luo, S.F.; Lu, G.Q.; Chen, X. Low-Temperature Sintering of Nanoscale Silver Paste for Large-Area Joints in Power Electronics Modules. *Key Eng. Mater.* **2007**, *353–358*, 2948–2953. [[CrossRef](#)]
39. Lu, G.; Calata, J.N.; Lei, T.G. Low-Temperature Sintering of Nanoscale Silver Paste for Power Chip Attachment. In Proceedings of the 5th International Conference on Integrated Power Electronics Systems, Nuremberg, Germany, 11–13 March 2008.
40. Sancaktar, E.; Bai, L. Electrically Conductive Epoxy Adhesives. *Polymers* **2011**, *3*, 427–466. [[CrossRef](#)]
41. Arrese, J.; Vescio, G.; Xuriguera, E.; Medina-Rodriguez, B.; Cornet, A.; Cirera, A. Flexible hybrid circuit fully inkjet-printed: Surface mount devices assembled by silver nanoparticles-based inkjet ink. *J. Appl. Phys.* **2017**, *121*, 104904. [[CrossRef](#)]
42. Li, X.; Sidén, J.; Andersson, H.; Sawatdee, A.; Öhman, R.; Eriksson, J.; Genchel, T. Enabling paper-based flexible circuits with aluminium and copper conductors. *Flex. Print. Electron.* **2019**, *4*, 045007. [[CrossRef](#)]
43. Neff, C.; Elston, E.; Burfeindt, M.; Crane, N.; Schrand, A. A fundamental study of printed ink resiliency for harsh mechanical and thermal environmental applications. *Addit. Manuf.* **2018**, *20*, 156–163. [[CrossRef](#)]
44. Rasul, J.S. Chip on paper technology utilizing anisotropically conductive adhesive for smart label applications. *Microelectron. Reliab.* **2004**, *44*, 135–140. [[CrossRef](#)]
45. Wu, A.T.; Chen, C.; Huang, J.; Chiang, J.; Wang, C. Development of low temperature solder alloys for advanced electronic packaging: Assessment of In-Bi alloys on Cu substrates. In Proceedings of the 2018 International Conference on Electronics Packaging and iMAPS All Asia Conference (ICEP-IAAC), Mie, Japan, 17–21 April 2018.

46. Bagrets, N.; Barth, C.; Weiss, K. Low Temperature Thermal and Thermo-Mechanical Properties of Soft Solders for Superconducting Applications. *IEEE Trans. Appl. Supercond.* **2014**, *24*, 1–3. [[CrossRef](#)]
47. Mei, Z.; Hua, F.; Glazer, J.; Key, C.C. Low temperature soldering. In Proceedings of the Twenty First IEEE/CPMT International Electronics Manufacturing Technology Symposium Proceedings 1997 IEMT Symposium, Austin, TX, USA, 13–15 October 1997.
48. Ren, G.; Wilding, I.J.; Collins, M.N. Alloying influences on low melt temperature SnZn and SnBi solder alloys for electronic interconnections. *J. Alloy. Compd.* **2016**, *665*, 251–260. [[CrossRef](#)]
49. Sahasrabudhe, S.; Mokler, S.; Renavikar, M.; Sane, S.; Byrd, K.; Brigham, E.; Jin, O.; Goonetilleke, P.; Badwe, N.; Parupalli, S. Low Temperature Solder—A Breakthrough Technology for Surface Mounted Devices. In Proceedings of the 2018 IEEE 68th Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 29 May–1 June 2018.
50. Song, R.-W.; Chou, T.-T.; Fleshman, C.J.; Chen, H.; Duh, J.-G. The Architecture Design and Novel Material Selection for Improved Reliability of Solder Interconnections in Microelectronic Packaging. *ECS Trans.* **2019**, *90*, 35–40. [[CrossRef](#)]
51. Yang, C.-H.; Zhou, S.; Lin, S.-K.; Nishikawa, H. A Computational Thermodynamics-Assisted Development of Sn-Bi-In-Ga Quaternary Alloys as Low-Temperature Pb-Free Solders. *Materials* **2019**, *12*, 631. [[CrossRef](#)]
52. Kim, K.-S.; Imanishi, T.; Suganuma, K.; Ueshima, M.; Kato, R. Properties of low temperature Sn–Ag–Bi–In solder systems. *Microelectron. Reliab.* **2007**, *47*, 1113–1119. [[CrossRef](#)]
53. Li, Q.; Lei, Y.; Lin, J.; Yang, S. Design and properties of Sn-Bi-In low-temperature solders. In Proceedings of the 2015 16th International Conference on Electronic Packaging Technology (ICEPT), Changsha, China, 11–14 August 2015.
54. Liu, P.L.; Shang, J.K. Interfacial embrittlement by bismuth segregation in copper/tin–bismuth Pb-free solder interconnect. *J. Mater. Res.* **2011**, *16*, 1651–1659. [[CrossRef](#)]
55. Nivelles, P.; Borgers, T.; Voroshazi, E.; Poortmans, J.; Haen, J.D.; Ceuninck, W.D.; Daenen, M. Mechanical and chemical adhesion at the encapsulant interfaces in laminated photovoltaic modules. In Proceedings of the 2018 IEEE International Reliability Physics Symposium (IRPS), Burlingame, CA, USA, 11–15 March 2018.
56. Ribas, M.; Chegudi, S.; Kumar, A.; Pandher, R.; Raut, R.; Mukherjee, S.; Sarkar, S.; Singh, B. Thermal and mechanical reliability of low-temperature solder alloys for handheld devices. In Proceedings of the 2014 IEEE 16th Electronics Packaging Technology Conference (EPTC), Singapore, 3–5 December 2014.
57. Un-Byoung, K.; Young-Ho, K. Electrical characteristics of fine pitch flip chip solder joints fabricated using low temperature solders. In Proceedings of the 2004 Proceedings. 54th Electronic Components and Technology Conference (IEEE Cat. No.04CH37546), Las Vegas, NV, USA, 4 June 2004.
58. Bai, H.; Xu, F.; Sha, W.; Chen, D.; Yan, J.; Gan, Y. Phase Structure, Microstructure and Properties of Sn-Bi-Ag Solder Alloy in Ternary System. *Rare Met.* **2019**. [[CrossRef](#)]
59. Mei, Z.; Holder, H.A.; Gleason, J.; Baker, J. Low-temperature solders. In Proceedings of the Electronic Materials and Processing Symposium, Los Angeles, CA, USA, 13–18 November 1994.
60. Made, R.I.; Gan, C.L.; Yan, L.L.; Yu, A.; Yoon, S.W.; Lau, J.H.; Lee, C. Study of Low-Temperature Thermocompression Bonding in Ag-In Solder for Packaging Applications. *J. Electron. Mater.* **2008**, *38*, 365. [[CrossRef](#)]
61. Sung, Y.G.; Myung, W.R.; Jeong, H.; Ko, M.K.; Moon, J.; Jung, S.B. Mechanical Reliability of the Epoxy Sn-58wt.%Bi Solder Joints with Different Surface Finishes Under Thermal Shock. *J. Electron. Mater.* **2018**, *47*, 4165–4169. [[CrossRef](#)]

