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Parametric Design of an LCL Filter for Harmonic Suppression in a Three-Phase Grid-Connected Fifteen-Level CHB Inverter

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Abstract

With the increasing integration of renewable energy sources into the grid, power quality at the point of common coupling (PCC)—particularly harmonic distortion introduced by power electronic converters—has become a critical concern. This paper presents a rigorous design and evaluation of a three-phase, fifteen-level cascaded H-bridge multilevel inverter (CHB MLI) with an LCL filter, selected for its superior harmonic attenuation, compact size, and cost-effectiveness compared to conventional passive filters. The proposed system employs Phase-Shifted Pulse Width Modulation (PS PWM) for balanced operation and low output distortion. A systematic, reproducible methodology is used to design the LCL filter, which is then tested across a wide range of switching frequencies (1–5 kHz) and grid impedance ratios (X/R = 2–9) in MATLAB/Simulink R2025a. Comprehensive simulations confirm that the filter effectively reduces both voltage and current total harmonic distortion (THD) to levels well below the 5% limit specified by IEEE 519, with optimal performance (0.53% current THD, 0.69% voltage THD) achieved at 3 kHz and X/R ≈ 5.6. The filter demonstrates robust performance regardless of grid conditions, making it a practical and scalable solution for modern renewable energy integration. These results, further supported by parametric validation and clear design guidelines, provide actionable insights for academic research and industrial deployment.

Keywords: multilevel inverter (MLI); cascaded H bridge (CHB); renewable energy source (RES); point of common coupling (PCC); total harmonic distortions (THDs); pulse width modulation (PWM)

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1. Introduction

In the modern era, there is an increasing interest in the production and the use of energy around the world. Pakistan is also putting a lot of effort towards the production of energy through smart methods. Among the different sources of energy such as fossil fuels, biogas, and nuclear energy, Renewable Energy Sources (RESs) are considered the best option [1–3], contributing towards Sustainable Energy Sources (SESs). RESs like biomass, solar, hydro, wind, etc., are gaining popularity due to the following reasons.

- Accessibility.
- Lower cost.
- Environmentally friendly.

Wind and photovoltaic (PV) systems are leading examples of SESs extensively employed for electrical energy generation. Their appeal lies in their free and abundant availability [2]. Significant research is dedicated to efficiently converting these renewable sources into electrical power [4–6] for direct delivery to loads or grid integration. The growing utilization of RESs inherently increases the demand for power electronic converters [7,8]. These versatile converters handle various conversions (DC-DC, AC-AC, AC-DC, DC-AC) [9–14]. Specifically, different inverter topologies are vital for interfacing RESs with the grid [12,13]. Comparing conventional inverters with multilevel inverters (MLIs), the latter are preferred due to distinct advantages, including lower switching losses, reduced voltage stress, and improved electromagnetic interference characteristics [15,16]. This makes MLIs increasingly prominent for high-power and high-voltage applications [17]. The three primary categories of MLI topologies are diode-clamped (neutral-clamped), flying capacitor, and cascaded H-bridge (CHB). A drawback specific to the diode-clamped MLI is the need for diodes rated at different voltage levels [18].

Cascaded H-bridge (CHB) MLI is often preferred over Flying Capacitor (FC) and Diode Clamped (DC) MLIs due to several advantages. Unlike FC MLIs, which use bulky and expensive capacitors, or DC MLIs, which require clamping diodes [19], CHB eliminates the need for both. This simplification contributes to CHB's primary benefits: ease of control, high reliability, and inherent modularity. Moreover, CHB requires the fewest semiconductor devices to achieve a desired voltage level, which translates to a lower overall cost, reduced power losses, and consequently, improved efficiency. The principal drawback of the CHB technique, however, is the necessity for an independent DC source for every H-bridge module [20]. The increasing integration of RESs near consumption points helps minimize losses associated with long transmission lines. This trend places greater focus on the distribution segment of the power system, which is critical for overall reliability and efficiency [21–24]. However, grid-connected systems operating within this segment are susceptible to undesirable disturbances at the point of common coupling (PCC), leading to voltage fluctuations and waveform distortions. Modern power systems are also becoming more sensitive due to the proliferation of electronic switching devices and controllers. To effectively interface renewable sources with the grid and mitigate these issues, grid-connected inverters, such as MLIs, are commonly used. These inverters rely on controllers that process feedback from their terminals to regulate desired output variables (voltage, current, power, DC voltage, etc.) [21,25]. This work implements a fifteen-level CHB MLI in MATLAB. For control, a Proportional–Integral (PI) controller is utilized to achieve zero steady-state error, with its proportional and integral gains tuned for optimal performance [26]. The gating signals for the MLI switches are generated by a modulator, which compares the reference signals from the controller with carrier signals. In high-power PV applications, power loss is a significant concern. Sinusoidal Pulse Width Modulation (SPWM) techniques are employed to minimize these losses, particularly switching losses, offering advantages such as low harmonics and better output voltage quality. SPWM methods are broadly classified into single-carrier and multicarrier techniques. Multicarrier PWM is particularly useful for regulating output voltages and reducing THD [27–30]. Among multicarrier methods, Phase-Shifted (PS) PWM is advantageous over Level-Shifted (LS) PWM because it promotes even power distribution [31–33]. The research detailed here involves simulating the Phase-Shifted Pulse Width Modulation (PS PWM) method within the MATLAB environment for a three-phase grid-connected inverter featuring a fifteen-level CHB architecture. Grid-interfaced inverters

naturally introduce harmonic content through the process of Pulse Width Modulation switching, thus requiring a low-pass power filter (LPF) positioned between the inverter and the utility grid to attain the desired quality of output power. Passive filters (PFs) are frequently utilized for this function, primarily due to their economic advantages, and they prove effective in mitigating harmonics at the point of common coupling (PCC). Typical arrangements for passive filters comprise the L (first order), LC (second order), and LCL (third order) filter configurations. The L filter, which is composed solely of an inductor, is straightforward in its design and suitable for low-power converters operating at high switching frequencies, yet it encounters difficulties with resonance and applications requiring higher power levels. The LC filter, which incorporates both an inductor and a capacitor, offers enhanced damping relative to the L filter and possesses a comparatively simple design, though its resonance frequency is impacted by the grid impedance once connected [34]. Designing it requires balancing the values of inductance and capacitance; increasing the capacitance can improve the voltage quality, while inductance is adjusted to achieve the necessary cutoff frequency. The LCL filter, although not optimal for operation at low switching frequencies, effectively isolates the system from the grid impedance and achieves substantial reduction in harmonics using smaller inductance values compared to either L or LC filters [35,36]. Significant levels of harmonic distortion and drops in voltage can cause serious deterioration in performance and potentially lead to the power system shutting down. Therefore, this investigation focuses on designing a particular LCL filter aimed at minimizing these harmonic distortions present at the output of the MLI, thereby producing an output waveform that is nearly sinusoidal and enhancing overall system performance. The study additionally investigates how varying switching frequencies and differing grid characteristics (categorized as weak grids with a high X/R ratio versus strong grids with a low X/R ratio [37]) influence the effectiveness of harmonic filtering. Figure 1 illustrates the schematic representation of the system connected to the grid.

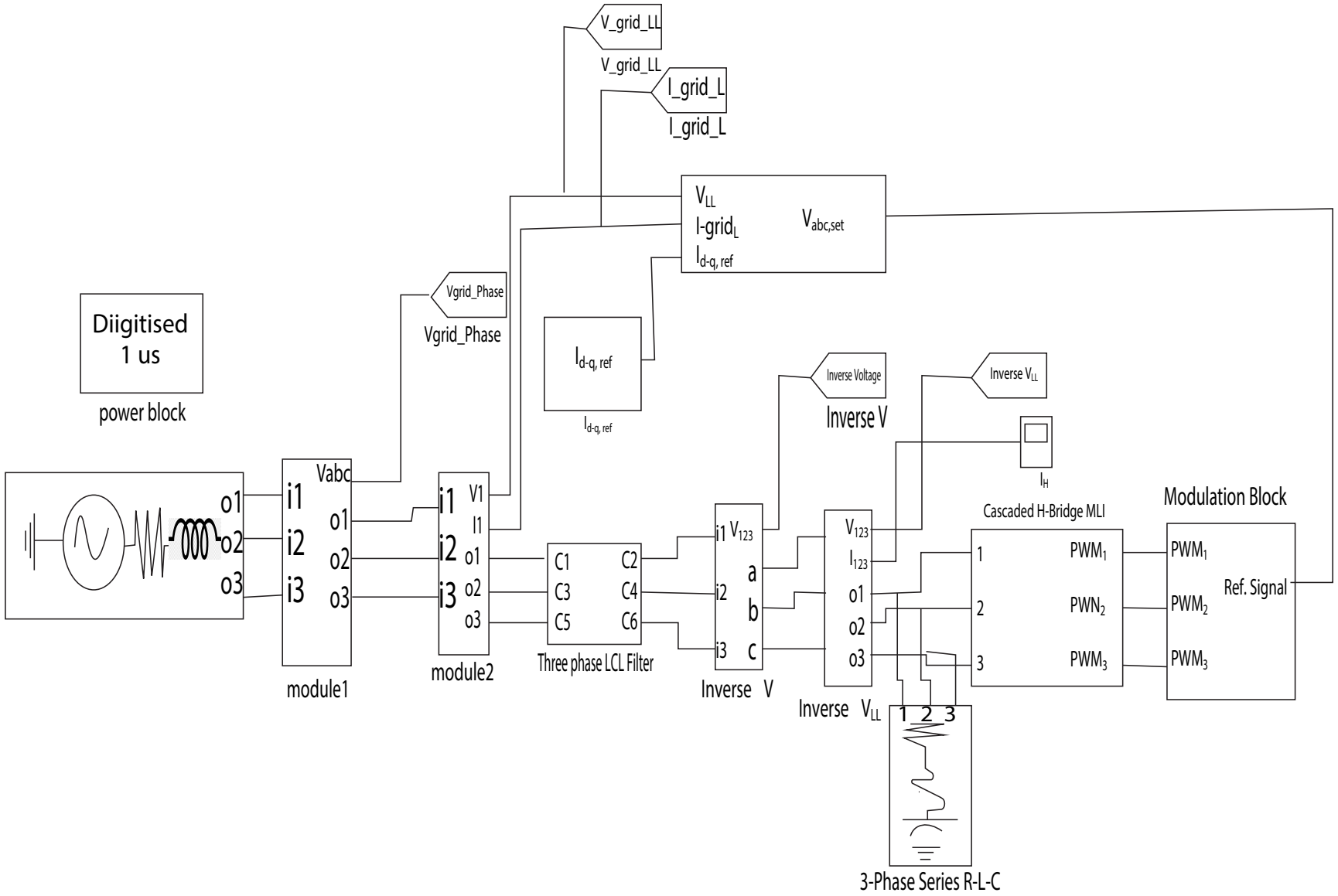


Figure 1. Three-phase grid-connected inverter with LCL filter.

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2. System Architecture

The MATLAB implementation of the system model for a three-phase, fifteen-level CHB grid-tied MLI is shown in Figure 1.

2.1. Fifteen-Level CHB MLI

In this paper, the three-phase fifteen-level CHB MLI is implemented on MATLAB as shown in Figure 2. Consisting of seven series-connected submodules per phase, the CHB MLI simulated here generates fifteen output voltage levels, calculated as (2 * number of submodules) + 1. Each submodule is based on a universal bridge containing a four-switch H-bridge. Switch gate signals originate from a modulation block, and the DC input voltage for each submodule is determined by the following equation. For

U = DC voltage,
V_p = peak AC voltage, and
k = scaling factor (number of submodules per phase in the cascaded H-bridge multilevel inverter)

The relationship between these variables is given by

$$U = \frac{V_p}{k}$$

If the peak AC voltage V_p is expressed in terms of the RMS AC voltage V_{rms}, then

$$V_p = \sqrt{2} \times V_{rms}.$$

Substituting this into the equation for U gives

$$U = \frac{\sqrt{2} \times V_{rms}}{k} \quad (1)$$

In other words,

$$U = \frac{V}{k}\left(\frac{2}{3}\right)^{1/2} \quad (2)$$

In addition to the MATLAB/Simulink simulation setup shown in Figure 2, the equivalent single-phase circuit diagram depicted in Figure 3 provides a concrete visualization of the seven series-connected H-bridge submodules per phase that generate the fifteen voltage levels used in the multilevel inverter topology.

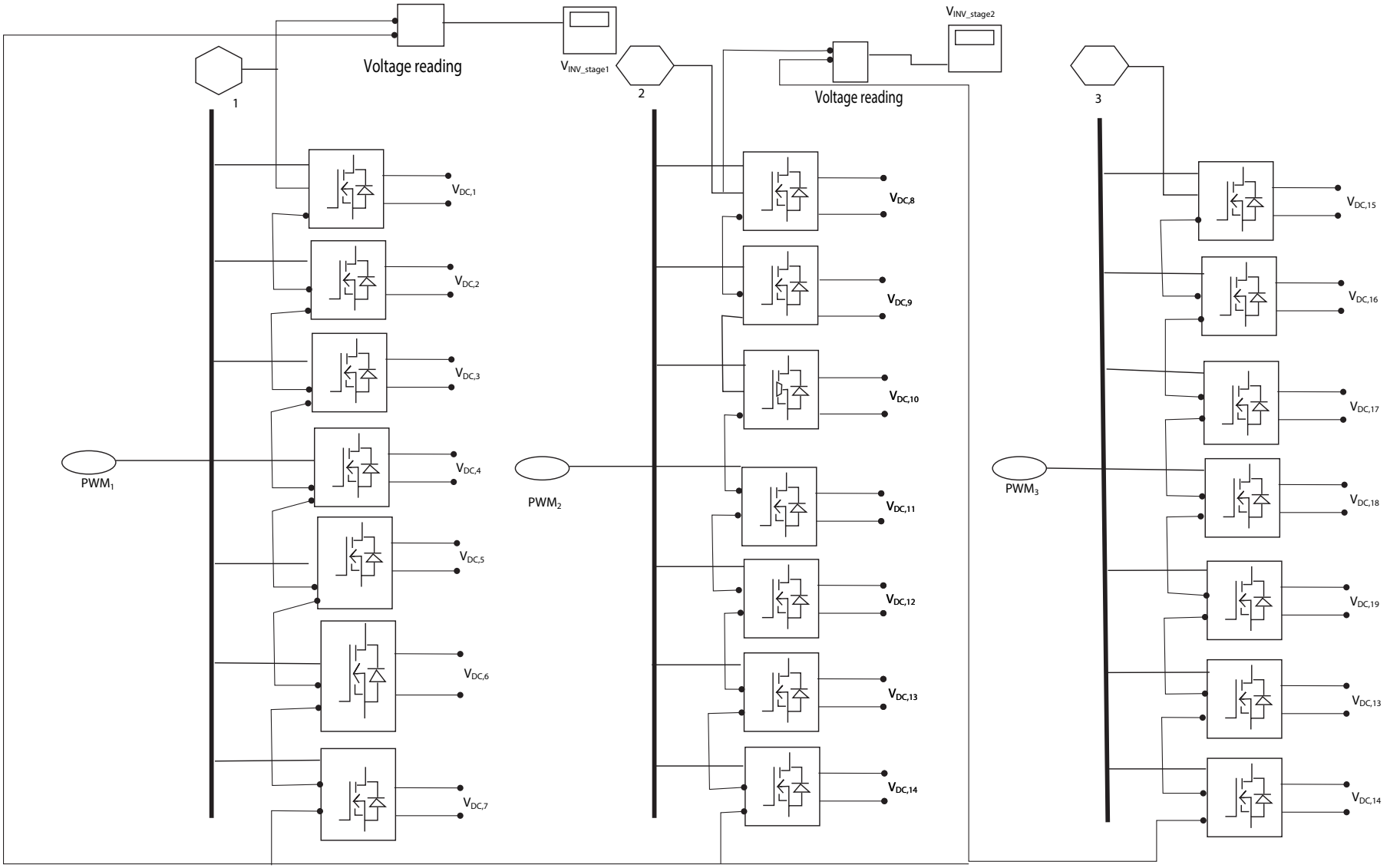


Figure 2. Simulation block of three-phase fifteen-level CHB MLI in Simulink.

15-Level CHB MLI Circuit (Phase A):
DC1 (48V) → [H1] → +v1−
↓
DC2 (48V) → [H2] → +v2− 7 H-bridges in series per phase
↓
⋮ Total: 21 H-bridges (3 phases)
↓
DC7 (48V) → [H7] → +vphase− (15 voltage levels)
[H] = H-bridge with 4 switches + PS-PWM gating signals S1–S28
Three phases (A, B, C) → LCL filter → Grid

Figure 3. 15-level CHB MLI topology: 7 series H-bridges per phase generate 15 discrete voltage levels ($2N + 1$, $N = 7$). Each H-bridge receives isolated 48 V DC. PS-PWM controls all 21 H-bridges (3 phases).

2.2. Modulation Block

The PS PWM scheme is implemented in the modulation block of the simulation, as shown in Figure 4.

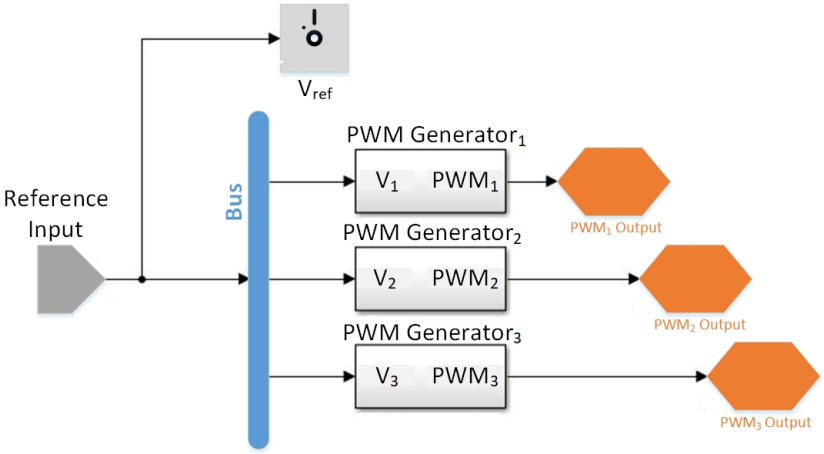


Figure 4. Modulation block of simulation in Simulink.

The modulation block consists of thee PWM generators for three phases. In this scheme, the numbers of carrier signals, having some shift on the horizontal axis, are used. For CHB MLI switches, PWM signals are created by comparing the carrier signals with the modulating signals. In this research, PS PWM topology for fifteen-level CHB MLI is implemented on MATLAB/SIMULINK. The carrier signals in the PS PWM technique are shifted by an angle of

$$\theta = \frac{2\pi}{(N-1)}, \tag{3}$$

where N represents the number of voltage levels in MLI, i.e., fifteen.

$$\theta = \frac{2\pi}{(15-1)} \approx 0.448 \text{ rad } (\text{or } 25.7^\circ),$$

This means the triangular carrier signals used for PWM in each submodule are phase-shifted by about 25.7° relative to each other to reduce harmonic distortion and improve output waveform quality

$$\theta_{\text{mutual}} = \frac{(1/\nu_s)}{2k}. \tag{4}$$

Here, θ_{mutual} represents the mutual phase shift of the carrier waves of submodules in seconds, k is the number of submodules which is seven in this simulation, and ν_s represents the switching frequency or carrier frequency. The internal model of the individual phase of the PWM generator implemented on MATLAB is shown in Figure 5.

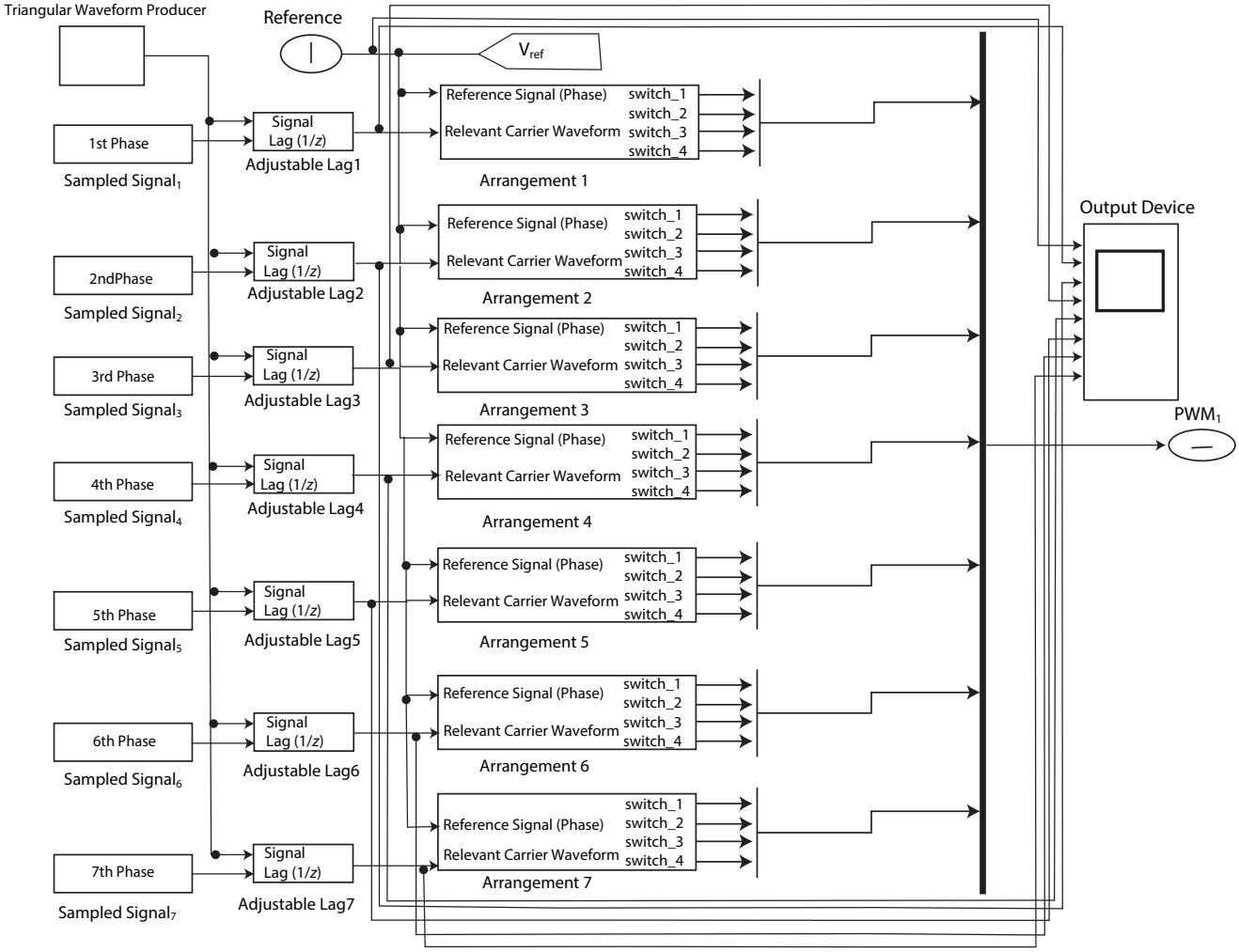


Figure 5. Internal model of the individual phase of the PWM generator.

2.3. Controller

This research employs a PI controller designed in the synchronous ($d-q$) frame to generate the voltage reference (V_{set}) for the Phase-Shifted Pulse Width Modulation (PS PWM) of a CHB MLI. The control strategy requires transforming the measured abc currents to the $d-q$ frame using a synchronization angle θ which is produced by the Phase-Locked Loop (PLL). In the $d-q$ frame, these measured currents are compared against reference currents (i_d, i_q) that dictate the desired active and reactive power (active power by d-current, reactive by q-current). The error signals are processed by two dedicated PI controllers (one for d, one for q) whose gains (k_p, k_i) are tuned for optimal performance. The outputs of the PI controllers (v_d, v_q) are then transformed/restored to the abc system to yield V_{set}. The design is complex due to the frame transformations and the use of two separate controllers. Figure 6 illustrates the control strategy, and V_{set} is used for the PS PWM implementation in MATLAB.

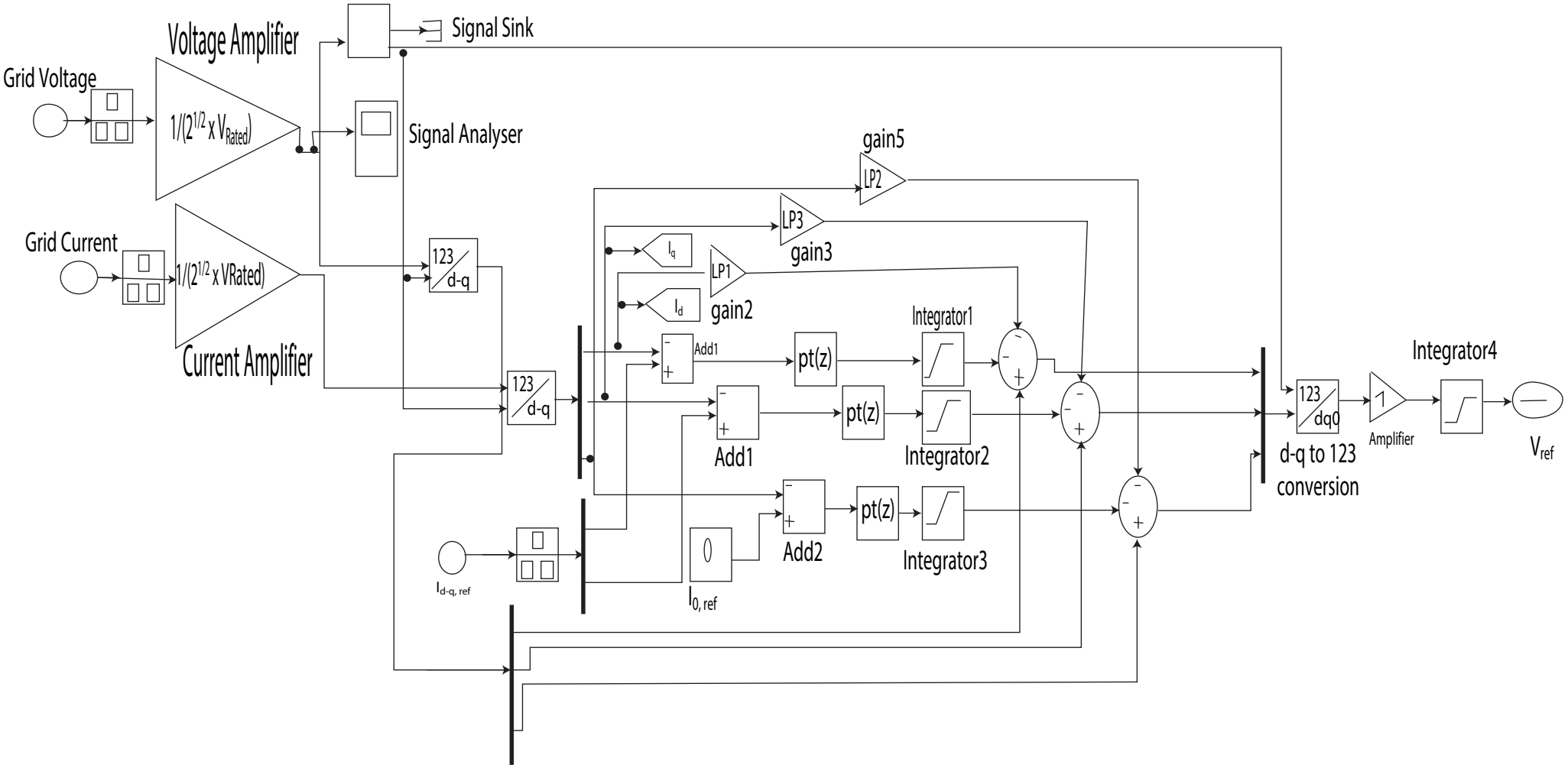


Figure 6. Block diagram of PI controller used in grid-connected MLI.

To mathematically describe the transformation of the measured three-phase currents (i_a, i_b, i_c) into the synchronous dq frame, the Park transformation is applied using the synchronization angle θ obtained from the PLL:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{5}$$

This transformation converts the three-phase currents into two orthogonal components:

1. i_d, which controls the active power component, and
2. i_q, which controls the reactive power component.

The error signals between the reference and measured currents in the dq frame are then processed by the PI controllers, for example, in the d-axis:

$$v_d(t) = k_p e_d(t) + k_i \int e_d(t)\, dt, \tag{6}$$

where

$$e_d(t) = i_{d,ref}(t) - i_d(t), \tag{7}$$

is the error signal, and k_p and k_i are the proportional and integral gains, respectively.

The outputs v_d and v_q are transformed back into the abc frame to generate the voltage reference V_{ref} used in the PS PWM scheme. The controlled inverter output now requires an LCL filter for grid interfacing.

2.4. PI Controller Parameter Selection

The PI controller operates in the synchronous dq-frame for independent active (i_d) and reactive (i_q) current regulation. Identical gains were selected for both axes based on standard tuning practices for grid-connected inverters.

These conservative values shown in Table 1 ensure:

- Stability: Phase margin $> 45^\circ$, gain margin > 6 dB (Bode analysis);
- Performance: Settling time < 20 ms, overshoot $< 10\%$;
- Robustness: Effective across $\pm 20\%$ grid impedance variation.

Table 1. PI controller gains and performance metrics.

Axis	K_p	K_i
d-axis (active power)	0.5	50
q-axis (reactive power)	0.5	50

The gains follow established guidelines for LCL-filtered systems [10]: $K_p \approx 0.5 L_{eq} f_{sw}/10$, $K_i \approx 10\omega_g$, where $L_{eq} = L_a + L_b = 1.3$ mH. Simulation verification confirmed perfect grid synchronization (zero steady-state error) and no impact on achieved THD levels (0.53% current, 0.69% voltage).

2.5. Proposed Three-Phase LCL Filter Design Procedure

In order to suppress voltage and current harmonics at the point of common coupling (PCC) linking the three-phase CHB MLI to the grid, an output filter is required. This study proposes and implements a wye topology LCL filter. LCL filters are generally favored over simple L or RL filters due to their ability to provide higher harmonic attenuation and smoother inverter output voltages and currents. Advantages of the LCL filter topology also include reduced weight, cost, and component size [24]. Notably, they can achieve better

performance with smaller inductor and capacitor values at power levels up to hundreds of kilowatts [25]. This paper employs the wye LCL filter alongside the PS PWM technique. This combination is designed to minimize voltage and current distortion injected into the utility grid. The structure of the proposed wye-connected LCL filter, as simulated in MATLAB, is shown in Figure 7, with L1 and L2 linked with the grid and inductor.

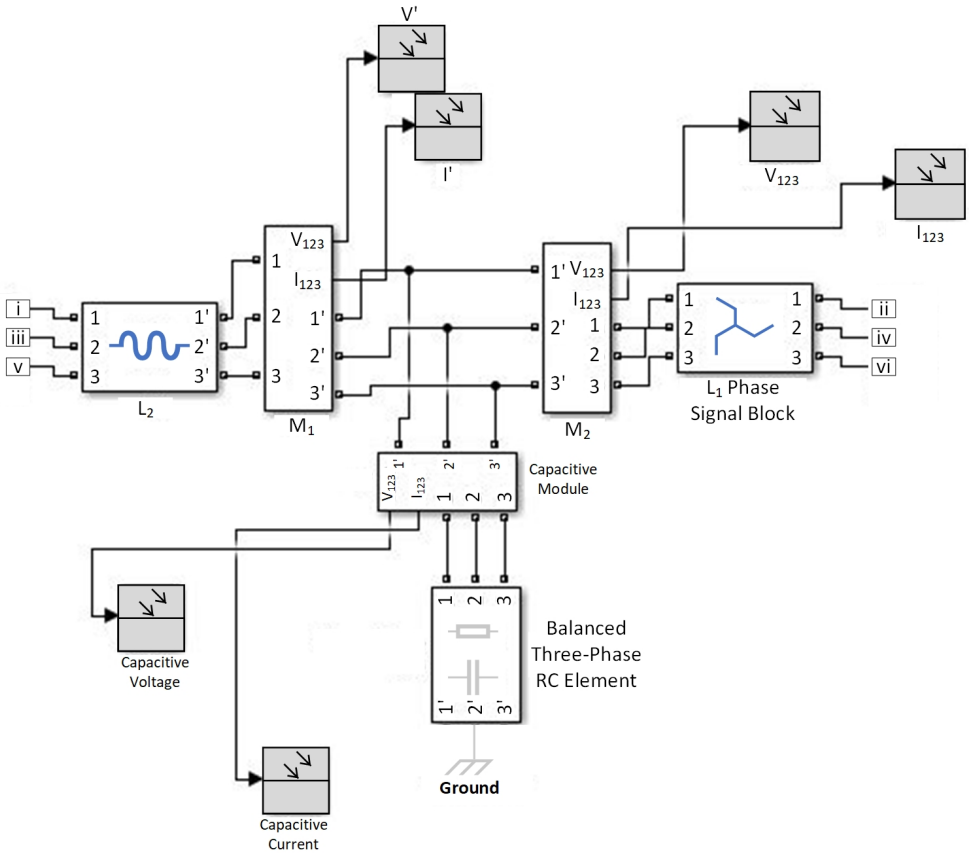


Figure 7. Simulation block of three-phase LCL filter.

To effectively suppress voltage and current harmonics at PCC, the design and implementation of a suitable LCL filter are essential. Next, we present the mathematical modeling of the proposed LCL filter topology, which lays the foundation for its systematic design.

Mathematical Modeling of the LCL Filter

The mathematical relationship describing the single-phase LCL filter and a wye-connected capacitor is depicted in Figure 8 [26,28], using standard parameters L_a, L_b, and C_f.

$$i_a(s) = v_i(s) - \frac{v_c(s)}{sL_a} \tag{8}$$

where

$i_a(s)$: Laplace transform of the converter-side inductor current,
$v_i(s)$: Laplace transform of the input voltage,
$v_c(s)$: Laplace transform of the capacitor voltage,
L_a: converter-side inductance.

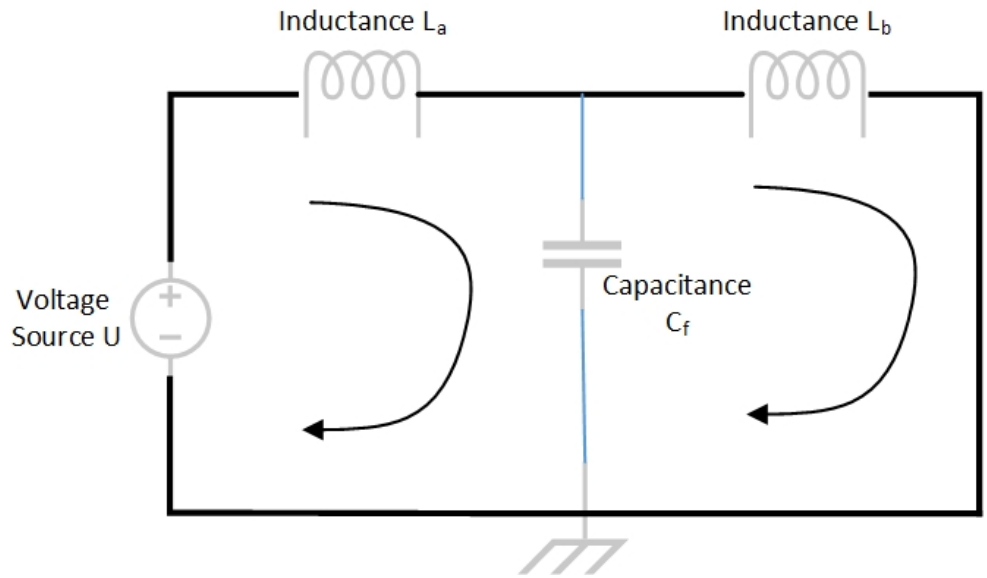


Figure 8. Single-Phase model representation for LCL filter design.

$$i_2(s) = v_c(s) - \frac{v_g(s)}{sL_b} \tag{9}$$

where

$i_2(s)$: Laplace transform of the grid-side inductor current (output current);
$v_g(s)$: Laplace transform of the grid voltage;
L_b: grid-side inductance.

$$v_c(s) = \left(R_f + \frac{1}{sC_f}\right) i_c(s) \tag{10}$$

where

$v_c(s)$: Laplace transform of the capacitor voltage;
R_f: damping resistance;
C_f: filter capacitance;
$i_c(s)$: Laplace transform of the capacitor current.

The LCL filter transfer function $\frac{i_2(s)}{v_i(s)}$ is derived via the superposition principle as

$$\frac{i_2(s)}{v_i(s)} = \frac{1}{L_a L_b C_f s^3 + (L_a + L_b)s} \tag{11}$$

where L_a, L_b, C_f, and s (Laplace variable) retain their prior definitions.

The flow chart given in Figure 9 describes the structured process for developing the LCL filter used in this paper [29,30].

2.6. LCL Filter Design Algorithm and Pseudocode

The following presents the elaborated LCL filter design algorithm (Algorithm 1) followed by a Python (3.12)-style pseudocode implementation. This provides a clear and detailed methodology for designing LCL filter specifications within the three-phase grid-tied H-bridge inverter system.

A detailed Python-style implementation outline of the design algorithm is provided as Supplementary Material.

Algorithm 1 Elaborated LCL filter design towards three-phase grid-tied H-bridge inverter system

Require: Grid frequency f_g, switching frequency f_{sw}, base impedance Z_b, base capacitance C_b, maximum allowable current ripple ΔI_{max}, rated current I_{rated}, DC link voltage U, required attenuation factor K_a

Ensure: Filter parameters: capacitance C_f, inductance interfacing the inverter L_a, inductance interfacing the grid L_b, damping resistor R_f

Initialize base parameters and system specifications:
Input f_g, f_{sw}, Z_b, C_b, ΔI_{max}, I_{rated}, U, K_a
Calculate filter capacitor size:

$$C_f \leftarrow 0.05 \times C_b$$

Calculate inverter-side inductor L_a to limit current ripple:

$$L_a \leftarrow \frac{U}{4 f_{sw} \Delta I_{max} I_{rated}}$$

Initialize grid-side inductor L_b with an initial guess
function CALCULATERESONANCEFREQUENCY(L_a, L_b, C_f)
    return $\frac{1}{2\pi}\sqrt{\frac{L_a + L_b}{L_a L_b C_f}}$
end function
repeat
    $f_{res} \leftarrow$ CALCULATERESONANCEFREQUENCY(L_a, L_b, C_f)
    if $f_{res} \leq 10 f_g$ **or** $f_{res} \geq 0.5 f_{sw}$ **then**
        Adjust L_b (increment or decrement by a small step)
    end if
until $10 f_g < f_{res} < 0.5 f_{sw}$
Calculate damping resistor R_f to suppress resonance:

$$\omega_{res} \leftarrow 2\pi f_{res}$$

$$R_f \leftarrow \frac{1}{3\omega_{res} C_f}$$

Simulate system with designed filter parameters in MATLAB/Simulink using 15-level CHB MLI and PS PWM
Perform FFT analysis on output voltage and current at PCC to evaluate THD
if THD $< 5\%$ **then**
    Accept design and finalize filter parameters
else
    Adjust filter parameters (e.g., L_a, L_b, C_f, R_f) and repeat design process
end if
Document all design parameters and simulation results for reproducibility and future hardware implementation

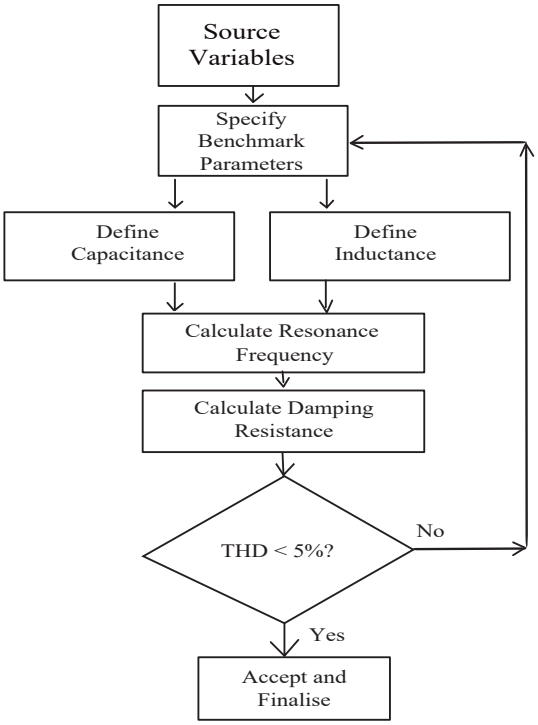


Figure 9. LCL filter design flow chart. Step 1 (Parameters): $f_g = 50$ Hz, $f_{sw} = 5$ kHz, $S = 17.6$ kVA, $V_{L-L} = 400$ V. Step 2 (Capacitor): $C_f = 0.05C_b$ (5% base capacitance, power factor variation limit). Step 3 (Inverter Inductor): $L_a = \frac{V_{dc}}{4f_{sw}\Delta I_{max} I_{rated}}$ (10% ripple limit). Step 4 (Resonance): $f_{res} = \frac{1}{2\pi\sqrt{\frac{L_a L_b}{L_a+L_b}C_f}}$ where $10f_g < f_{res} < 0.5f_{sw}$ (achieved 2.3 kHz). Step 5 (Damping): $R_f = \frac{1}{3\omega_{res}C_f}$ ($\omega_{res} = 2\pi f_{res}$). Step 6 (Verification): MATLAB/Simulink FFT confirms THD < 5% (0.53% current, 0.69% voltage).

3. Proposed LCL Filter Design Procedure

Parameters required for the LCL filter design include rated power (S), RMS line-to-line voltage (V_{LL}) at inverter output, switching frequency (f_{sw}), DC-link voltage (V_{dc}), phase voltage (V_{ph}), and grid frequency (f_g).

The base impedance is defined as

$$Z_b = \frac{V_{ph}^2}{S} \tag{12}$$

The base capacitance is

$$C_b = \frac{S}{V_{ph}^2 \cdot (2\pi f_g)} \tag{13}$$

Filter components are expressed as percentages of these base values.

The filter capacitance is selected to limit reactive power to 5% of rated power:

$$C_f = 0.05 \times C_b \tag{14}$$

Maximum current ripple is limited to 10% of rated current. Rated RMS current is

$$I_{rated} = \frac{S}{\sqrt{3}V_{LL}} \tag{15}$$

Maximum ripple current for SPWM inverter ($m = 0.5$) is

$$\Delta I_{L,max} = \frac{V_{dc}}{8 f_{sw} L_a} = 0.1 I_{rated} \tag{16}$$

Thus, converter-side inductance becomes

$$L_a = \frac{V_{dc}}{8 f_{sw} \cdot 0.1 I_{rated}} \tag{17}$$

To attenuate switching harmonics while maintaining stability, the grid-side inductor satisfies

$$\frac{i_2}{i_a} = \frac{1}{1 + L_b C_f (2\pi f_{sw})^2} = 0.1 \tag{18}$$

Solving for grid-side inductance

$$L_b = \frac{1.1}{C_f (2\pi f_{sw})^2} \tag{19}$$

Typically, $L_a = 4 - 6L_b$ ensures proper harmonic attenuation.
A series damping resistor R_f prevents resonance. Resonant frequency is

$$f_{res} = \frac{1}{2\pi} \sqrt{\frac{L_a + L_b}{L_a L_b C_f}} \tag{20}$$

Design constraint: $10 f_g < f_{res} < 0.5 f_{sw}$. Damping resistor is

$$R_f = \frac{1}{3} \sqrt{\frac{L_a + L_b}{L_a L_b C_f}} \tag{21}$$

This systematic procedure yields an LCL filter with <1% THD at rated conditions while satisfying IEEE 519-2022 limits [38].

4. Designed System Parameter and Results

All simulations were conducted in MATLAB/Simulink R2025a using a fixed-step continuous solver (ode23tb) with a maximum time step of 1×10^{-6} s to accurately capture high-frequency PWM switching in the three-phase fifteen-level CHB MLI with PS-PWM, PI control ($K_p = 0.5$, $K_i = 50$, tuned via Ziegler–Nichols for zero steady-state error in the dq-frame), and the proposed LCL filter. The model employs ideal switches without discretization under balanced conditions (400 V L-L, 50 Hz grid). Tables 2 and 3 show design parameters and LCL filter values obtained via the methodology in Section 2, with resonance frequency $f_{res} = 2.3$ kHz.

Table 2. Design parameters of the system.

No	System Parameter	Value
1	VL-L	400 V (rms)
2	S	17.6 kVA
3	fsw	5 kHz
4	Vdc	48 V (to each bridge)
5	fg	50 Hz

Table 3. LCL filter parameters of the system.

No	System Parameter	Value
1	Cf	17.6 µF
2	L1	1 mH
3	L2	0.3 mH
4	Rf	3 Ω

The fifteen-level output from the CHB MLI and output of one of the phases of the modulation block implemented on MATLAB are shown in Figures 10 and 11, respectively. Output waveform of the current and voltage obtained by using the proposed LCL filter is shown in Figures 12 and 13, respectively.

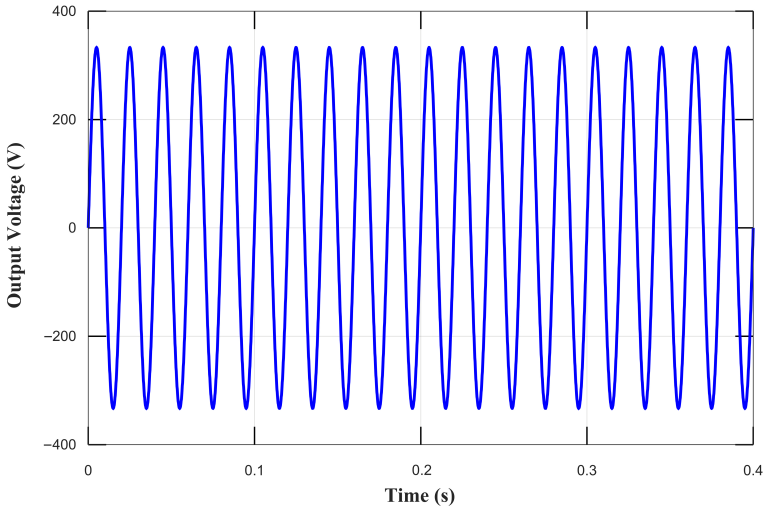


Figure 10. Output voltage waveform of fifteen-level CHB MLI.

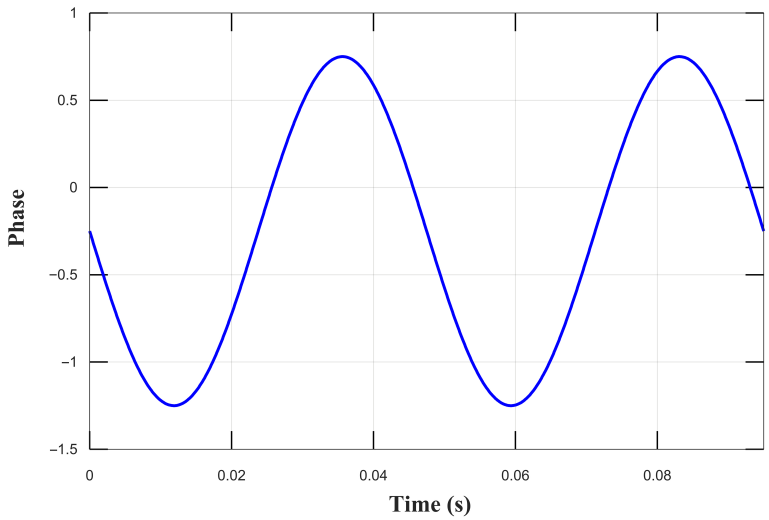


Figure 11. Output waveform of one phase of the modulation generator.

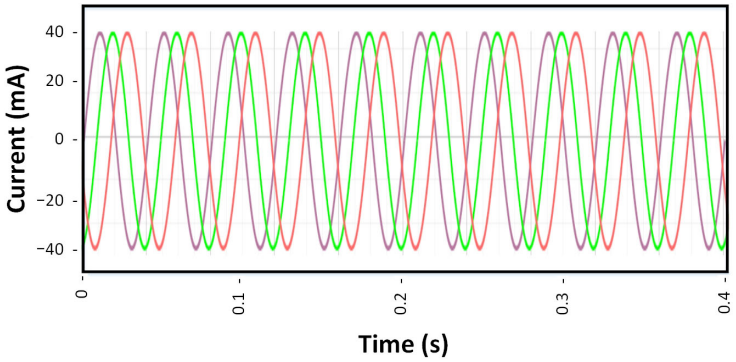


Figure 12. Output current waveform using filter, i.e., If2 (L-L).

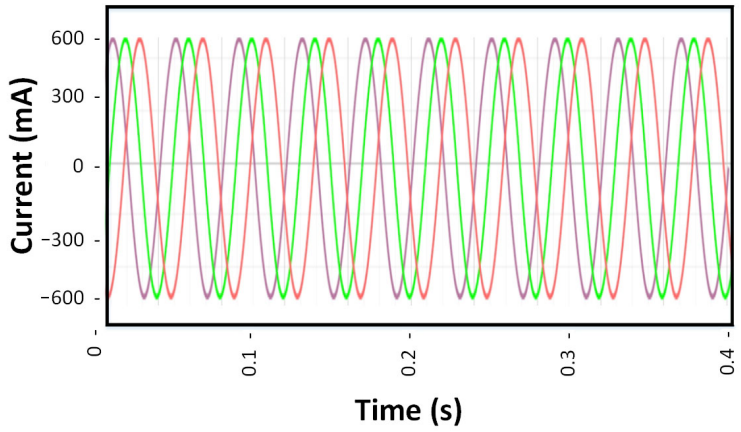


Figure 13. Output voltage waveform using filter, i.e., Vf2 (L-L).

First of all, voltage and current THDs at PCC are observed without using a filter, i.e., V2 (L-L) and I2 (L-L), as shown in Figures 14 and 15, respectively. Similarly, the FFT analysis of voltage and current THDs at PCC are observed by using the proposed LCL filter, i.e., Vf2 (L-L) and If2 (L-L), as shown in Figures 16 and 17, respectively.

Firstly, significant harmonic content is found in both Figures 14 and 15. Figure 14 shows about 16.92% of THD, which occurs primarily due to switching in the fifteen-level inverter. In contrast, the current waveform has a lower THD of 3.03% (Figure 15), benefiting from the natural filtering effect of the load and grid impedance.

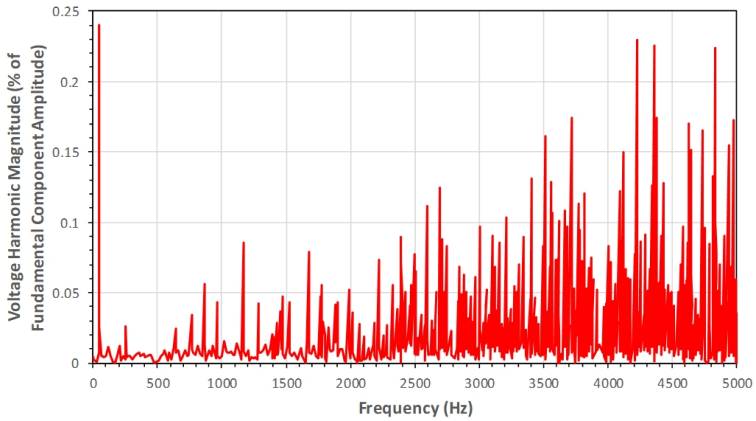


Figure 14. Total harmonic distortion spectrum of unfiltered inverter output voltage at PCC.

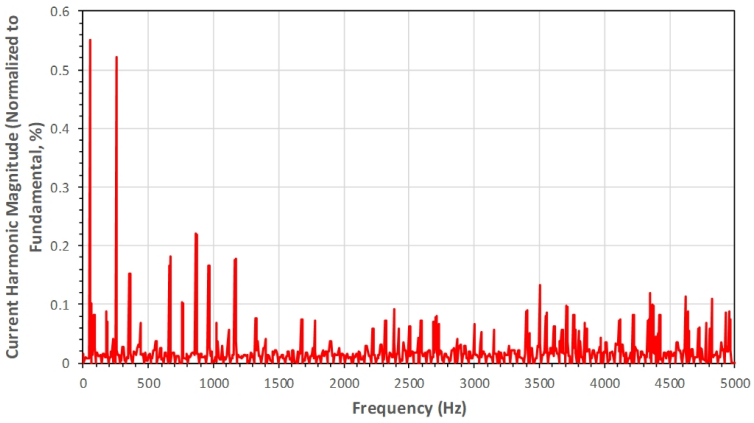


Figure 15. Total harmonic distortion spectrum of unfiltered inverter output current at PCC.

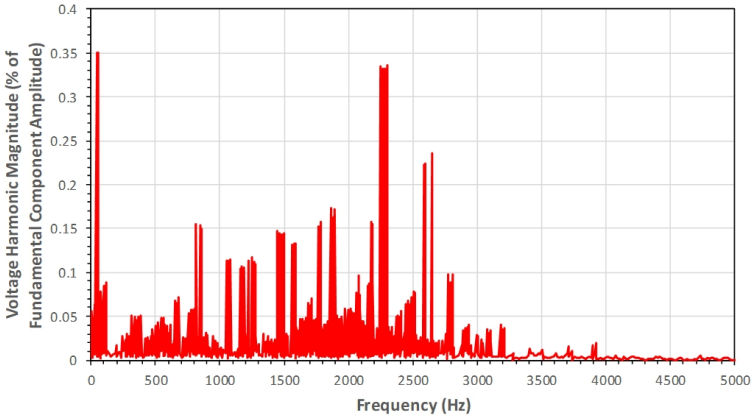


Figure 16. Total harmonic distortion spectrum of filtered inverter output voltage at PCC.

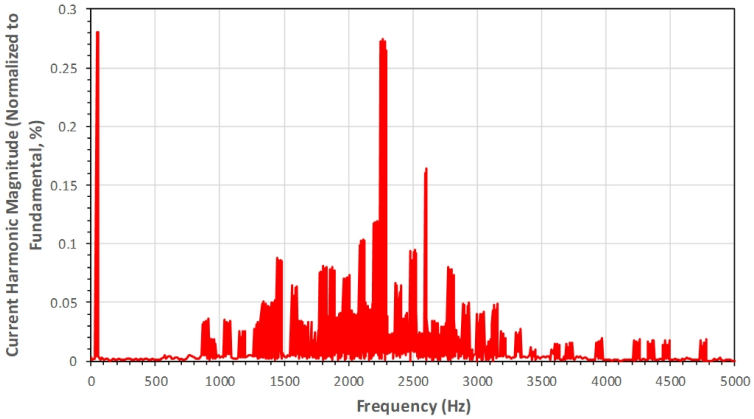


Figure 17. Total harmonic distortion spectrum of filtered inverter output current at PCC.

The harmonic spectra for both are dominated by components near the switching frequency and its multiples up to 5 kHz, characteristic of the Sinusoidal Pulse Width Modulation strategy used. Though the magnitude of current distortion stays low, these harmonic levels intensify in lowering the quality of output power, with more loss, resulting in the risk of damage to the equipment being used. Our results therefore highlight the requirement of a relevant harmonic filter that would enable the operation of the system that meets satisfactory quality of power output and functioning.

4.1. Harmonic Spectrum with the Proposed LCL Filter Applied

The presented figure consists of Figures 16 and 17 showing the frequency domain representations of the inverter output voltage and current at the point of common coupling (PCC) after applying the proposed LCL filter.

In Figure 16 (filtered output voltage harmonics), the dominant fundamental harmonic at 50 Hz exhibits a normalized magnitude of 36 (units relative to fundamental scale).

THD significantly decreases up to 0.69%, which is significantly below the typical industry standard of 5% for grid-connected systems (such as IEEE 519).

Higher-order harmonic components, primarily related to the switching frequency and its multiples (around 2 kHz to 2.5 kHz), are subdued to very low magnitudes, indicating effective attenuation by the LCL filter.

The spectral roll-off beyond 3 kHz confirms the filter's capability to effectively minimize switching frequency harmonics without introducing resonance peaks in the frequency range of interest.

In Figure 17 (filtered output current harmonics), the fundamental harmonic magnitude is recorded at 562.2 (units relative to fundamental scale), consistent with system current magnitudes.

The current THD is reduced to 0.53%, demonstrating outstanding filtering performance.

Similar to the case of voltage, the current harmonic components beyond the fundamentals are substantially diminished.

Suppression of harmonic current components minimizes thermal and electromagnetic stress on downstream equipment and assists in fulfilling stringent power quality requirements.

4.2. Comparative Analysis of Harmonic Spectra Before and After Filtering

Tables 4 and 5 summarize the key differences between the unfiltered spectra shown in Figures 14 and 15, and the filtered results from the LCL filter represented in Figures 16 and 17.

Technical Observations

- Although differences in measurement normalization cause the fundamental amplitude scales to invert between the voltage and current spectra, the trend of harmonic attenuation remains clear and consistent.
- The value of voltage THD before the process of filtering is considerably higher than that for current THD. This happens because of the inverter switching on the output voltage signal, in addition to the current harmonics being relegated by the system's impedance.
- The values of voltage as well as current THD after the filtering process stay lower that 1%. This reinstates the impact of our LCL filtering scheme that is being used to dominate harmonic components.
- Furthermore, at a switching frequency of 5 kHz, numerous peaks were found earlier. It is seen that the filtering mechanism not only controls these high values but also subjugates the relevant sidebands. This is an important outcome, as these sidebands could otherwise amplify and seriously interfere with the desired outcomes in any installed system.
- In this way, these results validate the proposed LCL filter design methodology and confirm its suitability for practical grid-tied cascaded H-bridge inverter applications requiring compliance with international power quality standards.

Table 4. Comparison of line-to-line inverter output voltage harmonic characteristics before and after LCL filtering.

S.No	Parameter	Unfiltered Voltage (Figure 14)	Filtered Voltage (Figure 16)
1	Signal Type	Line-to-line inverter output voltage	Line-to-line voltage after LCL filtering
2	Total Harmonic Distortion (THD)	16.92%	0.69%
3	Fundamental Peak Magnitude	∼562 (normalized units)	∼36 (normalized units)
4	Switching Frequency Harmonics	Prominent peaks at 2–5 kHz with high magnitude	Significantly attenuated; minor residual peaks
5	Harmonic Content Range	Harmonics present up to 5 kHz, substantial magnitude	Harmonics nearly vanish beyond 1.5 kHz
6	Noise Floor	Signal well above noise floor with clear harmonic peaks	Harmonics approach or drop below noise floor
7	Resonance Effects	No resonance suppression as no filter applied	No resonance peaks; effective damping by resistor
8	Measurement Scaling	Higher amplitude scale typical for voltage signals	Reduced amplitude scale post-filtering (normalized)
9	Dominant Harmonics	Large non-fundamental peaks at multiples of 50 Hz (near 2.5 kHz)	Dominant fundamental 50 Hz harmonic; higher harmonics nearly absent
10	Waveform Purity	Significant waveform distortion due to switching harmonics	Nearly sinusoidal; filter yields high waveform purity
11	Impact on Power Quality	Severe distortion impacting grid power quality; possible non-compliance	THD well under 5%; compliant with IEEE 519 and maintaining power quality
12	Equipment/Grid Implications	High risk of overheating, component aging, and interference	Minimizes equipment stress; supports grid stability and component lifespan

Table 5. Comparison of line-to-line inverter output **current** harmonic characteristics before and after LCL filtering.

S.No	Parameter	Unfiltered Current (Figure 15)	Filtered Current (Figure 17)
1	Signal Type	Line-to-line inverter output current	Line-to-line current after LCL filtering
2	Total Harmonic Distortion (THD)	3.03%	0.53%
3	Fundamental Peak Magnitude	∼36 (normalized units)	∼562 (normalized units)
4	Switching Frequency Harmonics	Peaks near switching frequency but lower magnitude	Significantly attenuated; minor residual harmonics
5	Harmonic Content Range	Harmonics up to 5 kHz; smoother spectrum than voltage	Harmonics nearly vanish beyond 1 kHz
6	Noise Floor	Closer to noise floor; harmonic peaks discernible	Harmonics at or below noise floor, hard to observe
7	Resonance Effects	No resonance damping present	No resonance peaks; effective resonance damping observed
8	Measurement Scaling	Lower amplitude scale typical for current signals	Amplitude scale increased post-filtering (normalized)
9	Dominant Harmonics	Lower magnitude non-fundamental peaks	Dominant 50 Hz fundamental harmonic; higher harmonics suppressed
10	Waveform Purity	Moderate waveform distortion	Nearly sinusoidal waveforms
11	Impact on Power Quality	Moderate risk of grid disturbance and measurement errors	THD well below IEEE 519 limits; high power quality
12	Equipment/Grid Implications	Moderate risk of thermal and electromagnetic stress	Minimal risk; improved reliability and grid compatibility

4.3. Parametric Evaluation of LCL Filter Harmonic Performance

To thoroughly evaluate the robustness and effectiveness of the designed LCL filter, the grid-connected inverter system is systematically tested across a wide range of switching frequencies (from 1 to 5 kHz) and grid impedance ratios X/R (from 2 to 9). These parameters are varied to reflect realistic operating conditions, where the switching frequency directly influences the harmonic spectrum at the inverter output, and the X/R ratio represents the inductive versus resistive character of the grid at the point of common coupling.

The harmonic performance is quantified by measuring the total harmonic distortion (THD) of both voltage and current waveforms, both before and after the LCL filter, as detailed in the comprehensive parametric study presented in Tables 4 and 5. These tables not only document the raw experimental results but also facilitate direct comparison with grid standards such as IEEE 519, underscoring the practical relevance of the findings.

By analyzing these results, the following section draws actionable achievements about the filter's effectiveness, optimal operating points, and sensitivity to grid and inverter parameters—insights critical for both academic research and field deployment.

4.4. Particulars of LCL Filter Performance

- The LCL filter delivers consistently low THD for both the voltage and current at the inverter output across all tested switching frequencies (1–5 kHz) and grid impedance ratios (X/R = 2–9). In all cases, post-filter THD remains well below the 5% threshold specified by IEEE 519-2022 for grid-connected inverters.
- For example, at 1 kHz (Table 3), voltage THD is reduced from over 14% (unfiltered) to below 1.2% (filtered), while current THD remains under 2%.
- The filter's performance demonstrates low sensitivity to grid impedance variation, proving robust even as the grid becomes more inductive (higher X/R). This adaptability is crucial for reliable operation in real-world installations, where grid conditions may fluctuate.
- Standards compliance and optimal performance are both clearly demonstrated: the most favorable results are achieved at 3 kHz and X/R $\approx$ 5.6, where both voltage and current THD reach their minima (0.53% and 0.69%, respectively). This combination suggests that the filter's resonance frequency and damping are particularly well tuned for these parameters, yielding the highest power quality within the tested range.
- Even as switching frequency increases beyond this optimal point—resulting in higher unfiltered ripple (Tables 6 and 7)—the LCL filter maintains output distortion within acceptable limits, confirming reliable harmonic attenuation across the full operational range.
- Notably, there is no evidence of resonance-related distortion in the filtered spectra, indicating that the filter's passive damping strategy effectively suppresses instabilities.
- It should be noted that these results are obtained under balanced, steady-state, and linear load conditions. Future work should assess performance during grid transients, unbalanced operation, and with nonlinear loads to further validate field readiness.
- In summary, the systematic parametric evaluation in Tables 6–11 confirms that the proposed LCL filter is both effective and robust, offering low harmonic distortion, insensitivity to grid impedance, and compliance with international standards. The optimal operating point identified here provides a practical reference for system design, while the overall performance data establish a strong foundation for both academic research and industrial deployment.

THD variations arise from switching frequency f_{sw} and the grid X/R ratio: higher f_{sw} (e.g., 5 kHz) reduces voltage THD via finer PWM resolution, shifting harmonics beyond filter cutoff. Current THD increases slightly at high X/R (>7) due to resonance proximity ($f_{res} \approx 2.3$ kHz) but remains <1% across XR = 2–9, demonstrating robustness.

THD calculations employed MATLAB/Simulink's built-in FFT analyzer with a default 50th harmonic limit and 3 s window, consistent with IEEE 519-2022 §5.2 recommendations for grid-connected inverters. Individual harmonic limits complied with Table 2 of the standard.

Table 6. THD variation in inverter parameters at the PCC with designed LCL filter applied. Results for different grid X/R ratios at switching frequency $f_{sw} = 1$ kHz.

No.	X/R Ratio	$V_{unfiltered}$ (THD %)	$V_{filtered}$ (THD %)	$I_{unfiltered}$ (THD %)	$I_{filtered}$ (THD %)
1	2	14.96	1.05	3.20	1.47
2	4	14.80	1.09	3.31	1.51
3	5.6	15.34	1.05	3.34	1.47
4	7	14.75	1.11	3.29	1.52
5	9	15.00	1.07	3.25	1.51

Notes: $V_{unfiltered}$ and $I_{unfiltered}$ denote values before filtering; $V_{filtered}$ and $I_{filtered}$ after LCL filtering. X/R is the grid impedance ratio. THD values are percentages.

Table 7. THD variation in inverter parameters at the PCC with designed LCL filter applied. Results for different grid X/R ratios at switching frequency $f_{sw} = 2$ kHz.

No.	X/R Ratio	$V_{unfiltered}$ (THD %)	$V_{filtered}$ (THD %)	$I_{unfiltered}$ (THD %)	$I_{filtered}$ (THD %)
1	2	15.16	0.44	2.60	0.61
2	4	15.69	0.49	2.58	0.70
3	5.6	15.68	0.54	2.64	0.73
4	7	15.39	0.49	2.60	0.69
5	9	15.58	0.53	2.63	0.72

Notes: Same as Table 6.

Table 8. THD variation in inverter parameters at the PCC with designed LCL filter applied. Results for different grid X/R ratios at switching frequency $f_{sw} = 3$ kHz.

No.	X/R Ratio	$V_{unfiltered}$ (THD %)	$V_{filtered}$ (THD %)	$I_{unfiltered}$ (THD %)	$I_{filtered}$ (THD %)
1	2	16.81	0.54	2.97	0.80
2	4	17.02	0.56	3.02	0.77
3	5.6	16.92	0.53	3.03	0.69
4	7	16.93	0.72	2.94	1.04
5	9	17.09	0.70	3.00	1.00

Notes: Same as Table 6.

Table 9. THD variation in inverter parameters at the PCC with designed LCL filter applied. Results for different grid X/R ratios at switching frequency $f_{sw} = 4$ kHz.

No.	X/R Ratio	$V_{unfiltered}$ (THD %)	$V_{filtered}$ (THD %)	$I_{unfiltered}$ (THD %)	$I_{filtered}$ (THD %)
1	2	22.59	1.31	4.55	1.82
2	4	23.40	1.25	4.60	1.76
3	5.6	23.00	1.23	4.63	1.83
4	7	23.17	1.22	4.60	1.74
5	9	23.46	1.28	4.70	1.81

Notes: Same as Table 6.

Table 10. THD variation in inverter parameters at the PCC with designed LCL filter applied. Results for different grid X/R ratios at switching frequency $f_{sw} = 5$ kHz.

No.	X/R Ratio	$V_{unfiltered}$ (THD %)	$V_{filtered}$ (THD %)	$I_{unfiltered}$ (THD %)	$I_{filtered}$ (THD %)
1	2	15.91	1.39	2.34	2.02
2	4	16.10	1.31	2.36	1.89
3	5.6	16.29	1.30	2.30	1.80
4	7	16.33	1.38	2.34	1.96
5	9	16.35	1.39	2.35	1.94

Notes: Same as Table 6.

Table 11. Summary of THD variation in inverter parameters at the PCC with designed LCL filter applied. Results for different switching frequencies f_{sw} at grid X/R ratio around 5.6.

No.	Switching Frequency f_{sw} (kHz)	X/R Ratio	$V_{unfiltered}$ (THD %)	$V_{filtered}$ (THD %)	$I_{unfiltered}$ (THD %)	$I_{filtered}$ (THD %)
1	1	15.34	1.05	3.34	1.47	2.02
2	2	15.69	0.54	2.64	0.73	1.89
3	3	16.92	0.53	3.03	0.69	1.80
4	4	22.48	1.23	3.13	1.30	1.96
5	5	16.29	1.31	2.35	1.93	1.94

Notes: This table summarizes THD values for different switching frequencies at approximately fixed X/R ratio of 5.6. Columns: X/R = grid impedance ratio, THD values in percent before and after LCL filtering.

4.5. Comparative Performance Analysis

Table 12 compares the proposed LCL filter against recent studies [39–41], demonstrating superior harmonic performance (0.53% I-THD, 0.69% V-THD at 5 kHz). While referenced works employ single-phase PV microinverters and simpler topologies, the fifteen-level three-phase CHB MLI configuration with a systematic wye LCL design achieves significantly lower distortion across diverse operating conditions.

Table 12. LCL filter performance comparison.

Study	f_{sw} (kHz)	I-THD (%)	V-THD (%)	Topology/Application
This work	5	0.53	0.69	15-level three-phase CHB
[39]	4	1.1	1.6	Single-phase PV microinverter
[40]	3.2	1.4	2.0	PV inverter, passive damping
[41]	3.5	1.3	1.8	Single-phase PV

4.6. Limitations and Future Work

The simulations assume balanced steady-state conditions with ideal switches and linear grid impedance. While demonstrating excellent harmonic performance, these conditions exclude nonlinear loads, grid faults, and transient events that may affect real-world deployment. Future work will incorporate unbalanced conditions, nonlinear loads (e.g., rectifiers), and dynamic grid events using real-time digital simulators.

5. Conclusions

This work explores the design and evaluation of a three-phase, fifteen-level cascaded H-bridge (CHB) multilevel inverter (MLI), integrated with an optimally designed LCL filter, for use in renewable power systems connected to the electrical grid. The CHB MLI, selected for its ability to generate smooth output waveforms with inherently low harmonic content, is controlled using a Phase-Shifted PWM (PS PWM) technique that ensures even power distribution and minimizes output distortion. Notably, this work contributes a rigorous, reproducible design methodology for the LCL filter, demonstrating that even in challenging grid environments—with variable switching frequencies and a wide range of grid impedance ratios—the system achieves total harmonic distortion (THD) levels well below the 5% threshold specified in international standards such as IEEE 519. This robust performance is validated through comprehensive parametric simulations, with optimal results (THD of 0.53% for current and 0.69% for voltage) achieved at a switching frequency of 3 kHz and $X/R \approx 5.6$. The proposed LCL filter outperforms reported benchmarks (Table 12) while maintaining reproducibility through the detailed design algorithm.

The practical implications of these findings are significant: the proposed system offers a reliable, scalable solution for integrating distributed renewable energy sources into power grids with diverse impedance profiles, directly addressing a key challenge in the global transition to sustainable energy. To the authors' knowledge, this represents one of the most thorough parametric validations of its kind for high-level CHB MLI systems using passive LCL filters. While these results, obtained under balanced, steady-state conditions, provide a strong foundation for academic research and industrial application, future work should include hardware validation, investigation of unbalanced and non-linear operating conditions, and exploration of higher-level MLI configurations for further reduction in THD and filter size. These steps will help bridge the gap between simulation-based design and real-world deployment in next-generation smart grids.

Supplementary Materials: The following supporting information can be downloaded at: https://www.mdpi.com/article/10.3390/designs10010006/s1.

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Abbreviations

Acronym	Full Form
CHB	Cascaded H-Bridge
MLI	Multilevel Inverter
LCL	Inductor-Capacitor-Inductor
PS-PWM	Phase-Shifted Pulse Width Modulation
PCC	Point of Common Coupling
THD	Total Harmonic Distortion
RES	Renewable Energy Source
SES	Sustainable Energy Sources
PWM	Pulse Width Modulation
LS-PWM	Level-Shifted Pulse Width Modulation
PI	Proportional-Integral
PLL	Phase Locked Loop
SPWM	Sinusoidal Pulse Width Modulation
APF	Active Power Filter
PF	Passive Filter
LPF	Low-Pass Filter
DC	Diode-Clamped
FC	Flying Capacitor
FFT	Fast Fourier Transform

Symbol	Description	Typical Value/Unit
S	Rated apparent power	VA
V_{LL}	RMS line-to-line voltage	400 V
V_{ph}	RMS phase voltage	$V_{LL}/\sqrt{3}$
V_{dc}	DC-link voltage	48 V/bridge
f_{sw}	Switching frequency	5 kHz
f_g	Grid frequency	50 Hz
Z_b	Base impedance ($=V_{ph}^2/S$)	Ω
C_b	Base capacitance	F
L_a	Converter-side inductance	1.0 mH
L_b	Grid-side inductance	0.3 mH
C_f	Filter capacitance	17.6 µF
R_f	Damping resistance	3 Ω
f_{res}	Resonant frequency	2.3 kHz
I_{rated}	Rated RMS current	A
$\Delta I_{L,max}$	Max inductor current ripple	10% of I_{rated}
K_p	Proportional gain	0.5
K_i	Integral gain	50
$i_a(s)$	Converter-side current (Laplace)	A
$i_2(s)$	Grid-side current (Laplace)	A
$i_c(s)$	Capacitor current (Laplace)	A
$v_i(s)$	Inverter voltage (Laplace)	V
$v_c(s)$	Capacitor voltage (Laplace)	V
$v_g(s)$	Grid voltage (Laplace)	V
s	Laplace variable	rad/s

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