

Article

Contribution to the Development of a Smart Ultrasound Scanner: Design and Analysis of the High-Voltage Power Supply of the Transmitter

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Abstract: A smart ultrasound scanner plays an important role in the transition to point-of-care imaging. DC–DC bipolar converters are essential in the generation of the ultrasound burst signal as they power the piezoelectric transducer. The conventional bipolar converter has minimal output gain and high-voltage stress, and the longer duty cycle on the semiconductors produces high conduction losses and reduces the efficiency of the system. The transmitter supply voltage is minimal, necessitating the use of high-gain bipolar converters. This proposed study is concerned with the development of an improved high-output voltage gain symmetric bipolar DC–DC converter topology which may be suitable for applications such as powering a smart ultrasound scanner transmitter. The proposed converter combines the conventional single-ended primary inductor converter (SEPIC) with a voltage multiplier cell (VMC) to improve voltage gain, transistor duty cycle, efficiency, and reliability. The present study describes the working principle of the proposed converter. The analysis of the voltage gain is carried out in continuous current mode (CCM) and discontinuous current mode (DCM), taking into account the nonidealities of the device. The simulation of the proposed system is carried out in the numerical environment Matlab/Simulink in order to verify its characteristics. A prototype model is realized and the experimental study presented validates the theoretical arguments and simulations. Due to the advantages of continuous input current, self-balancing bipolar outputs, and small component size, the proposed converter is a suitable choice for smart ultrasound transmitters.

Keywords: SEPIC-Cuk converter; high-voltage gain; symmetrical bipolar voltage; ultrasound scanner



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1. Introduction

Ultrasound imaging is a widely used technique for diagnostic purpose because it is a nonionizing, real-time, noninvasive, and inexpensive imaging modality [1–3]. Especially, point-of-care ultrasound systems have been used to bring modern medical imaging technology to remote places like rural areas, making the diagnostics faster. These systems leverage the power and resources of a mobile/tablet to process, display, and transfer ultrasound images. This small equipment is typically powered by a lithium-ion battery or from a USB source. However, the performance of point-of-care ultrasound systems suffers

from a limited number of ultrasonic array transducer elements, overheating, and battery issues, thereby affecting the sensitivity and resolution of such ultrasound systems [4,5]. To overcome overheating and battery issues, manufacturers need to use cooling systems such as fans and aluminum heat pipe structures even though the internal structures of point-of-care ultrasound systems are much smaller than conventional benchtop ultrasound machines [4].

The whole architecture, illustrated in Figure 1, mainly consists of a piezoelectric transducer, a high-voltage (HV) switch, a controller, an imaging system, and a power supply. The basic principle for an ultrasound imaging system is to transmit an ultrasound burst signal into the area of interest of the organ, receive echoes, and process for imaging [6]. The piezoelectric element is ceramic, and has the property to transform an electrical signal into an ultrasound pressure wave and vice versa, so it serves as both transmitter and receiver [7]. To excite these elements, typically, the ultrasound sensors consist of many piezoelectric elements and use a DC–DC converter to generate high-voltage (HV) bipolar pulses from low-voltage control logic inputs (up to 80 V) and high frequencies (2–20 MHz) [8]. A number of researchers have developed prototypes of portable ultrasound scanners that supply variable symmetric bipolar voltages to the probes [9–11]. Voltages of up to ± 80 V are obtained from low-voltage sources in a single conventional bipolar converter stage. Unfortunately, the supply voltage level is low, and for high-voltage applications, the voltage gain should be high. Also, the input current ripple of the converter should be low to reduce output power fluctuations and increase the life of the supply. Chip manufacturers are also important sources of knowledge and expertise [12,13], as they are the main producers of design notes. They also provide guidance on system design, but component integration can be difficult. For example, datasheets may be incomplete or source code may not be available (e.g., Texas Instruments swroop-smartprobe reference design files). However, most of the power dissipation and overheating problems come from the DC–DC converter and reduce the efficiency of the system [14]. To optimize the high-voltage design for low power consumption, Rathod and al. [15] advocated for electrical impedance matching to improve the level of energy transferred to the transducer. Therefore, to improve the operation of the system in terms of voltage gain, efficiency, and lifetime, a high-voltage bipolar DC–DC converter with high efficiency and low input current ripple should be used.

Basically, the conventional bipolar nonisolated DC–DC converters have been used extensively in high-voltage bipolar DC–DC converters because of their advantages, such as simplicity, ease of control, and continuous input current. Their component count is also less in comparison with the isolated converter topology [16]. However, this high-duty cycle produces high conduction loss in the active switch and diode reverse recovery loss. Additionally, the switch voltage stress is also high, which is equal to the output voltage [12,13,17]. Isolated converters, such as forward, flyback, half-bridge, full-bridge, and push–pull types, can provide a high voltage gain by increasing the transformer's turns ratio. However, there are some significant issues such as leakage inductance, core saturation, thermal effect, high-voltage spikes across the switches, a high number of switching devices and transformers, more isolated sensors, complicated control schemes, and huge size that also make it costly compared to nonisolated converters [18–23]. Consequently, the power dissipation is high, increasing the switching losses and noise, further degrading the system performance. Therefore, considering the requirements in smart ultrasound scanners [24–26], nonisolated converters are preferred.

While many topologies can meet high gain requirements, most have a longer duty cycle, posing a risk to the inductor current saturation and reducing converter performance [27–33]. Extensive research has been carried out to develop bipolar high-gain converters that overcome the drawbacks of ordinary bipolar converters. As a simple technique to enhance the voltage gain of the conventional bipolar converter, switched capacitor/switched inductor voltage multiplier cells (VMCs) are used [17]. However, in these topologies, the metal oxide semiconductor field effect transistor (MOSFET) is connected in series with the power source at the input, which inevitably leads to pulsing input current

and higher conduction losses. Some more competitive ones are surveyed here. In [34], the analysis and control of a step-up converter using the winding cross-coupled inductor approach for DC microgrid applications is presented. This converter has an extremely high gain with a low voltage load on the semiconductors. Leakage energy is recovered via the passive clamp circuit. The large number of power diodes and capacitors is the main disadvantage of this structure. Using three winding coupled inductors and VMC, a single switch ultrahigh step-up DC–DC converter was proposed in [35]. Low diode reverse recovery, low duty cycle, and high efficiency are the main advantages of this topology. However, it suffers from high-input current ripple, and to solve this problem, an RC low pass filter is used. A novel bipolar output converter was proposed in [36]. This converter possesses very simple circuit configuration and can achieve a high step-up voltage gain by adopting an active switched inductor network. By reducing the ripple of the input current, a DC–DC converter topology was proposed in [37] to provide bipolar output voltages in quadratic form with equal and different voltage levels and common ground. Its disadvantage is the use of two power switches with simultaneous operation. A symmetrical multilevel DC–DC boost converter with ripple reduction structure was also analyzed by [38]. The advantages of this topology are high voltage gain, low switch stress, and the ability to reduce the input current ripple and capacitor voltage ripple. In order to further increase the output voltage with low duty cycle, the coupled inductor is combined with VMC by [39]. Continuous input current with low ripple, common ground between output and input ports, low voltage stress across semiconductors, low number of components, high voltage gain, and high efficiency are the main advantages of the proposed converter. In [40], the proposed structure could achieve higher voltage gain by using magnetic coupling and VMC. A power MOSFET with low resistance was used to reduce conduction losses.

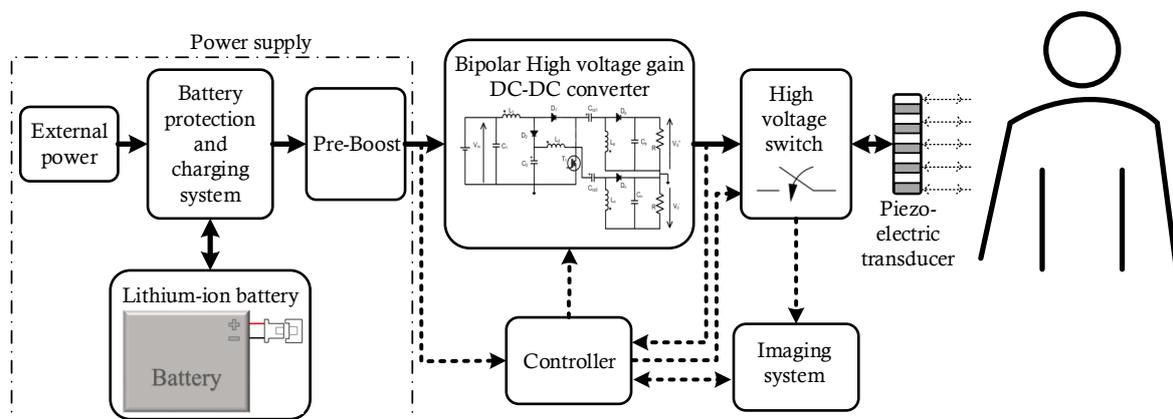


Figure 1. Representative block diagram of usage case of smart ultrasound scanner.

This paper focuses on the design and analysis of a compact, nonisolated symmetrical high-voltage gain supply for powering a smart ultrasound scanner transmitter. This design generates a programmable bipolar supply up to ± 80 V, from a very low input voltage in a single stage. The converter has been designed to offer continuous input current using only a single active switch and to allow a relatively reduced voltage stress across all power semiconductors of the DC–DC converter. Hence, this paper contributes the following:

- Minimization of the symmetry error;
- Wide range of voltage levels with high accuracy;
- Optimization of energy transit;
- Continuity of service.

The rest of the paper is organized as follows: Section 2 describes the study system and presents the novel DC–DC converter that constitutes the originality of this study. Section 3 presents the design considerations. Section 4 provides a theoretical comparative analysis of the proposed converter, highlighting the efficiency and voltage gain. Section 5 presents the simulation and experimental results. Lastly, Section 6 concludes the paper.

2. Converter Configuration

2.1. Main Circuit

The proposed DC–DC converter for powering the transmitter of a smart ultrasound scanner is a new structure of a nonisolated symmetrical bipolar DC–DC converter with high voltage gain, based on the SEPIC–Cuk topology. This modified SEPIC–Cuk converter (MSC) has a single input port and two symmetrical output ports, as shown in Figure 2a. It uses a single switching node, common to both SEPIC and Cuk power stages, to provide corresponding positive and negative ground referenced outputs. The converter is controlled by the duty cycle of the switch T_1 and has the same voltage gain for each of the positive and negative output ports, providing step-down and step-up conversion. Like other switched mode DC–DC power supplies, the MSC exchanges energy between inductors (L_1, L_2, L_p and L_n) and capacitors ($C_1, C_2, C_{CP1}, C_{CP2}, C_p$ and C_n) to convert from one voltage to another.

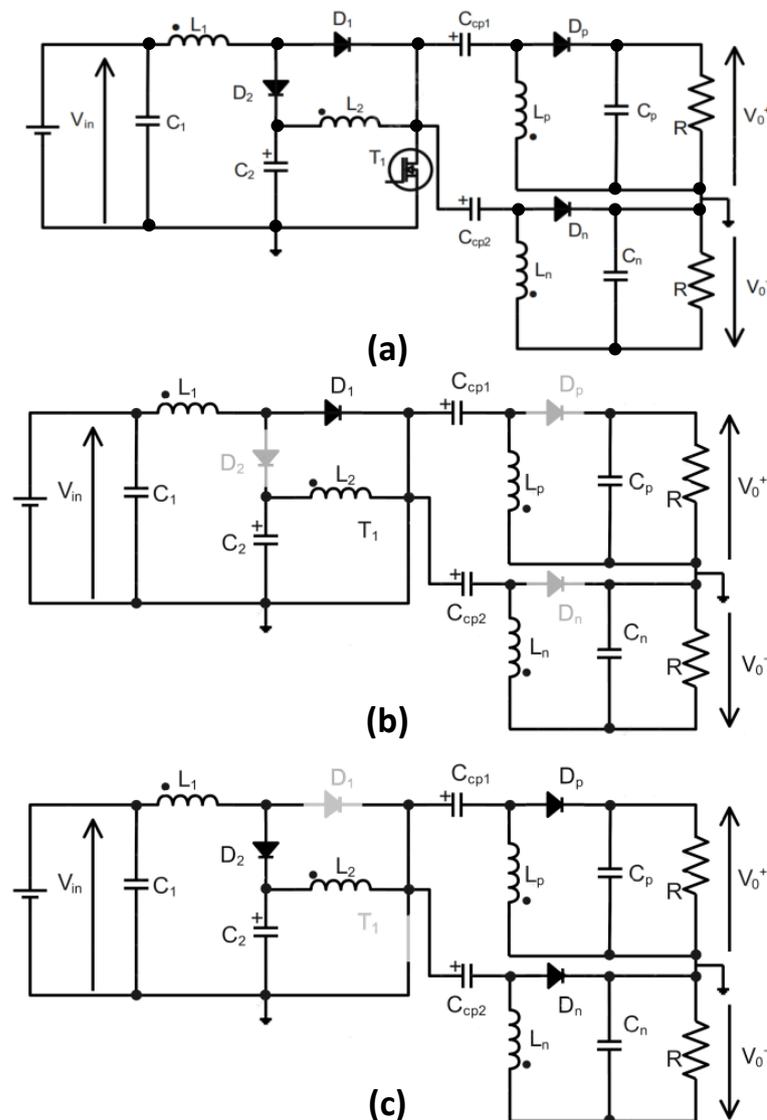


Figure 2. Power circuit of (a) MSC, (b) MSC in mode-A, and (c) MSC in mode-B.

2.2. Continuous Conduction Mode (CCM) Operation and Analysis

The continuous conduction mode (CCM) of the MSC presents two operations, mode-A and mode-B, as illustrated in Figure 2. All capacitors are considered as voltage sources and the semiconductors are considered ideals for the theoretical analysis. The state of

transistor T_1 is controlled by voltage pulses to its gate, with the corresponding duty cycle k (see Figure 3a).

(1) Mode-A [$t_0 \ t_1$]: At t_0 , transistor T_1 is conducting and the diodes D_2, D_p , and D_n are blocked. The input inductor L_1 is charged by the input voltage V_{in} through the diode D_1 . The inductor L_2 takes energy from the capacitor C_2 . The inductors L_p and L_n take energy from the coupling capacitors C_{cp1} and C_{cp2} . The output currents to the loads are supplied by capacitors C_p and C_n . The simplified schematic while T_1 is conducting (ON state) is shown in Figure 2b. The characteristic waveforms of each component in mode-A are presented in Figure 3a.

By applying the Kirchhoff voltage law (KVL) to the MSC power circuit in Figure 2, we obtain the following:

$$\begin{cases} V_{L1} = V_{in} - V_{D1}; \\ V_{L2} = V_{C2}; \\ V_{Lp} = V_{Ccp1}; \\ V_{Ln} = V_0^- + V_{Ccp2}; \end{cases} \tag{1}$$

where V_{L1}, V_{L2}, V_{Lp} , and V_{Ln} are, respectively, the voltages across the inductors L_1, L_2, L_p , and L_n . V_{C2}, V_{Ccp1} , and V_{Ccp2} are the voltages across the capacitors C_2, C_{CP1} , and C_{CP2} , respectively. V_0^- is the negative output voltage and V_{D1} is the diode forward voltage of D_1 .

(2) Mode-B [$t_1 \ t_2$]: At t_1 , transistor T_1 is turned off and the diodes D_2, D_p , and D_n are conducting. All four inductors are demagnetized. The inductor L_1 , along with input voltage V_{in} , charges the capacitor C_2 . The combination of inductor L_2 and capacitor C_2 charges both C_{CP1} and C_{CP2} . At the same time, inductors L_p and L_n discharge through the loads in positive output and negative output, respectively. The characteristic waveforms of each component in mode-B are presented in Figure 3a.

From the analysis of this operating mode, the following expressions are obtained:

$$\begin{cases} V_{L1} = V_{in} - V_{C2} - V_{D2}; \\ V_{L2} = V_{C2} - V_{Ccp1} - V_{Dp} - V_0^+; \\ V_{L2} = V_{C2} - V_{Ccp2} - V_{Dn}; \\ V_{Lp} = -V_0^+ - V_{Dp}; \\ V_{Ln} = V_0^- - V_{Dn}; \end{cases} \tag{2}$$

where V_{D2}, V_{Dp} , and V_{Dn} are the diode forward voltages of D_1, D_2 , and D_3 . V_0^+ is the positive output voltage.

The switching transistor is assumed ideal and the voltages across inductors and diodes assume no ohmic losses. All four diodes have the same characteristics ($V_{D1} = V_{D2} = V_{Dp} = V_{Dn} = V_D$). By applying the inductor volt second balance (IVSB) principle for the inductors L_1, L_2, L_p , and L_n ,

$$k(V_{in} - V_D) + (1 - k)(V_{in} - V_{C2} - V_D) = 0, \tag{3}$$

$$\frac{V_{C2}}{V_{in} - V_D} = \frac{1}{(1 - k)}, \tag{4}$$

$$k V_{C2} + (1 - k)(V_{C2} - V_{Ccp1} - V_D - V_0^+) = 0 \tag{5}$$

$$V_{Ccp1} = \frac{V_{C2}}{(1 - k)} - V_D - V_0^+, \tag{6}$$

$$k V_{Ccp1} - (1 - k)(-V_0^+ - V_D) = 0, \tag{7}$$

$$V_{Ccp1} = \frac{(1 - k)(V_0^+ + V_D)}{k}. \tag{8}$$

By combining (6) and (8), we obtain

$$V_{C2} = \frac{1-k}{k}(V_0^+ + V_D). \tag{9}$$

Equation (9) in (4) gives

$$\frac{V_0^+ + V_D}{V_{in} - V_D} = \frac{k}{(1-k)^2}, \tag{10}$$

$$k V_{C2} + (1-k)(V_{C2} - V_{Ccp2} - V_D) = 0, \tag{11}$$

$$V_{Ccp2} = \frac{V_{C2}}{1-k} - V_D, \tag{12}$$

$$k(V_0^- + V_{Ccp2}) + (1-k)(V_0^- - V_D) = 0, \tag{13}$$

$$V_{Ccp2} = \frac{(1-k)V_D - V_0^-}{k}. \tag{14}$$

Equations (12) and (14) give

$$V_{C2} = \frac{(1-k)}{k}(V_D - V_0^-). \tag{15}$$

With (4) and (15), we obtain

$$\frac{V_0^- - V_D}{V_{in} - V_D} = -\frac{k}{(1-k)^2}. \tag{16}$$

From (10) and (16), we notice that the maximum duty cycle occurs at $V_{in,min}$ and the minimum duty cycle occurs at $V_{in,max}$. If we ignore the diode drop, we arrive at the ideal voltage gains of the proposed converter in CCM mode as represented by

$$\begin{cases} G_{p-CCM} = \frac{V_0^+}{V_{in}} = \frac{k}{(1-k)^2}, \\ G_{n-CCM} = \frac{V_0^-}{V_{in}} = -\frac{k}{(1-k)^2}. \end{cases} \tag{17}$$

From the voltage gains given by these expressions, using the proposed converter in CCM, we are able to obtain two symmetrical outputs with the same gain.

2.3. Discontinuous Conduction Mode (DCM) Operation and Analysis

The MSC can be operated in discontinuous conduction mode (DCM) as the currents through inductors reach zero levels individually or together as respective diodes, or both become reverse-biased. The DCM operation of MSC is divided into three modes: modes A, B, and C. Modes A and B have operating principles similar to CCM, whereas mode-C is a prolongation of mode-B. Based on the inductor current and respective diode operating state, the MSC can work in three different possible DCM modes as mode-I, mode-II, and mode-III. In mode-I, the inductor current $I_{L1,min}$ individually reaches zero level as diode D_2 becomes reverse-biased. In mode-II, the diode D_2 is forward-biased and the diodes D_n and D_p become reversely biased due to inductors current $I_{L2,min}$, $I_{Ln,min}$, and $I_{Lp,min}$. Similarly in mode-III, diodes D_2 , D_n , and D_p become reverse-biased by the effect of current through inductors L_1 , L_2 , L_n , and L_p . The power circuitry with the respective current paths in three possible DCM modes is shown in Figure 2c. Based on the three different possible modes (discontinuous inductor current mode (DICM), discontinuous capacitor voltage mode (DCVM), and discontinuous quasi-resonant mode (DQRM)) [41], MSC has three different voltage gains in DCM. Hence, for simplicity, the MSC is analyzed with mode-II

DCM mode. The respective characteristic waveforms of each component are shown in Figure 3b.

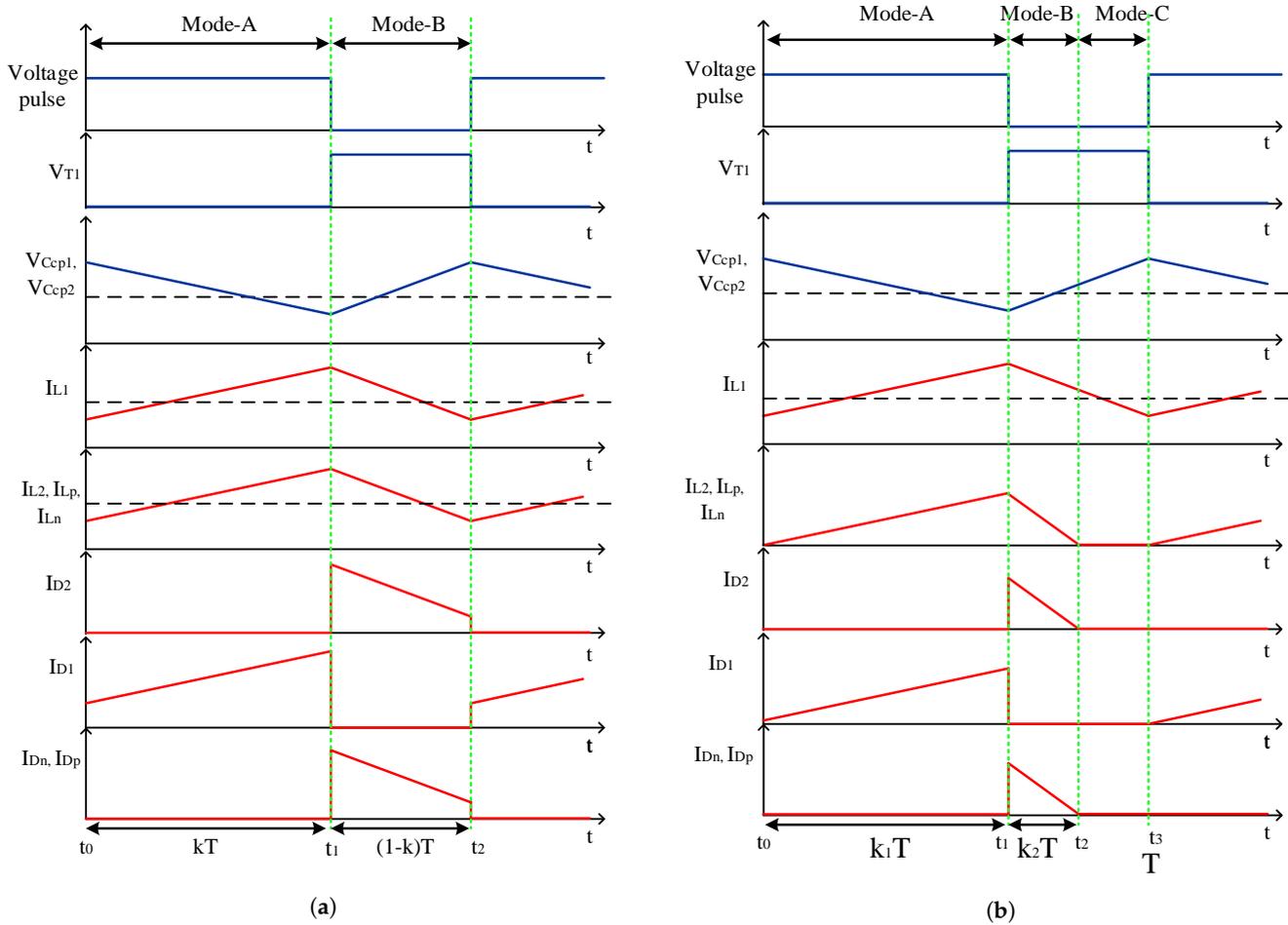


Figure 3. MSC waveforms: (a) CCM; (b) DCM.

(1) **Mode-A** [t_0 t_1]: In this mode, the transistor is turned on and the equivalent circuit is the same as mode-A of CCM (see Figure 3b). The peak amplitude current through inductors L_1 , L_2 , L_n , and L_p can be expressed as

$$\begin{cases} I_{L1,max} = k_1 T \frac{(V_{in} - V_{D1})}{L_1}; \\ I_{L2,max} = k_1 T \frac{V_{C2}}{L_2}; \\ I_{Lp,max} = k_1 T \frac{V_{Ccp1}}{L_p}; \\ I_{Ln,max} = k_1 T \frac{(V_0^- + V_{Ccp2})}{L_n}. \end{cases} \tag{18}$$

(2) **Mode-B** [t_1 t_2]: In this mode, the transistor is turned off and the equivalent circuit is the same as mode-B of CCM (see Figure 3b). The peak amplitude current through inductors L_1 , L_2 , L_n , and L_p can be expressed as

$$\begin{cases} I_{L1,min} = -k_2 T \frac{(V_{in} - V_{C2} - V_{D2})}{L_1}; \\ I_{L2,min} = k_2 T \frac{(V_{C2} - V_{Ccp1} - V_{Dp} - V_0^+)}{L_2}; \\ I_{L2,min} = -k_2 T \frac{(V_{C2} - V_{Ccp2} - V_{Dn})}{L_2}; \\ I_{Lp,min} = k_2 T \frac{(V_0^+ + V_{Dp})}{L_p}; \\ I_{Ln,min} = -k_2 T \frac{(V_0^- - V_{Dn})}{L_n}. \end{cases} \tag{19}$$

(3) Mode-C [t_2 t_3]: In this mode, the switching transistor is turned off. At the end of this mode, the energies stored in inductors L_2 , L_n , and L_p are zero. Hence, only energy stored in capacitors C_p and C_n is discharged to the loads connected to the positive and negative output ports, respectively. The equivalent circuit of mode-C-II is shown in Figure 3b. Therefore, from (18) and (19),

$$k_2 = k_1 \frac{V_{C2}}{V_0^+} = -k_1 \frac{V_{C2}}{V_0^-}. \tag{20}$$

From Figure 3b, during operation, the inductors L_2 and L_p only supply energy to the capacitor C_p and the positive output during mode-B. Similarly, L_2 and L_n only supply energy to capacitor C_n and the negative output during mode-B. For the rest of the time, only capacitors C_p and C_n ensure the continuity of the energy supply to the respective outputs. The energy stored in capacitors C_n and C_p is expressed as follows:

$$\begin{cases} Q_{Cp} = T I_{Cp} = \frac{1}{2}k_2 T (\frac{1}{2}I_{L2} + I_{Lp})_{max} - T I_0^+; \\ Q_{Cn} = T I_{Cn} = -\frac{1}{2}k_2 T (\frac{1}{2}I_{L2} + I_{Lp})_{max} - T I_0^-. \end{cases} \tag{21}$$

The average capacitor's C_p and C_n currents during each switching period are given by,

$$\begin{cases} I_{Cp} = \frac{1}{2}k_2(\frac{1}{2}I_{L2} + I_{Lp})_{max} - I_0^+; \\ I_{Cn} = -\frac{1}{2}k_2(\frac{1}{2}I_{L2} + I_{Lp})_{max} - I_0^-. \end{cases} \tag{22}$$

By substituting (18) and (20) in (22), I_{Cp} and I_{Cn} are derived as follows:

$$\begin{cases} V_{Ccp1} k^2 T (\frac{V_{Ccp1} + V_{C2}}{L}) = \frac{V_0^+}{R}; \\ V_{Ccp2} k^2 T (\frac{V_{Ccp2} + V_{C2}}{L}) = -\frac{V_0^-}{R}. \end{cases} \tag{23}$$

From (4)–(17), (23) is rearranged as

$$\begin{cases} G_{p-DCM} = \frac{V_0^+}{V_{in}} = \sqrt{\frac{k^2}{(1-k)^2 \tau}}; \\ G_{n-DCM} = \frac{V_0^-}{V_{in}} = -\sqrt{\frac{k^2}{(1-k)^2 \tau}}; \end{cases} \tag{24}$$

where $\tau = \frac{L}{RT}$, is the normalized inductor time constant.

Equation (24) represents the voltage gain of the MSC in DCM. Using (17) and (24), the boundary for CCM and DCM is derived as follows:

$$\tau_B = (1 - k)^2, \tag{25}$$

where τ_B is the boundary normalized inductor time constant.

2.4. Input and Output Currents Relationship

Assuming 100% efficiency, we arrive at the following expression:

$$P_o = P_{in}, \tag{26}$$

$$V_{01}I_{01} + V_{02}I_{02} = V_{in}I_{in}, \tag{27}$$

$$V_0^+I_0^+ + V_0^-I_0^- = V_{in}I_{in}, \tag{28}$$

where I_0^+ and I_0^- are currents through the positive and negative outputs, respectively.

However, for smart ultrasound scanner applications, the DC–DC converter has a symmetric circuit. Therefore, output voltages and currents are symmetries ($V_0^- = -V_0^+$ and $I_0^- = -I_0^+$),

$$2V_0^+I_0^+ = V_{in}I_{in}. \tag{29}$$

Using (17), the relationship between the average input and output currents can be expressed as

$$I_{in} = 2 \frac{V_0^+}{V_{in}} I_0^+ = 2 \frac{k}{(1-k)^2} I_0^+; \tag{30}$$

$$\begin{cases} I_0^+ = \frac{(1-k)^2}{2k} I_{in}; \\ I_0^- = -\frac{(1-k)^2}{2k} I_{in}. \end{cases} \tag{31}$$

3. Design Considerations

To design, ensure proper operation, and avoid damaging the proposed converter, we need to define the technical characteristics of each component. The design process involved analyzing the converter in the ON or OFF state to obtain equations that describe the currents through, and the voltages across, many components. Small ripple approximations are applied to simplify the derivations in the capacitor and inductor equations.

3.1. Inductors Selection

The selection of an inductor depends on the duty cycle, switching frequency, and resistive load. When the mosfet transistor is conducting, the voltage across the inductor L_1 equals

$$V_{L1} = L \frac{di_{L1}}{dt}. \tag{32}$$

Using KVL and assuming zero loss in mosfet, the peak-to-peak current can be calculated as follows:

$$I_{L1,p2p} = \Delta I_{L1} = \frac{kV_{in}}{L_1 f_{sw}}, \tag{33}$$

where f_{sw} is the switching frequency of the regulator and is defined as

$$f_{sw} = \frac{1}{T_{sw}}. \tag{34}$$

Using (33), the inductor value can be obtained as follows:

$$L_1 = \frac{kV_{in}}{\Delta I_{L1} f_{sw}}. \tag{35}$$

The maximum and minimum current in inductor L_1 can be expressed as

$$I_{L1,max} = I_{L1} + \frac{\Delta I_{L1}}{2} = I_{in} + \frac{\Delta I_{L1}}{2}, \tag{36}$$

$$I_{L1,min} = I_{L1} - \frac{\Delta I_{L1}}{2} = I_{in} - \frac{\Delta I_{L1}}{2}. \tag{37}$$

Using (30), (36) and (37),

$$\begin{aligned} I_{L1,max} &= 2 \frac{k}{(1-k)^2} I_0^+ + \frac{\Delta I_{L1}}{2} \\ &= 2 \frac{k}{(1-k)^2} I_0^+ \left(1 + \frac{(\Delta I_{L1})_{\%}}{2} \right), \end{aligned} \tag{38}$$

$$\begin{aligned} I_{L1,min} &= 2 \frac{k}{(1-k)^2} I_0^+ - \frac{\Delta I_{L1}}{2} \\ &= 2 \frac{k}{(1-k)^2} I_0^+ \left(1 - \frac{(\Delta I_{L1})_{\%}}{2} \right), \end{aligned} \tag{39}$$

where $(\Delta I_{L1})\%$ is the maximum allowed ripple in the inductor in percent.

With the symmetric resistive outputs, the maximum and minimum peak values of inductor current I_{L1} are derived by combining (17), (30) and (33) as follows:

$$I_{L1,max} = \frac{2k^2 V_{in}}{(1-k)^4 R} + \frac{kV_{in}}{2L_1 f_{sw}}, \tag{40}$$

$$I_{L1,min} = \frac{2k^2 V_{in}}{(1-k)^4 R} - \frac{kV_{in}}{2L_1 f_{sw}}. \tag{41}$$

To operate the converter in CCM mode, the inductor current must remain positive. To determine the boundary condition between CCM and DCM, $I_{L1,min}$ is set to zero in (41):

$$(L_1)_{crit} = \frac{(1-k)^4 R}{4k f_{sw}}. \tag{42}$$

Equation (42) gives the critical value of inductor L_1 below which ($L_1 < (L_1)_{crit}$) MSC works in DCM mode and works in CCM as $L_1 > (L_1)_{crit}$.

With the same concept, the ripple content of I_{L2} can be derived from (4) as follows:

$$I_{L2,p2p} = \Delta I_{L2} = \frac{kV_{C2}}{L_2 f_{sw}} = \frac{kV_{in}}{(1-k) L_2 f_{sw}}. \tag{43}$$

The MSC has a cascaded connection of boost followed by an SEPIC-Cuk converter to achieve high voltage gain with higher efficiency and reliability due to its simplicity, the low voltage stress of the switches, and the ability to step up the low voltage input. However, the number of components can be excessive. As SEPIC-Cuk receives the input from the boost converter, the inductor L_2 current can be derived as follows:

$$\begin{cases} V_{C2} I_{L2} = 2 \frac{V_0^2}{R}, \\ I_{L2} = 2 \frac{V_0^2}{V_{C2} R} = 2 \frac{k^2 V_{in}}{(1-k)^3 R}. \end{cases} \tag{44}$$

The maximum and minimum peak values of the inductor current I_{L2} can be derived as follows:

$$I_{L2,max} = I_{L2} + \frac{\Delta I_{L2}}{2} = \frac{k^2 V_{in}}{(1-k)^3 R} + \frac{kV_{in}}{2(1-k)L_2 f_{sw}}, \tag{45}$$

$$I_{L2,min} = I_{L2} - \frac{\Delta I_{L2}}{2} = \frac{k^2 V_{in}}{(1-k)^3 R} - \frac{kV_{in}}{2(1-k)L_2 f_{sw}}. \tag{46}$$

To determine the boundary condition between CCM and DCM, $I_{L2,min}$ is set to zero in (46):

$$(L_2)_{crit} = \frac{(1-k)^2 R}{2k f_{sw}}. \tag{47}$$

With the same concept, the current ripple of inductor L_p is derived from (17) and (20) as follows:

$$I_{Lp,p2p} = \Delta I_{Lp} = \frac{kV_{Ccp1}}{L_p f_{sw}} = \frac{kV_{in}}{(1-k) L_p f_{sw}}, \tag{48}$$

$$I_{Ln,p2p} = \Delta I_{Ln} = \frac{kV_{Ccp2}}{L_n f_{sw}} = \frac{kV_{in}}{(1-k) L_n f_{sw}}. \tag{49}$$

In MSC, the current through inductor L_p is load current and can be derived as follows:

$$I_{Lp} = \frac{V_0^+}{R} = \frac{kV_{in}}{(1-k)^2 R}. \tag{50}$$

The maximum and minimum values of the inductor current I_{Lp} are

$$\begin{aligned}
 I_{Lp,max} &= I_{Lp} + \frac{\Delta I_{Lp}}{2} \\
 &= \frac{k^2 V_{in}}{(1-k)^2 R} + \frac{k V_{in}}{2(1-k)L_p f_{sw}}, \tag{51}
 \end{aligned}$$

$$\begin{aligned}
 I_{Lp,min} &= I_{Lp} - \frac{\Delta I_{Lp}}{2} \\
 &= \frac{k^2 V_{in}}{(1-k)^2 R} - \frac{k V_{in}}{2(1-k)L_p f_{sw}}. \tag{52}
 \end{aligned}$$

To determine the boundary condition between CCM and DCM, $I_{Lp,min}$ is set to zero in (46):

$$(L_p)_{crit} = \frac{(1-k) R}{2f_{sw}}. \tag{53}$$

Similarly,

$$(L_n)_{crit} = \frac{(1-k) R}{2f_{sw}}. \tag{54}$$

We can note that the inductances required will be largest at the minimum output power because the factor R appears in the denominator for the inductor equations.

3.2. Capacitors Selection

The value of capacitors depends on the voltage ripple (ΔV_{C1} in C_1 , ΔV_{C2} in C_2 , $\Delta V_{C_{cp1}}$ in C_{cp1} , $\Delta V_{C_{cp2}}$ in C_{cp2} , ΔV_{C_p} in C_p , and ΔV_{C_n} in C_n), duty cycle, load resistance, and switching frequency.

The coupling capacitors C_{cp1} and C_{cp2} must be able to handle voltages equal to $V_{in,min}$. The peak-to-peak voltage across the coupling capacitor can be calculated as follows:

$$\Delta V_{C_{cp}} = \frac{(1-k) I_{in}}{f_{sw} C_{C_{cp}}} = \frac{k I_{out}}{(1-k) f_{sw} C_{C_{cp}}}. \tag{55}$$

The ripple across the coupling capacitor C_{cp} is determined by its capacitance and also its equivalent series resistance (ESR). Assuming a linear relationship between the two sources of ripple, we arrive at

$$\Delta V_{C_{cp}} \leq \frac{k I_{out}}{(1-k) f_{sw} C_{C_{cp}}} + ESR * \max(I_{in,peak}, I_{out,peak}). \tag{56}$$

The selection of the output capacitors C_p and C_n is also made to obtain the desired voltage ripple value. Its peak-to-peak value is given by the following:

$$\Delta V_{C_p} = \frac{k V_{C_p}}{R C_p f_{sw}}. \tag{57}$$

$$\Delta V_{C_n} = \frac{(1-k) |V_{C_n}|}{8 L_n C_n f_{sw}^2}. \tag{58}$$

It is recommended to use a ceramic capacitor to keep the ESR losses as small as possible.

With the design specifications given in Table 1, the simulation and hardware prototype parameters of each component are listed in Table 2.

Table 1. Design specifications.

Parameters	Specifications
Input voltage	5 V
Output voltage	Bipolar and symmetrical from 50 to 80 V at 25 mA
Switching frequency	250 kHz
Overall system efficiency	≥80%
Voltage symmetry with equal load on both rails	≤2%

Table 2. Simulation and hardware prototype parameters.

Elements	Specifications
Duty cycle	$0.5 \leq k \leq 0.8$
L_1	10 μ H
L_2	470 μ H
L_p, L_n	1.5 mH
T_1	mosfet $V_{DSmax} = 100$ V $R_{DSon} = 58$ m Ω $V_{GS} = 3.2$ V, $T_{off} = 9$ ns
C_2	220 nF
C_p, C_n	2.2 μ F
C_{cp1}	1.65 μ F
C_{cp2}	100 nF
D_1, D_2, D_3, D_4	$V_F = 0.8$ V, $V_{RRM} = 150$ V
C_{in}	10 μ F

4. Efficiency Analysis of the Proposed Converter and Comparison

4.1. Efficiency Analysis of the Proposed Converter Considering Nonideality under CCM

The proposed converter efficiency is analyzed through the equivalent circuit of MSC with nonidealities of circuit components, i.e., internal resistance and forward voltage of the respective components, as shown in Figure 4, where r_{L1}, r_{L2}, r_{Lp} , and r_{Ln} are the ESR of inductors L_1, L_2, L_p , and L_n , respectively. Similarly, r_{D1}, r_{D2}, r_{Dp} , and r_{Dn} are internal resistance, and V_{F1}, V_{F2}, V_{Fp} , and V_{Fn} are the forward-voltage-drop diodes D_1, D_2, D_p , and D_n , respectively, whereas r_T is the forward ON state resistance of a controlled switch T_1 .

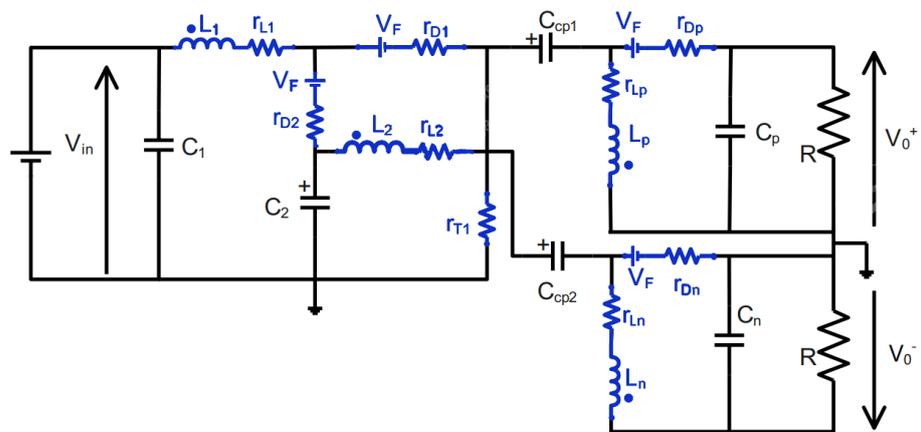


Figure 4. The equivalent circuit of the proposed converter with ESR of inductor, switch, and voltage drop of diodes.

With the consideration of nonidealities in conducting and nonconducting states, the equivalent voltage equations across the four inductors are

$$ON\ STATE \begin{cases} V_{L1} = V_{in} - V_{D1} - V_{r_{L1}} - V_T; \\ V_{L2} = V_{C2} - V_{r_{L2}} - V_T; \\ V_{Lp} = V_{Ccp1} - V_{r_{Lp}} - V_T; \\ V_{Ln} = V_0^- + V_{Ccp2} - V_{r_{Ln}} - V_T. \end{cases} \quad (59)$$

$$OFF\ STATE \begin{cases} V_{L1} = V_{in} - V_{C2} - V_{D2} - V_{r_{L1}}; \\ V_{L2} = V_{C2} - V_{Ccp1} - V_{Dp} - V_0^+ - V_{r_{L2}}; \\ V_{Lp} = -V_0^+ - V_{Dp} - V_{r_{Lp}} - V_{r_{Ln}}; \\ V_{Ln} = V_0^- - V_{Dn}; \end{cases} \quad (60)$$

with

$$\begin{cases} V_T = r_T(I_{L1} + I_{L2} + I_{L3} + I_{L4}); \\ V_{r_{L1}} = r_{L1}I_{L1}; \\ V_{r_{L2}} = r_{L2}I_{L2}; \\ V_{r_{Lp}} = r_{Lp}I_{Lp}; \\ V_{r_{Ln}} = r_{Ln}I_{Ln}; \\ V_{D1} = V_{F1} - r_{D1}I_{L1}; \\ V_{D2} = V_{F2} - r_{D2}I_{L1}; \\ V_{Dp} = V_{F1} - r_{Dp}(\frac{I_{L2}}{2} + I_{Lp}); \\ V_{Dn} = V_{Fn} - r_{Dn}(\frac{I_{L2}}{2} + I_{Ln}). \end{cases} \quad (61)$$

Applying the IVSB principle, the output voltage of MSC in terms of the voltage drop across each component can be expressed by the following:

$$V_0 = \frac{k}{(1-k)^2} V_{in} - \frac{k^2}{(1-k)^2} V_{D1} - \frac{k}{1-k} V_{D2} - \frac{k}{(1-k)^2} V_T - \frac{k}{(1-k)^2} V_{r_{L1}} - \frac{k}{(1-k)} V_{r_{L2}} - kV_{r_{Lp}}. \quad (62)$$

The MSC real voltage gain is derived similarly to the method in the CCM analysis and includes the impact of the nonidealities of components (see Table 2).

From (59)–(62), the real voltage gain G_{real} is given by the following equation:

$$G_{real} = \frac{G}{A + \frac{(1+G)V_F}{G V_{in}} + 2k \frac{r_L}{R} G + B G^2}, \quad (63)$$

where

$$\begin{cases} G = \frac{k}{(1-k)^2}; \\ A = 1 + \frac{r_p}{R} + \frac{1}{1-k} \frac{r_D}{R}; \\ B = \frac{2}{R} (r_1 + r_D + \frac{r_T}{k}). \end{cases} \quad (64)$$

The voltage gain and efficiency of the converter are affected by conduction loss due to the parasitic resistance of the circuit element and switching loss by the semiconductor devices

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{P_{out}}{P_{out} + P^T_{loss} + P^D_{loss} + P^L_{loss} + P^C_{loss}}. \quad (65)$$

Equation (65) gives the relation of output power with efficiency. To evaluate the power losses and efficiency of the MSC, the losses can be calculated for each component.

The power losses in the circuit can be divided into two categories: (1) Conduction losses (P_{cond}); (2) Switching or overlap losses P_{sw} . In this paper, the power loss by capacitors and diode switching losses are not considered.

The total power losses in transistor are equal to

$$P_T = P_{cond} + P_{sw}. \quad (66)$$

The conduction losses in the transistor are given by

$$P_{cond} = I_{T,rms}^2 r_{DS(on)} k_{max}. \tag{67}$$

The switching losses are approximately equal to

$$P_{sw} = \frac{1}{2} V_{DS} I_{T,peak} (\tau_r + \tau_f) f_{sw}, \tag{68}$$

where τ_r and τ_f are the rise and fall time of T .

When T_1 is turned off, the voltage from the drain to the source can be calculated using a KVL:

$$V_{DS} = V_{Ccp} + V_D + V_{out} = V_{Ccp1} + V_{Dp} + V_0^+. \tag{69}$$

Therefore,

$$P_{sw} = \frac{1}{2} (V_{Ccp1} + V_D + V_0^+) I_{T,peak} (\tau_r + \tau_f) f_{sw}, \tag{70}$$

$$P_{sw} = \frac{1}{2} \left(\frac{k + (1 - k)^2}{(1 - k)^2} V_{Ccp1} + V_D \right) I_{T,peak} (\tau_r + \tau_f) f_{sw}. \tag{71}$$

The power loss by inductors can be derived as follows:

$$P_L = r_L I_{L,rms}^2. \tag{72}$$

The diode selected must be able to withstand reverse voltages and average current. The conduction loss in the diode is equal to the diode average current times the forward voltage drop in the diode. Therefore, the diode package must be able to dissipate up to

$$P_D = I_{D,rms} V_D. \tag{73}$$

To improve efficiency (or reduce losses in the diode), a diode with a low forward voltage is recommended. Schottky diodes are good candidates due to their low forward voltage.

The overall efficiency of the MSC is given by

$$\eta = \frac{1}{A + \frac{(1+G)V_F}{G V_{in}} + r_L \frac{2k}{R} G + B G^2} - \frac{P_{sw}}{P_{in}}, \tag{74}$$

where G , A and B are defined in (64).

Figure 5 illustrates the voltage gain of the MSC with the effect of parasitic elements as a function of the duty cycle under different load conditions. In the ideal case, the voltage gain is equal to zero at $k = 0$ and tends to infinity as k approaches one. In the practical case where some small parasitic resistances and loads are presented, the output voltage tends to zero at $k = 1$. In addition, it can be seen that the load limits the maximum voltage gain that the converter can produce. It is advisable not to operate the converter beyond a duty cycle of 0.9 to prevent the converter from reaching the critical point where the gain declines until reaching zero at the unity duty cycle.

Figure 6 shows the overall efficiency of the MSC with the effect of parasitic elements as a function of the duty cycle under different load conditions. It can be seen that to obtain high efficiency, with the same parasitic elements in Figure 5, the converter's load should be reduced. Increasing the load on the converter reduces the efficiency. The efficiency of the converter is high and equal for the selected loads when the duty cycle is less than 0.7, and after that, the efficiency of the converter decreases until it reaches zero at unity duty cycle. It can be seen that the proposed converter has a better efficiency performance when $R_{load} = 100 \Omega$ and the efficiency exceeds 93.4%.

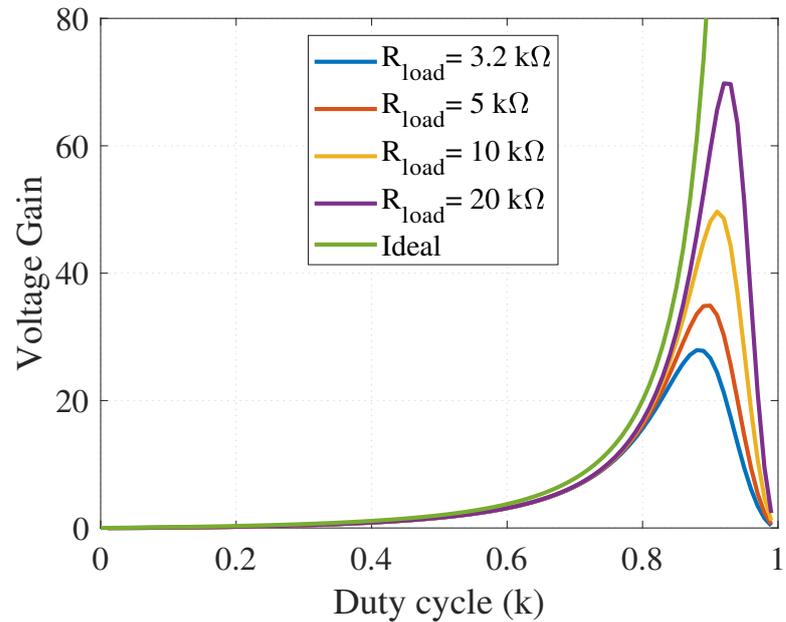


Figure 5. Voltage gain of nonideal proposed converter.

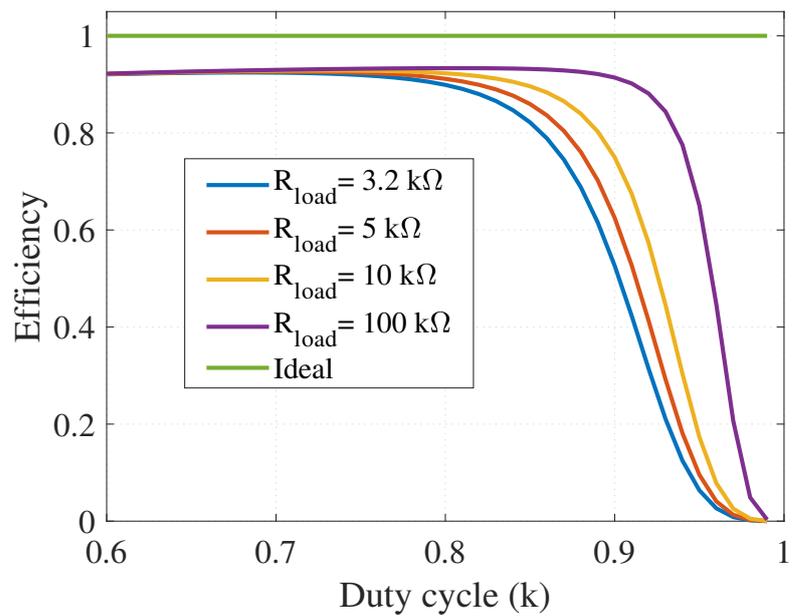


Figure 6. Efficiency graph of nonideal proposed converter.

4.2. Comparison with Recent Similar Converters

The proposed converter is compared with recent similar converters as discussed in the literature. For this comparison, we considered equivalent converters that could be connected to a bipolar output. Table 3 presents a comparison in terms of voltage gain, number of switches, diodes, inductors, and capacitors. The proposed converter is one of the converters that require a minimal number of switches and provides common ground between loads. From Figure 7, it is noticed that for $k \geq 0.65$, the proposed converter gives higher voltage gain compared to other converters.

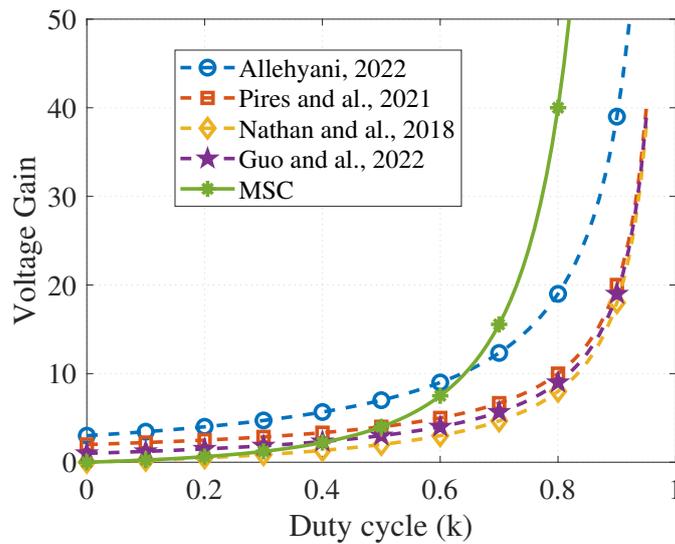


Figure 7. Graph of voltage gain of recent similar converter and MSC versus duty cycle.

Table 3. Comparison between the proposed converter and other high voltage gain converters.

Converter	Voltage Gain	Switch	Diodes	Inductors	Capacitors
[30]	$\frac{2k}{1-k}$	1	2	3	4
[31]	$\frac{2}{1-k}$	1	3	2	4
[36]	$\frac{k+1}{1-k}$	2	2	2	4
[38]	$\frac{3+k}{1-k}$	2	6	2	6
Proposed	$\frac{2k}{(1-k)^2}$	1	4	4	5

Input voltage range, output voltage, efficiency, and output voltage regulation are the most critical parameters in the design of a high-voltage power supply for an ultrasonic transducer. Table 4 compares this work with other realizations. In [9,42], the proposed architectures have a wide input voltage range and specific output voltage levels. In [12,13], the input voltages are fixed at 12 V and they can provide high efficiency. Our proposed architecture has a wide input voltage range and can achieve ±80 V at the output. The output voltage regulation and symmetry are less than others.

Table 4. Comparison of the proposed converter to recent similar solutions.

Work	Input Voltage Range	Output Voltage	Power	Peak Efficiency	Output Voltage Regulation	Voltage Symmetry with Equal Load on Both Rails	Topology
[9]	4.25–5.5 V	±80 V	4 W	80%	±2%	1%	SEPIC-Cuk
[10]	5 V	±50 V	5.6 W	NA *	NA	NA	NA
[11]	3.7 V	±70 V	7.5 W	NA	NA	NA	NA
[12]	12 V	±60 V	6 W	88.2%	±4%	2%	SEPIC-Cuk
[13]	12 V	±75 V	1.5 W	88%	±2%	1%	SEPIC-Cuk
[42]	3.6–8.4 V	±100 V	4 W	75%	±2%	1%	Pre-boost + SEPIC-Cuk
Proposed	4.75–12 V	±80 V	5 W	82%	±1.3%	1.09%	Voltage multiplier cell + SEPIC-Cuk

* NA: Not Available.

5. Results and Discussion

The simulation and experimental results of the proposed bipolar high-voltage gain DC–DC converter were performed to validate the theoretical analysis and also test its functionality. The tests were carried out in accordance with the design specifications and component parameters listed in Tables 1 and 2.

5.1. Simulation Tests

To investigate the operation of the proposed converter, the simulation results were obtained by using Matlab/Simulink software (version R2020b). Figures 8–11 show the simulation results of the input and output voltages and currents, the inductor currents, and the voltage stress and current of diodes and the switch. In addition to voltage and current waveform demonstrations in steady state, voltage and current ripples in each figure are illustrated in detail for demonstration of the accuracy in simulations. The input voltage is 5 V, the switching frequency is 250 kHz, and duty cycle k is between 0.5 and 0.8.

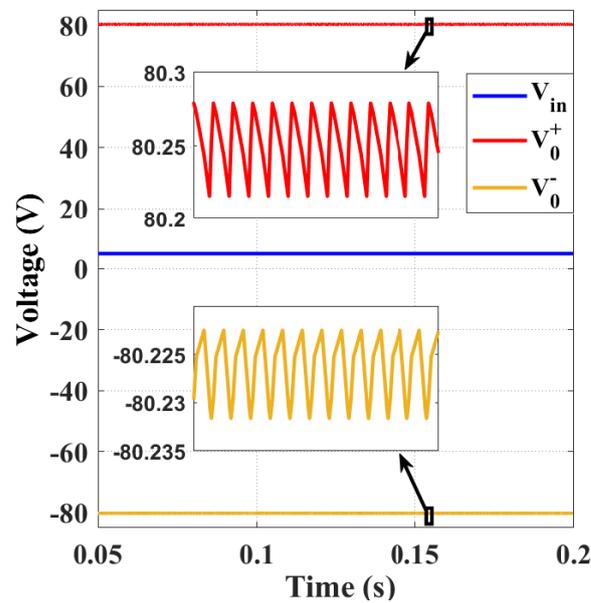


Figure 8. Simulation graph of the input voltage and the symmetrical voltages at the converter output.

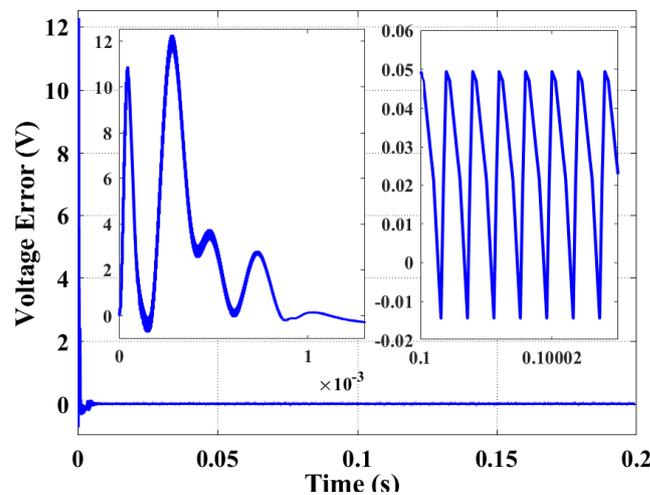


Figure 9. Simulation graph of the symmetrical voltage error at the converter output.

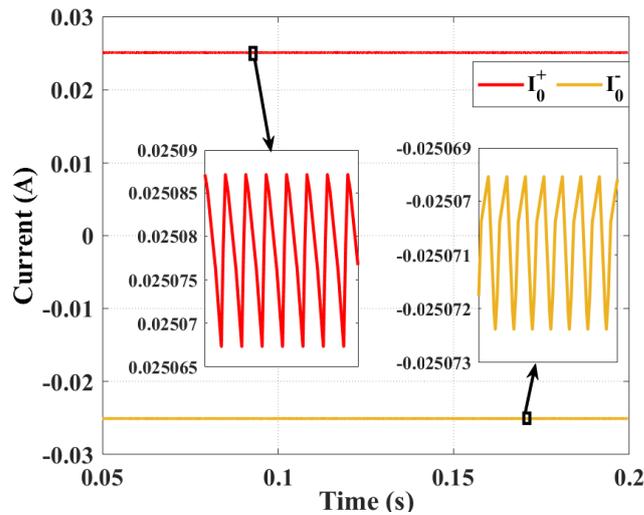


Figure 10. Simulation graph of the converter output currents.

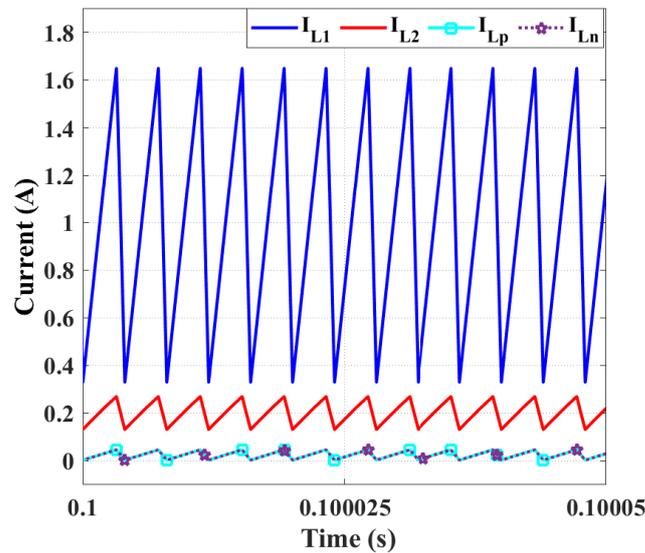


Figure 11. Simulation waveforms of the input and output voltages and currents of the converter.

Figure 8 shows the output ripple of the high-voltage circuit of both negative (V_0^-) and positive (V_0^+) rail at full load. It is shown that the output voltages are settled at +80.25 V and −80.227 V, which are very close to the theoretical values. The ripple is measured at the output capacitor and the peak-to-peak ripple is close to 70 mV. According to Table 1, the output ripple is 0.0875%. The voltage error between the outputs is very low (see Figure 9) and voltage symmetry with an equal load on both rails is less than 1%. Figures 10 and 11 show the output and inductor’s current waveforms; the current decreases linearly when the switch is off and increases linearly when the switch is on, which is consistent with the theoretical analysis.

5.2. Experimental Tests

To experimentally confirm the performance of the proposed converter and the accuracy of the simulation results, a prototype of our converter is designed and tests are performed in the laboratory environment. Figure 12 depicts the proposed converter prototype. The experimental test setup of MSC is shown in Figure 13.

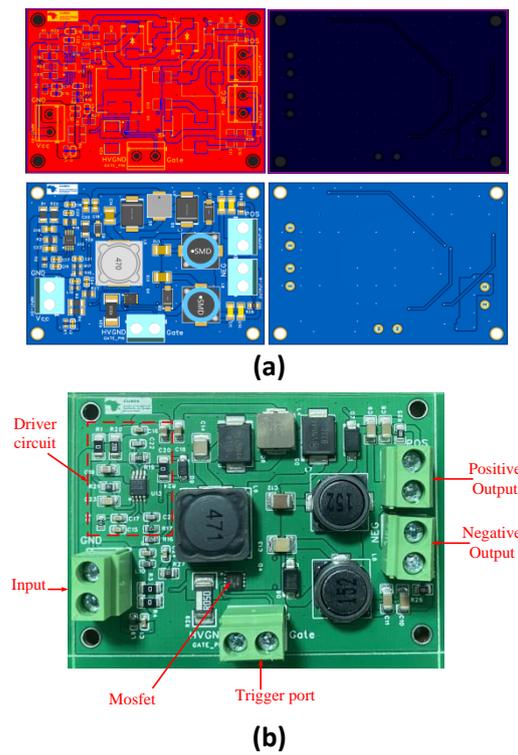


Figure 12. Proposed converter prototype: (a) Pcb design; (b) hardware.

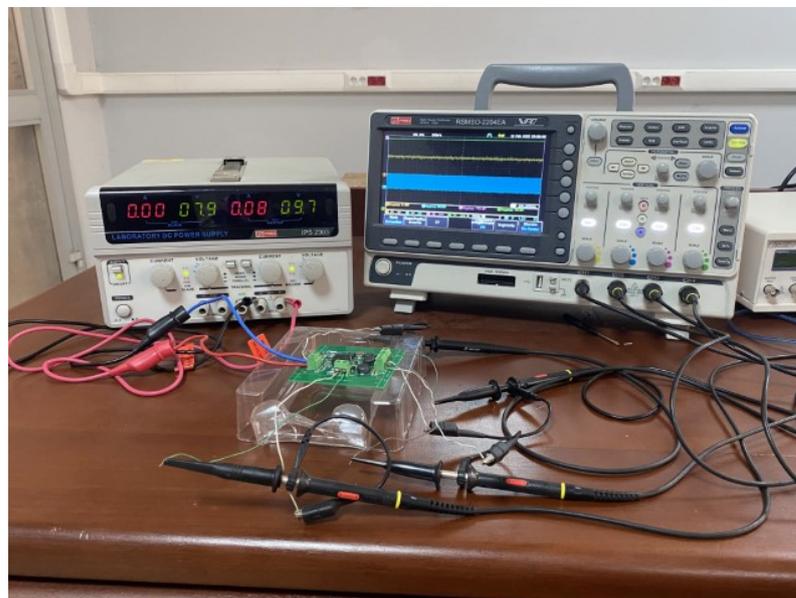


Figure 13. Experimental test setup of MSC.

Figure 14 shows the gate pulses and the positive output voltage waveforms V_0^+ for the proposed converter. It can be seen that a voltage gain of 14.796 is observed when the input is 5 V, at the switching frequency 251 kHz with the duty cycle of 72.06%. This experimental voltage gain is validated with the theoretical calculation and the converter is operated at CCM operation. Figure 15 shows the bipolar positive and negative output voltage waveforms V_0^+ and V_0^- . It is observed that the average value of the positive output voltage is 74.086 V, with a ripple voltage of 2.77%, and the average negative output voltage is -73.281 V, with a ripple voltage of 2.67%. The voltage symmetry with an equal load on both rails is 1.09%.

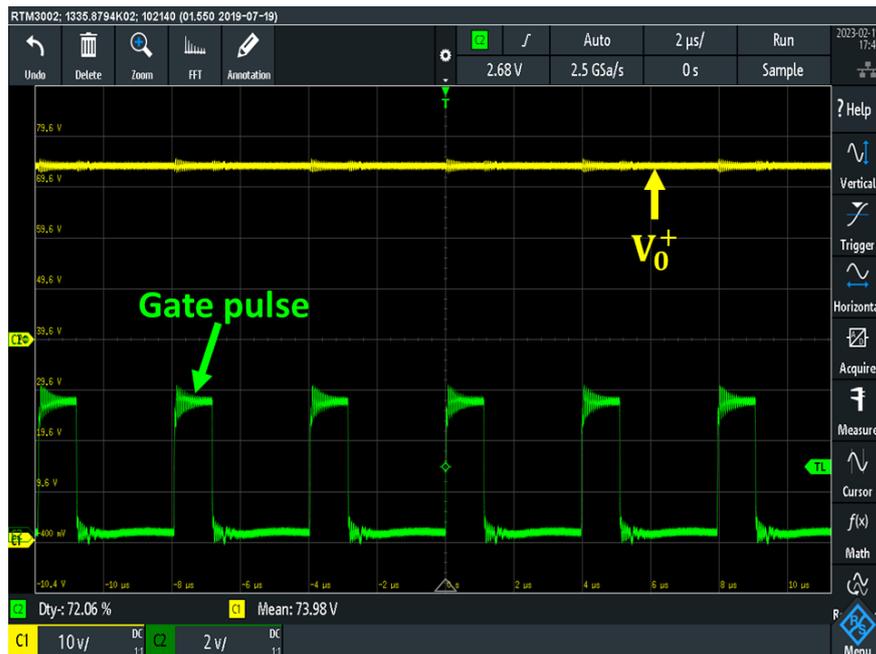


Figure 14. Experimental waveforms of the gate pulses voltage and positive output voltage of the proposed converter.

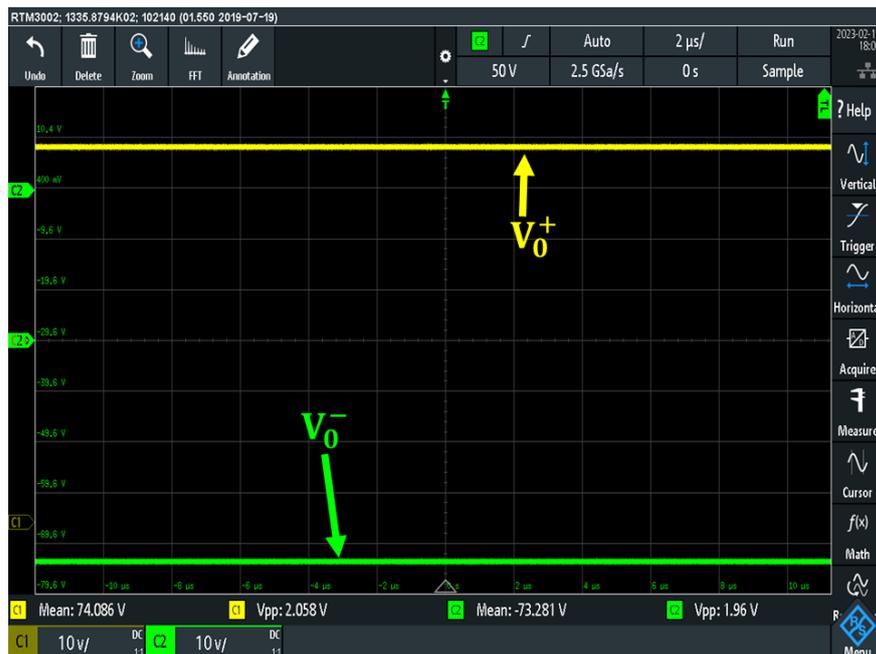


Figure 15. Experimental waveforms of the bipolar symmetrical output voltages of the proposed converter.

Figure 16 illustrates that the proposed converter can balance the bipolar output voltage under a sudden input voltage change. The waveforms of the positive and negative rails (V_0^+ and V_0^-) show that they maintain the same voltage value even when the input voltage changes from 5 V to 10 V.

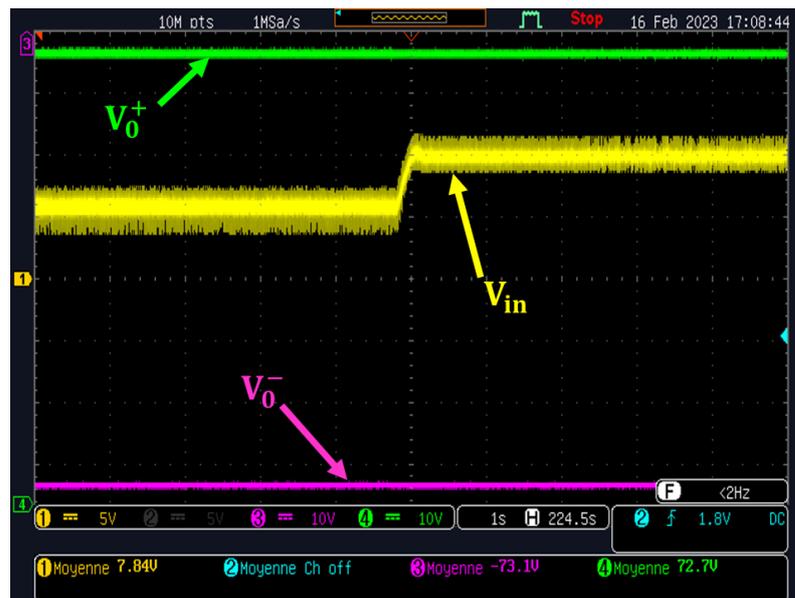


Figure 16. Experimental waveforms of the output voltages (V_0^+ and V_0^-) for the situation of a sudden change of input voltage V_{in} .

Despite being quite similar, the characteristics of the bipolar output voltages in the developed prototype are not as good as the simulation results. This is mainly due to parasitic elements introduced in the circuit design of the prototype.

6. Conclusions

In this study, a new structure of the nonisolated symmetrical bipolar DC–DC converter with high voltage gain was proposed. The proposed converter was analyzed based on the working principle of CCM and DCM. Considering the specifications and nonidealities of the converter components, we expressed the real efficiency and voltage gain as a function of load. The proposed DC–DC converter has the advantages of high voltage gain and wide duty cycle range, continuous input current, and was designed to maintain a reduced number of components by using only a single active switch. In addition, the assumptions, theoretical analysis, and design were validated by simulation and hardware implementation. The results are illustrated for 74 V output from 5 V input supply with a gain of 14.796. According to the obtained results, it can be concluded that the proposed converter is well suited to smart ultrasound scanner applications.

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References

1. Macovski, A. *Medical Imaging Systems*; Prentice Hall: Hoboken, NJ, USA, 1983.
2. Shung, K.K. *Diagnostic Ultrasound Imaging and Blood Flow Measurements*, 2nd ed.; CRC Press: Boca Raton, FL, USA, 2015.
3. Fontoura, B.D.; Epple, N.; Niederleithinger, E. A Portable Low-Cost Ultrasound Measurement Device for Concrete Monitoring. *Inventions* **2021**, *6*, 36. [[CrossRef](#)]

4. Daniels, J.M.; Hoppmann, R.A. *Practical Point-of-Care Medical Ultrasound*; Springer: Berlin/Heidelberg, Germany, 2016.
5. Choi, H.; Choe, S. Therapeutic Effect Enhancement by Dual-Bias High-Voltage Circuit of Transmit Amplifier for Immersion Ultrasound Transducer Applications. *Sensors* **2018**, *18*, 4210. [[CrossRef](#)] [[PubMed](#)]
6. Chan, V.; Perlas, A. Basics of Ultrasound Imaging. In *Atlas of Ultrasound-Guided Procedures in Interventional Pain Management*; Springer: Berlin/Heidelberg, Germany, 2011; pp. 13–19.
7. Grangé, G. Guide pratique de l'échographie obstétricale et gynécologique. *Rev. Med. Perinat.* **2013**, *5*, 69–70. [[CrossRef](#)]
8. I. Maxim Integrated Products. MAX14808/MAX14809 Octal Three- 21 Level/Quad Five-Level High-Voltage 2A Digital Pulsers with T/R Switch. Technical Report March 2013. Available online: <https://www.analog.com/media/en/technical-documentation/data-sheets/MAX14808-MAX14809.pdf> (accessed on 28 June 2023).
9. Xu, X.; Wala, S.A.; Vishwa, A.; Shen, J.; Dijeesh, K.; Devi, S.; Chandak, A.; Dixit, S.; Granata, E.; Pithadia, S.; et al. A Programmable Platform for Accelerating the Development of Smart Ultrasound Transducer Probe. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **2021**, *68*, 1296–1304. [[CrossRef](#)] [[PubMed](#)]
10. Hager, P.A.; Benini, L. LightProbe: A Digital Ultrasound Probe for Software-Defined Ultrafast Imaging. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **2019**, *66*, 747–760. [[CrossRef](#)]
11. Ahn, S.; Kang, J.; Kim, P.; Lee, G.; Jeong, E.; Jung, W.; Park, M.; Song, T. Smartphone-Based Portable Ultrasound Imaging System: Prototype Implementation and Evaluation. In Proceedings of the 2015 IEEE International Ultrasonics Symposium (IUS), Taipei, Taiwan, 21–24 October 2015; pp. 1–4.
12. Texas Instrument. *6-W Dual-Output SEPIC Converter Reference Design*; Test Report; Texas Instruments: Dallas, TX, USA, 2019.
13. Chen, M.; Feng, R.; Zhu, E. *Programmable \pm HV Power Supply with Low Static Power Consumption for Smart Probe*; Texas Instruments: Dallas, TX, USA, 2022.
14. Choi, H.; Yoon, C.; Yeom, J.-Y. A Wideband High-Voltage Power Amplifier Post-Linearizer for Medical Ultrasound Transducers. *Appl. Sci.* **2017**, *7*, 354. [[CrossRef](#)]
15. Rathod, V.T. A Review of Electric Impedance Matching Techniques for Piezoelectric Sensors, Actuators and Transducers. *Electronics* **2019**, *8*, 169. [[CrossRef](#)]
16. Navamani, J.D.; Vijayakumar, K.; Jegatheesan, R. Non-Isolated High Gain DC-DC Converter by Quadratic Boost Converter and Voltage Multiplier Cell. *Ain Shams Eng. J.* **2018**, *9*, 1397–1406. [[CrossRef](#)]
17. Sutikno, T.; Purnama, H.S.; Widodo, N.S.; Padmanaban, S.; Sahid, M.R. A review on non-isolated low-power DC-DC converter topologies with high output gain for solar photovoltaic system applications. *Clean Energy* **2022**, *6*, 557–572. [[CrossRef](#)]
18. Jotham, L.J.; Ooi, C.A.; Teh, J. Non-Isolated Conventional DC-DC Converter Comparison for a Photovoltaic System: A Review. *J. Renew. Sustain. Energy* **2020**, *12*, 013502. [[CrossRef](#)]
19. Pires, V.F.; Cordeiro, A.; Foito, D.; Silva, J.F.A. Dual Output and High Voltage Gain DC-DC Converter for PV and Fuel Cell Generators Connected to DC Bipolar Microgrids. *IEEE Access* **2021**, *9*, 157124–157133. [[CrossRef](#)]
20. Mumtaz, F.; Zaihar Yahaya, N.; Tanzim Meraj, S.; Singh, B.; Kannan, R.; Ibrahim, O. Review on Non-Isolated DC-DC Converters and Their Control Techniques for Renewable Energy Applications. *Ain Shams Eng. J.* **2021**, *12*, 3747–3763. [[CrossRef](#)]
21. Prabhakaran, P.; Agarwal, V. Novel Boost-SEPIC Type Interleaved DC-DC Converter for Mitigation of Voltage Imbalance in a Low-Voltage Bipolar DC Microgrid. *IEEE Trans. Ind. Electron.* **2020**, *67*, 6494–6504. [[CrossRef](#)]
22. Gopi, A.; Saravanakumar, R. High Step-up Isolated Efficient Single Switch DC-DC Converter for Renewable Energy Source. *Ain Shams Eng. J.* **2014**, *5*, 1115–1127. [[CrossRef](#)]
23. Affam, A.; Buswig, Y.M.; Othman, A.-K.B.H.; Julai, N.B.; Qays, O. A Review of Multiple Input DC-DC Converter Topologies Linked with Hybrid Electric Vehicles and Renewable Energy Systems. *Renew. Sustain. Energy Rev.* **2021**, *135*, 110186. [[CrossRef](#)]
24. Zhang, K.; Gao, G.; Zhao, C.; Wang, Y.; Wang, Y.; Li, J. Review of the Design of Power Ultrasonic Generator for Piezoelectric Transducer. *Ultrason. Sonochem.* **2023**, *96*, 106438. [[CrossRef](#)]
25. Jonveaux, L.; Schloh, C.; Meng, W.; Arija, J.; Rintoul, J. Review of Current Simple Ultrasound Hardware Considerations, Designs, and Processing Opportunities. *J. Open Hardw.* **2022**, *6*, 3. [[CrossRef](#)]
26. Boni, E.; Yu, A.C.H.; Freear, S.; Jensen, J.A.; Tortoli, P. Ultrasound Open Platforms for Next-Generation Imaging Technique Development. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **2018**, *65*, 1078–1092. [[CrossRef](#)]
27. Aljafari, B.; Devarajan, G.; Arumugam, S.; Vairavasundaram, I. Design and Implementation of Hybrid PV/Battery-Based Improved Single-Ended Primary-Inductor Converter-Fed Hybrid Electric Vehicle. *Int. Trans. Electr. Energy Syst.* **2022**, *2022*, 2934167. [[CrossRef](#)]
28. Shaik, R.K.; Dhanamjayulu, C. Synthesis and Implementation of a Multiport Dual Input-Dual Output Converter for Electric Vehicle Applications. *Int. Trans. Electr. Energy Syst.* **2022**, *2022*, 9279475. [[CrossRef](#)]
29. Annambhotla, L.T.S.; Parthiban, P. Non-Isolated Power Factor Corrected AC/DC Converter with High Step-Down Voltage Ratio for Low-Power Applications. *Int. Trans. Electr. Energy Syst.* **2022**, *2022*, 7142957. [[CrossRef](#)]
30. Nathan, K.; Ghosh, S.; Siwakoti, Y.; Long, T. A New DC-DC Converter for Photovoltaic Systems: Coupled-Inductors Combined Cuk-SEPIC Converter. *IEEE Trans. Energy Convers.* **2018**, *34*, 191–201. [[CrossRef](#)]
31. Pires, V.F.; Foito, D.; Silva, J.F. A Single Switch Hybrid DC/DC Converter with Extended Static Gain for Photovoltaic Applications. *Electr. Power Syst. Res.* **2017**, *146*, 228–235. [[CrossRef](#)]
32. Elsayad, N.; Moradisizkoochi, H.; Mohammed, O. A New Three-Level Flying-Capacitor Boost Converter with an Integrated LC2D Output Network for Fuel-Cell Vehicles: Analysis and Design. *Inventions* **2018**, *3*, 61. [[CrossRef](#)]

33. Moradisizkoochi, H.; Elsayad, N.; Mohammed, O. A Soft-Switched DC/DC Converter Using Integrated Dual Half-Bridge with High Voltage Gain and Low Voltage Stress for DC Microgrid Applications. *Inventions* **2018**, *3*, 63. [[CrossRef](#)]
34. Kurdkandi, N.V.; Nouri, T. Analysis of an efficient interleaved ultra-large gain DC–DC converter for DC microgrid applications. *IET Power Electron.* **2020**, *13*, 2008–2018. [[CrossRef](#)]
35. Azizkandi, M.E.; Sedaghati, F.; Shayeghi, H.; Blaabjerg, F. A High Voltage Gain DC–DC Converter Based on Three Winding Coupled Inductor and Voltage Multiplier Cell. *IEEE Trans. Power Electron.* **2020**, *35*, 4558–4567. [[CrossRef](#)]
36. Guo, Y.; Sun, H. A Bipolar Output Active-Switched-Inductor Converter for Bipolar DC Microgrid. *Int. J. Photoenergy* **2022**, *2022*, 72521633. [[CrossRef](#)]
37. Hasanpour, S.; Nouri, T. New Coupled-Inductor High-Gain DC/DC Converter with Bipolar Outputs. *IEEE Trans. Ind. Electron.* **2023**, *99*, 1–12. [[CrossRef](#)]
38. Allehyani, A. Analysis of a Symmetrical Multilevel DC-DC Boost Converter with Ripple Reduction Structure for Solar PV Systems. *Alex. Eng. J.* **2022**, *61*, 7055–7065. [[CrossRef](#)]
39. Nouhi, H.; Talavat, V.; Farhadi-Kangarlu, M. A Nonisolated Single-Switch Coupled Inductor-Based DC-DC Converter with High Voltage Gain for Renewable Power Generation Systems. *Int. Trans. Electr. Energy Syst.* **2023**, *2023*, e2600232. [[CrossRef](#)]
40. Pourjafar, S.; Shayeghi, H.; Hashemzadeh, S.M.; Sedaghati, F.; Maalandish, M. A Non-Isolated High Step-up DC–DC Converter Using Magnetic Coupling and Voltage Multiplier Circuit. *IET Power Electron.* **2021**, *14*, 1637–1655. [[CrossRef](#)]
41. Chen, Y.; Zhang, B. *Equivalent-Small-Parameter Analysis of DC/DC Switched-Mode Converter*; CPSS Power Electronics Series; Springer: Singapore, 2019; ISBN 9789811325731.
42. Elisa, G.; Abhishek, V.; Jun, S. *Designing Bipolar High Voltage SEPIC Supply for Ultrasound Smart Probe*; Application Note; Texas Instruments: Dallas, TX, USA, 2023.

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