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A Soft-Switched DC/DC Converter Using Integrated Dual Half-Bridge with High Voltage Gain and Low Voltage Stress for DC Microgrid Applications

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Abstract: In this paper, a soft-switched boost converter including an integrated dual half-bridge circuit with high voltage gain and continuous input current is introduced that can be suitable for the applications requiring a wide voltage gain range, such as for the front-end of the inverter in a DC microgrid to integrate renewable energy sources (RES). In the proposed converter, two half-bridge converters are connected in series at the output stage to enhance the voltage gain. Additionally, the balanced voltage multiplier stage is employed at the output to increase the voltage conversion ratio, as well as distribute the voltage stress across semiconductors; hence, switches with smaller on-resistance $R_{DS(on)}$ can be adopted resulting in an improvement in the efficiency. The converter takes advantage of the clamp circuit not only to confine the voltage stress of switches, but also to achieve the soft-switching, which leads to a reduction in the switching loss as well as the cost. The mentioned features make the proposed converter a proper choice for interfacing RES to the DC-link bus of the inverter. The operation modes, steady-state analysis, and design consideration of the proposed topology have been demonstrated in the paper. A 1-kW laboratory prototype was built using gallium nitride (GaN) transistors and silicon carbide (SiC) diodes to confirm the effectiveness of the proposed topology.

Keywords: high step-up converter; micro grid; photovoltaic; soft switching; wide-bandgap devices

1. Introduction

Recent clean energy technologies, such as photovoltaic (PV), fuel cell, and wind, are attracting a global attraction due to the environmental issue and scarcity of fossil fuels. RES can generate electricity with minimum atmospheric pollution and carbon emission. Traditionally, the distribution system was centralized transmission grid system due to the distance between the generation and demand location. On the other hand, with the development of RES, microgrids support the grid by decentralized generation [1–4]. The general layout of a hybrid microgrid including a high step-up DC/DC converter is demonstrated in Figure 1. Since PV modules can generate the low-level voltage, it needs a DC-DC converter with a high voltage gain to solve the issue resulting from the mismatch in the voltage level of PV and the DC-bus. In other words, this converter must boost the voltage of PV (15–30 V) to the essential level demanded by the DC-bus (around 400 V). In addition to a high voltage conversion ratio, the converter should provide the power conversion with high efficiency as well as high power density and low input current ripple [5–9].

Even though the conventional boost converter is the most straightforward approach, it suffers from a high voltage stress of semiconductors and hard-switching, which leads to low efficiency. Moreover, the voltage gain keeps reducing with the rise of the load current [10,11]. Different techniques

for increasing the voltage gain have been presented, such as employing a switched-capacitor circuit, switched-inductor circuit, voltage lift, and so on, and each one has its own advantages and disadvantages depending on the applications and design criteria. High component count, a complex control circuit, high cost, and high weight are some of the drawbacks of these topologies compared to the conventional boost converter [12–17].

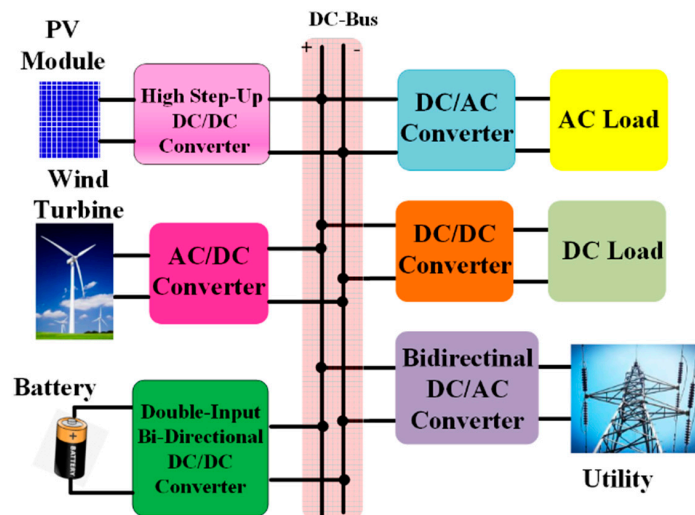


Figure 1. General layout of a hybrid microgrid system.

A promising approach for increasing the voltage gain that relies on high-frequency coupled magnetics employs the transformer or coupled inductor. The transformer provides another freedom except for the duty cycle of the switch to increase the voltage gain, offering a high boosting factor in accordance with its turns-ratio [18,19]. A family of DC/DC converters with high voltage gain has been introduced in [20], which employs the passive clamp circuit to improve the efficiency by recycling the leakage energy of coupled inductors. The reverse recovery problem of diodes is another critical issue that was addressed by this family of converters; therefore, their losses can be diminished. In [21], a high step-up converter employing a coupled inductor has been presented, which can greatly decrease the voltage rating of semiconductors by a cancellation of resonance between the parasitic capacitance of semiconductors and the leakage inductance of the coupled inductor. The main drawback of these topologies is the high voltage spikes across the main switches because of the leakage inductance of the magnetic component. Multilevel architectures gained a great deal of interest, especially in the past decade, as they distribute the voltage stress across the semiconductor devices, which helps use the semiconductor devices with low-rated voltage; hence, they can improve the system efficiency [22]. However, the complex control algorithm impedes employing them in industrial applications.

A crucial characteristic that impacts on the lifetime of RES-based power systems is the current ripple of the source, which has been investigated by many studies [23–26]. The current-fed converter using built-in transformer is an effective method for high-power and high-voltage applications, which can smooth the input current and reduce the loss. High step-up converters with switched-coupled-inductors have been introduced in [27] that benefit from shared current stress. However, there is a considerable ripple in the current drawn from the input source, causing the lifespan of systems to be shortened. Paralleled input configuration using coupled inductors have attracted considerable attention lately due to their ability to effectively reduce the input current ripple and enhance the power level by sharing the input current equally among different branches [28–30]. Accordingly, the size of magnetic components and the current stress of semiconductor devices can be decreased. However, the structure of the coupled inductor is very complicated; therefore, they are not the ultimate choice for high-power industrial applications.

Half-bridge converter has demonstrated widespread applications for use in high step-up DC/DC converters especially for PV-based microgrid applications owing to its merits, such as simplicity, ease of control, soft-switching operation in terms of zero voltage switching (ZVS) of switches and zero current switching (ZCS) of diodes, and small input filter because of the continuous input current [29–31]. Depending on the input voltage and output power, however, the soft-switching performance cannot be achieved for a wide voltage and power range. Moreover, still the voltage gain is not high enough to minimize the value of the turns ratio, so a high value of the turns ratio is required to achieve the desired range of voltage gain.

In this paper, a soft-switched high step-up DC/DC converter with an integrated dual half-bridge topology is proposed as the front-end of the inverter for DC microgrid applications. The converter offers substantial voltage gain by a series connection of secondary windings of transformers. Additionally, a voltage multiplier stage (VMS) is employed at the output stage to amplify the voltage gain, as well as to reduce the voltage stress across the semiconductors evenly. Furthermore, the VMS directly transfers the leakage energy of transformers to the output capacitors. In the proposed converter, the active-clamp circuit not only restricts the voltage stress of switches but paves the way for soft-switching performance leading to higher efficiency. As a result, switches with lower rated-voltage and smaller on-resistance $R_{DS(on)}$ can be utilized because the voltage stress of switches is much lower than the output voltage; thus, the conduction loss will reduce. Concerning the control technique, the converter takes the advantage of asymmetrical pulse width modulation in terms of simplicity of the control circuit.

This paper is divided into six sections, and organized as follows: the second section discusses the schematic and the operating principles, and detailed theoretical analysis of the proposed converter. Additionally, a comparison is carried out in this section by evaluating the principal characteristics of state-of-the-art high step-up converters. Section 3 demonstrates the design considerations. Section 4 provides the simulation and experimental results and, finally, a conclusion is drawn in Section 5.

2. Structure and Operating Principles of the Proposed Converter

2.1. General Structure

The proposed converter is shown in Figure 2a, which consists of conventional boost converter with active-clamp circuit to provide an input current with low ripple as well as soft-switching performance, and the balanced VMS to increase the voltage conversion ratio. The equivalent circuit of proposed converter is depicted in Figure 2b, in which V_{in} denotes the PV source; V_o denotes the output voltage; L_B denotes the boost inductor; C_r denotes the DC-blocking capacitor; C_{o1} – C_{o4} denote the output capacitors; C_{m1} and C_{m2} denote the switched capacitor; S_M and S_C denote the main and clamp switch, respectively; D_{o1} – D_{o4} denote the output diodes; and R_o denotes the load resistance. It is noteworthy to mention that a magnetizing inductor (L_m), a leakage inductor (L_k), and an ideal transformer with a turns ratio of $n = N_2/N_1$ are used to model the transformers. In Figure 2b, L_{k1} and L_{m1} denotes the leakage inductor and the magnetizing inductor of transformer T_1 ; L_{k2} and L_{m2} denotes the leakage inductor and the magnetizing inductor of transformer T_2 .

2.2. Operation Modes

There are six operation modes in the proposed converter during one switching period, as illustrated in Figure 3. The key waveforms during one switching period are shown in Figure 4. To analysis the operation in the steady-state and derive the operational parameters of proposed converter, following assumptions are made:

- (1) The inductor L_k shows the total inductance of leakage inductors L_{k1} and L_{k2} .
- (2) all passive and active semiconductors are considered ideal; and
- (3) the capacitors are large enough to assume that their voltage is constant during one switching period.

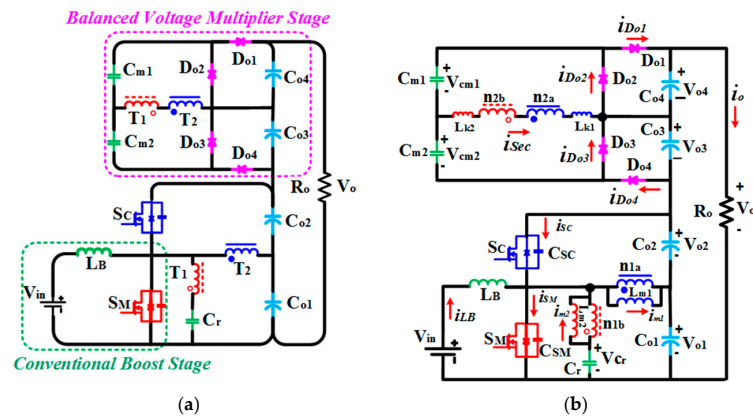


Figure 2. The schematic of the proposed converter: (a) proposed converter; and (b) the equivalent circuit.

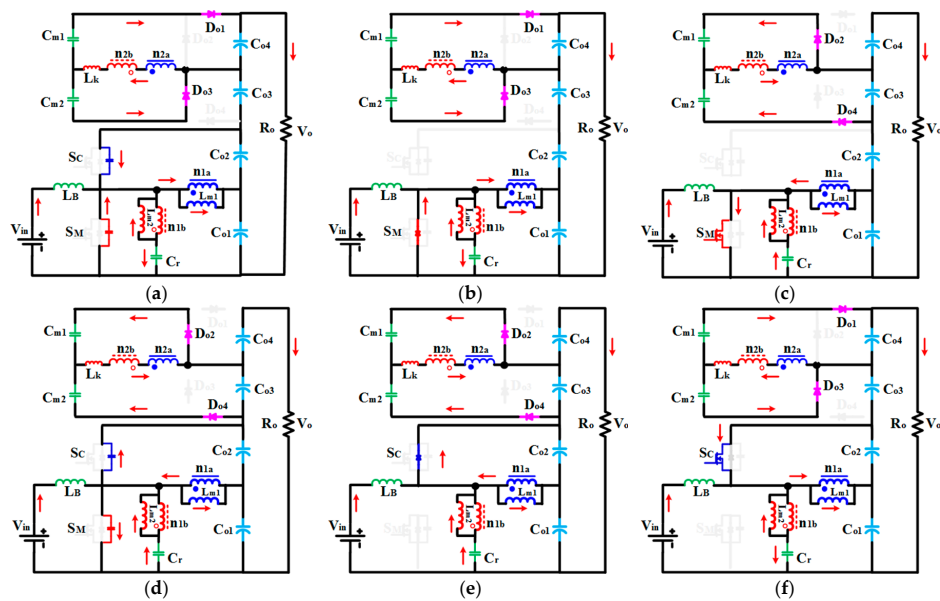


Figure 3. Operation modes: (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4; (e) Mode 5; and (f) Mode 6.

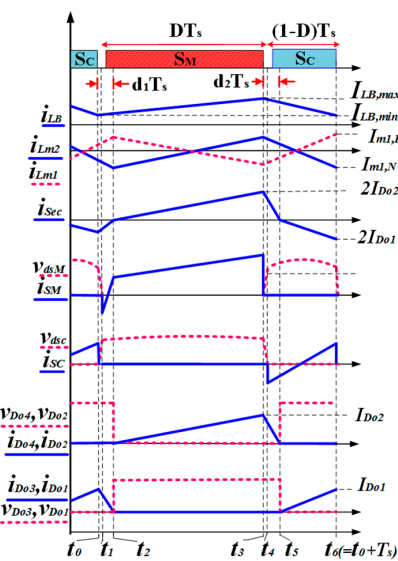


Figure 4. Key waveforms of the proposed converter.

2.2.1. Mode 1 [t_0 – t_1]

Before t_0 , the clamp switch was conducting the current. At t_0 , the gate pulse of S_C is removed, as shown in Figure 4. As depicted in Figure 3a, during this state, the parasitic capacitors of switches S_M and S_C are being discharged and charged, respectively. Due to the parasitic capacitor, the voltage stress of clamp switch increases linearly, which is expressed by:

$$V_{SM} \cong \frac{i_{LB}(t_0) - 2ni_{Lk}(t_0) - i_{Lm1}(t_0) + i_{Lm2}(t_0)}{C_{SM} + C_{SC}}(t - t_0) \quad (1)$$

The duration of this mode can be determined by:

$$\Delta t_{01} = \frac{(C_{SM} + C_{SC})(V_{o1}(t_0) + V_{o2}(t_0))}{i_{LB}(t_0) - 2ni_{Lk}(t_0) - i_{Lm1}(t_0) + i_{Lm2}(t_0)} \quad (2)$$

2.2.2. Mode 2 [t_1 – t_2]

This mode starts when the voltage of main switch V_{SM} becomes zero and, hence, its antiparallel diode starts conducting the current. Thus, the ZVS performance of main switch at turn-on instant is ensured. During this mode in Figure 3b, the voltage stress of clamp switch is restricted to the total voltage of capacitors C_{o1} and C_{o2} without spikes problem. At the output stage, the output diodes D_{o2} and D_{o4} are cut off, and diodes D_{o1} and D_{o3} are conducting the current, expressed as:

$$i_{D_{o1}}(t) = i_{D_{o3}}(t) = 0.5i_{Lk}(t) = 0.5i_{Lk}(t_0) + \frac{nV_{Cr}(t_0) + nV_{o1}(t_0) + V_{o4}(t_0) - V_{cm1}(t_0)}{2L_k}(t - t_0) \quad (3)$$

During this mode, the boost inductor stores the energy of the input source, i.e., PV source, and the input current increases which can be determined by:

$$i_{LB}(t) = i_{LB}(t_1) + \frac{V_{in}}{L_B}(t - t_1) \quad (4)$$

The current of magnetizing inductors can be defined by:

$$i_{Lm1}(t) = i_{Lm1}(t_1) - \frac{V_{o1}(t_1)}{L_{m1}}(t - t_1) \quad (5)$$

$$i_{Lm2}(t) = i_{Lm2}(t_1) + \frac{V_{Cr}(t_1)}{L_{m2}}(t - t_1) \quad (6)$$

2.2.3. Mode 3 [t_2 – t_3]

This mode starts at t_2 when the leakage inductors current becomes zero; so, the diodes D_{o2} and D_{o4} turn on, as shown in Figure 3c. Therefore, ZCS at turn-on instant is achieved for these diodes, alleviating their losses. In the meantime, the transformers transfer the energy of input source and output capacitor C_{o1} to the switched capacitor C_{m1} and output capacitor C_{o3} . The secondary windings of transformer are connected in a way that the total voltage of the output stage increases. The current of leakage inductance and output diodes, and main switch can be expressed by:

$$i_{D_{o2}}(t) = i_{D_{o4}}(t) = 0.5i_{Lk}(t) = 0.5i_{Lk}(t_2) + \frac{nV_{Cr}(t_2) + nV_{o1}(t_2) - V_{cm1}(t_2)}{2L_k}(t - t_2) \quad (7)$$

$$i_{SM}(t) = i_{in}(t) + 2ni_{Lk}(t) + i_{Lm2}(t) - i_{Lm1}(t) \quad (8)$$

2.2.4. Mode 4 [t_3 – t_4]

At t_3 , the gate pulse of clamp switch is removed, and the output capacitors of switches S_M and S_C are being charged and discharged, respectively. Due to the parasitic capacitor, the voltage stress of main switch increases linearly. The circuit condition at the VMS is the same as in Mode 3. The following equations define the voltage stress of main switch and the duration of this mode as:

$$V_{SC} \cong \frac{i_{LB}(t_3) + 2ni_{Lk}(3) - i_{Lm1}(t_3) + i_{Lm2}(t_3)}{C_{SM} + C_{SC}}(t - t_3) \quad (9)$$

$$\Delta t_{34} = \frac{(C_{SM} + C_{SC})(V_{o1}(t_3) + V_{o2}(t_3))}{i_{LB}(t_3) + 2ni_{Lk}(t_3) - i_{Lm1}(t_3) + i_{Lm2}(t_3)} \quad (10)$$

2.2.5. Mode 5 [t_4 – t_5]

As shown in Figure 4, at the beginning of this mode, the voltage across clamp switch V_{SC} becomes zero; thus, the current flows through the antiparallel diode of clamp switch. Accordingly, the ZVS implementation of clamp switch at turn-on instant is guaranteed. During this mode, the voltage stress of main switch is effectively confined to the total voltage of capacitors C_{o1} and C_{o2} without ringing and spikes issue, shown in Figure 3e. In the meantime, the boost inductor is transferring the PV-source energy to the output capacitor C_{o1} and C_{o2} . At the output stage, the output diodes D_{o2} and D_{o4} are conducting the current. The following equations can be written for this operation mode:

$$i_{D_{o2}}(t) = i_{D_{o4}}(t) = 0.5i_{Lk}(t) = 0.5i_{Lk}(t_4) + \frac{nV_{Cr}(t_4) - nV_{o1}(t_4) - 2nV_{o2}(t_4) - V_{cm1}(t_4)}{2L_k}(t - t_4) \quad (11)$$

$$i_{LB}(t) = i_{LB}(t_4) + \frac{V_{in} - V_{o1} - V_{o2}}{L_B}(t - t_4) \quad (12)$$

$$i_{Lm1}(t) = i_{Lm1}(t_4) + \frac{V_{o2}(t_4)}{L_{m1}}(t - t_4) \quad (13)$$

$$i_{Lm2}(t) = i_{Lm2}(t_4) + \frac{V_{Cr}(t_4) - V_{o1}(t_4) - V_{o2}(t_4)}{L_{m2}}(t - t_4) \quad (14)$$

2.2.6. Mode 6 [t_5 – t_6]

At the beginning of this mode, the direction of inductor current changes; thus, the diodes D_{o2} and D_{o4} are cut off and diodes D_{o1} and D_{o3} turn on, as shown in Figure 3f. Therefore, ZCS at turn-on instant is enabled for diodes D_{o1} and D_{o3} , which helps alleviate turn-on losses. In the meantime, the energy stored in the switched-capacitor C_{m1} is being released to the output capacitor C_{o4} . On the other hand, the switched-capacitor C_{m2} is storing the energy transferred by transformers from the input stage. The current of leakage inductance and output diodes, and clamp switch can be expressed by:

$$\begin{aligned} i_{D_{o1}}(t) = i_{D_{o3}}(t) &= 0.5i_{Lk}(t) \\ &= 0.5i_{Lk}(t_5) \\ &\quad + \frac{nV_{Cr}(t_5) - nV_{o1}(t_5) - 2nV_{o2}(t_5) + V_{o4}(t_5) - V_{cm1}(t_5)}{2L_k}(t - t_5) \end{aligned} \quad (15)$$

$$i_{SC}(t) = i_{in}(t) + 2ni_{Lk}(t) + i_{Lm2}(t) - i_{Lm1}(t) \quad (16)$$

At the end of this operation mode the gate pulse of clamp switch will be removed, and the converter begins a new switching period.

2.3. Voltage Gain

To derive the operational parameters of proposed converter, it is assumed that as compared with the leakage inductors, the magnetizing inductors are so large that their effect can be neglected.

By applying the voltage-second balance to the inductor L_B and the primary winding of transformers T_2 , the output voltage V_{o1} and V_{o2} can be expressed as:

$$V_{o1} + V_{o2} = \frac{V_{in}}{1-D} \quad (17)$$

$$V_{o1} = V_{in} \quad (18)$$

$$V_{o2} = \frac{DV_{in}}{1-D} \quad (19)$$

The duty cycle of the main switch is denoted as $D = T_{on}/T_s$, where T_{on} represents the conduction time of main switch in each switching period and T_s represents the switching period. Considering Figure 3, the voltage of DC-blocking capacitor can be derived by applying the voltage-second balance to the primary windings of transformers T_1 as follows:

$$V_{Cr} = V_{in} \quad (20)$$

From Equations (3) and (15), the diode D_{o1} peak current, I_{Do1} , can be written as follows:

$$I_{Do1} = \frac{2nV_{in} + V_{o4} - V_{cm1}}{2L_k} d_1 T_s = \frac{\frac{2nDV_{in}}{1-D} - V_{o4} + V_{cm1}}{2L_k} (1-D-d_2) T_s \quad (21)$$

From Equations (7) and (11), the diode D_{o2} peak current, I_{Do2} , can be achieved from:

$$I_{Do2} = \frac{2nV_{in} - V_{cm1}}{2L_k} (D-d_1) T_s = \frac{\frac{2nDV_{in}}{1-D} + V_{cm1}}{2L_k} d_2 T_s \quad (22)$$

From Equations (21) and (22), the output voltage V_{o4} and the voltage of switched capacitor C_{m1} can be obtained by:

$$V_{cm1} = 2nV_{in} \frac{(D-d_1)(1-D) - Dd_2}{(1-D)(D-d_1+d_2)} \quad (23)$$

$$V_{o4} = 2nV_{in} \left[\frac{(D-d_1)(1-D) - Dd_2}{(1-D)(D-d_1+d_2)} + \frac{D(1-D-d_2) - (1-D)d_1}{(1-D)(1-D+d_1-d_2)} \right] \quad (24)$$

Since the average capacitor current must be zero at steady-state, the output diode currents I_{Do1} and I_{Do2} can be expressed as:

$$I_o = \int_0^{T_s} i_{Do1}(t) dt = \int_0^{T_s} i_{Do2}(t) dt \quad (25)$$

From Equation (25) and Figure 4, the output current can be determined by:

$$I_o = \frac{(D-d_1+d_2)}{2} I_{Do2} = \frac{(1-D+d_1-d_2)}{2} I_{Do1} \quad (26)$$

From Equations (23), (24), and (26), the parameters d_1 and d_2 , which are shown in Figure 4 can be demonstrated in the form of:

$$d_1 = kD \quad (27)$$

$$d_2 = k(1-D) \quad (28)$$

$$k = 0.5 \left(1 - \sqrt{1 - \frac{8L_k I_o f_s}{nDV_{in}}} \right) \quad (29)$$

Since the VMS operates symmetrically, the voltage stress of capacitors C_{o3} and C_{o4} is identical; so, the voltage gain, $M = V_{out}/V_{in}$, can be defined as follows:

$$M = \frac{V_o}{V_{in}} = \frac{V_{o1} + V_{o2} + V_{o3} + V_{o4}}{V_{in}} = \frac{1}{1-D} + \frac{4n(1-2k)D}{(D-2Dk+k)(1-D+2Dk-k)} \quad (30)$$

When ignoring the variable k in Equation (30) due to the small order of value of leakage inductance, the ideal voltage gain will be:

$$M = \frac{V_o}{V_{in}} = \frac{4n+1}{1-D} \quad (31)$$

Figure 5 shows the voltage gain characteristic of proposed converter versus different duty cycle (D) and turns-ratio (n) for different values of variable k . The converter ensures high voltage gain with a small turns ratio even with a low duty cycle and, thus, the voltage stress as well as the switching loss can be reduced.

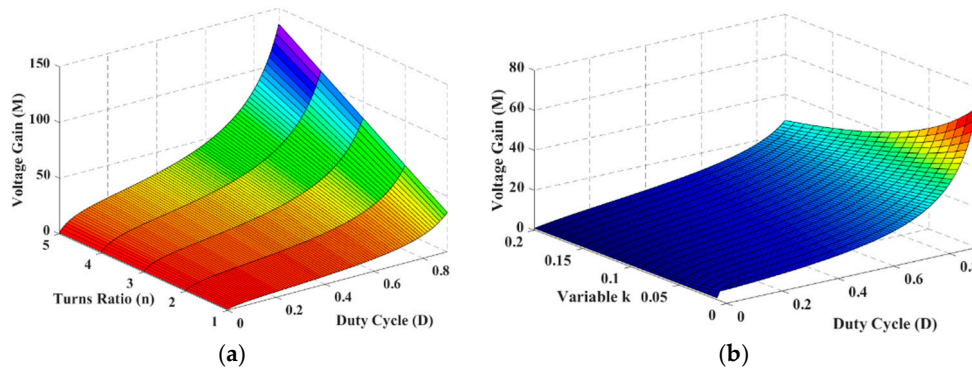


Figure 5. Voltage gain characteristics: (a) voltage gain versus different duty cycle and turns-ratio when $k = 0.06$; and (b) voltage gain versus different duty cycle and variable k when $n = 1.5$.

2.4. Voltage Stress Across Switches and Diodes

From the operation principle of proposed converter, the voltage stress of switches is effectively restricted to the voltage across output capacitors C_{o1} and C_{o2} without ringing and spikes issue due to adopting active-clamp configuration. Thus, the voltage stress of switches can be expressed by:

$$V_{SM,max} = V_{SC,max} = V_{o1} + V_{o2} = \frac{V_{in}}{1-D} = \frac{V_o}{4n+1} \quad (32)$$

Due to the balanced operation of VMS, the voltage stress of all diodes is identical and can be achieved by:

$$V_{Do1} = V_{Do2} = V_{Do3} = V_{Do4} = \frac{2nV_o}{4n+1} \quad (33)$$

From Equation (33), it can be concluded that the switches and diodes withstand much lower voltage stress than the output voltage resulting in switches with smaller on-resistance $R_{DS(on)}$ can be used; hence, the efficiency can be improved. Moreover, when turns-ratio keeps increasing the voltage stress of switches and diodes reduces.

2.5. The Magnetizing Inductor Minimum and Maximum Currents i_{m1} and i_{m2}

From Equations (5), (6), (13), and (14), the relation between maximum and minimum magnetizing current for transformers T_1 and T_2 can be written as follows:

$$I_{m1,P} - I_{m1,N} = I_{m2,P} - I_{m2,N} = \frac{V_{in}DT_s}{2L_{m1}} \quad (34)$$

From Figure 2, along with the ampere-second balance for capacitors, it can be concluded that the average value of the current of magnetizing inductors is zero. Thus, the magnetizing inductor maximum and minimum current can be achieved from:

$$I_{m1,P} = I_{m1,N} = I_{m2,P} = I_{m2,N} = \frac{V_{in}DT_s}{2L_{m1}} \quad (35)$$

2.6. ZVS Soft-Switching Conditions for Switches S_M and S_C

As illustrated in “Operation Modes” section, the soft-switching performance can be achieved for both switches as an inherent advantage of proposed topology leading to less switching loss in the active semiconductors. The ZVS performance is guaranteed for switch S_C if its gate-pulse is applied when the anti-parallel diode is conducting the current during mode 5. In other words, the following condition should be satisfied:

$$0.5L_B I_{SC,ZVS}^2 \geq 0.5(C_{SM} + C_{SC})\left(\frac{V_{in}}{1-D}\right)^2 \quad (36)$$

where the ZVS current $I_{SC,ZVS}$ is defined by:

$$I_{SC,ZVS} = I_{LB,max} + 2I_{m1,P} + \frac{8nI_o}{D} = \frac{2L_BP_o + DT_sV_{in}^2}{2V_{in}L_B} + \frac{V_{in}DT_s}{L_{m1}} + \frac{8nP_o}{DV_o} \quad (37)$$

To ensure the ZVS performance at turn-on instant for main switch S_M , the energy difference between the energy stored in the leakage inductor L_k and magnetizing inductor L_m should be larger than the energy stored in the parasitic capacitors of S_M and S_C . This condition can be written as follows:

$$0.5L_B I_{SM,ZVS}^2 \geq 0.5(C_{SM} + C_{SC})\left(\frac{V_{in}}{1-D}\right)^2 \quad (38)$$

The ZVS current of main switch $I_{SM,ZVS}$ is defined by:

$$I_{SM,ZVS} = I_{LB,min} - 2I_{m1,P} - \frac{8nI_o}{1-D} = \frac{2L_BP_o - DT_sV_{in}^2}{2V_{in}L_B} - \frac{V_{in}DT_s}{L_{m1}} + \frac{8nP_o}{(1-D)V_o} \quad (39)$$

The relationship between the ZVS current versus the input voltage and output power for both switches S_M and S_C are plotted in Figure 6a,b, respectively. It can be seen that the soft-switching can be achieved for both switches for a wide range of input voltage and output power, improving the efficiency of power conversion system.

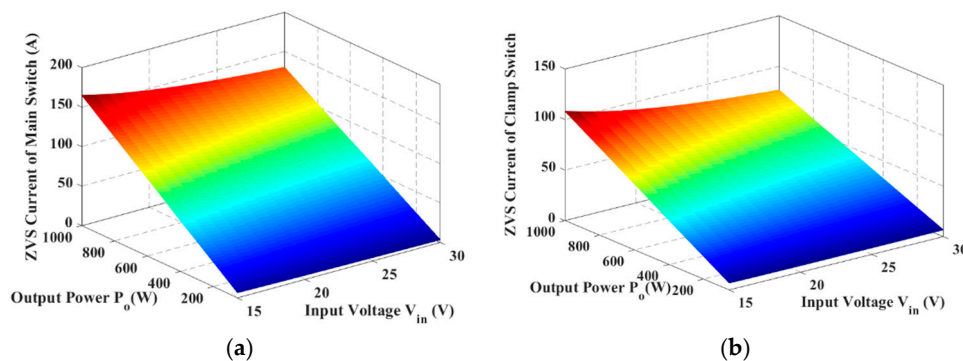


Figure 6. Soft-switching characteristics of the proposed converter. (a) ZVS current of the main switch; and (b) ZVS current of the clamp switch.

2.7. Current Stress of Power Switches and Diodes

From Figure 2 and Equation (8), the maximum current of main switch can be derived by:

$$I_{SM,max} = I_{LB,max} + 2I_{m1,P} + \frac{8nI_o}{D} = \frac{2L_BP_o + DT_sV_{in}^2}{2V_{in}L_B} + \frac{V_{in}DT_s}{L_{m1}} + \frac{8nP_o}{DV_o} \quad (40)$$

Similarly, the maximum current of clamp switch can be derived from Equation (16), determined by:

$$I_{SC,max} = I_{LB,min} - 2I_{m1,P} + \frac{8nI_o}{(1-D)} = \frac{2L_BP_o - DT_sV_{in}^2}{2V_{in}L_B} - \frac{V_{in}DT_s}{L_{m1}} + \frac{8nP_o}{(1-D)V_o} \quad (41)$$

The maximum current and average current of output diodes can be estimated by ignoring the effect of leakage inductance, which is given as follows:

$$I_{Do1,max} = I_{Do3,max} = \frac{2I_o}{1-D} \quad (42)$$

$$I_{Do2,max} = I_{Do4,max} = \frac{2I_o}{D} \quad (43)$$

$$I_{Do1,avg} = I_{Do2,avg} = I_{Do3,avg} = I_{Do4,avg} = I_o \quad (44)$$

2.8. Comparison with Other High Step-Up Converters

To have a better insight into the performance superiority of proposed topology, a comparison is carried out regarding the functional characteristics, including the voltage gain, voltage stress of switches and diodes, number of passive and active components, soft-switching performance, and complexity of control circuit. Table 1 compares the proposed converter with the state-of-the-art high step-up DC/DC converters. It can be seen that the proposed converter offers the much higher voltage gain, as well as lowest voltage stress of semiconductors. Thus, the losses and price for implementing a prototype will be lower. Regarding the soft-switching, even though the converters cited in [26] and [28] have the soft-switching characteristic, the proposed converter can provide ZVS conditions for both switches with minimum number of switches, resulting in efficiency improvement. Furthermore, compared to other converters, the control technique and gate-driver circuit are simple for proposed converter due to the asymmetrical PWM control scheme. Figure 7 shows the voltage gain and voltage stress of switches and diodes for proposed converter in comparison to that of other converters. The relation between the voltage gain and duty cycle (D), as shown in Figure 7a, indicates that the proposed converter boosts the input voltage with lower operating duty cycle. Therefore, the voltage stress of the switches and the losses will be lower. Figure 7b,c demonstrates the voltage stress of switches and diodes for different values of turns ratio (n), respectively. To sum up, the proposed topology outperforms its counterparts regarding the vital specifications of a high step-up converter.

Table 1. Performance comparison among proposed converter and other converters.

Item	Converter Cited in [26]	Converter Cited in [27]	Converter Cited in [28]	Converter Cited in [29]	Proposed Converter
Voltage gain	$\frac{2n+2}{1-D}$	$\frac{D(2n+1)+1}{1-D}$	$\frac{2n+2}{1-D}$	$\frac{2n+4}{1-D}$	$\frac{4n+1}{1-D}$
Switch voltage stress	$\frac{V_o}{2n+2}$	$\frac{V_o}{D(2n+1)+1}$	$\frac{V_o}{2n+2}$	$\frac{V_o}{2n+4}$	$\frac{V_o}{4n+1}$
Diode voltage stress	V_o	$\frac{2nV_o}{D(2n+1)+1}$	V_o	$\frac{nV_o}{n+2}$	$\frac{2nV_o}{4n+1}$
No. of Components	S ¹	4	2	4	2
	D ²	2	3	4	4
	C ³	4	3	5	7
	L ⁴	0	0	2	1
No. of Transformer or coupled inductors	2	2	1	2	2
Soft-switching	Soft switching (ZVS)	Hard switching	Soft switching (ZVS)	Hard switching	Soft switching (ZVS)
Control circuit	Complex	Simple	Complex	Simple	Simple

¹ Switch; ² Diode; ³ Capacitor; ⁴ Inductor.

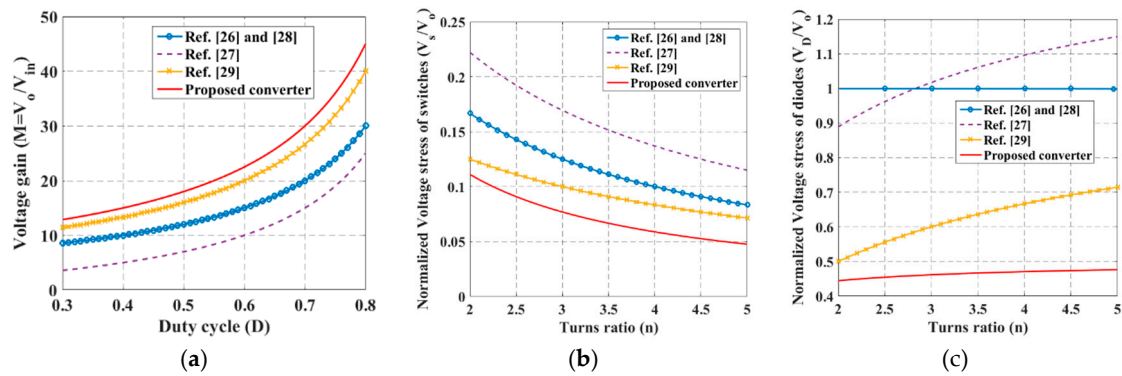


Figure 7. Comparison between the proposed converter and other step-up converters. (a) Voltage gain versus duty cycle (D) when $n = 2$; (b) voltage stress of switches versus turns ratio (n); and (c) voltage stress of diodes versus turns ratio (n).

2.9. Loss Analysis of Proposed Converter

The losses in the proposed converter can be divided into five major contributors, namely: conduction and switching losses of the switches, losses of the diodes, losses of the transformers, and losses of the inductor.

2.9.1. Conduction Loss of Switches

The conduction loss of switches can be calculated by:

$$P_{Cond,S} = R_{DS(on)} I_{rms,s}^2 \quad (45)$$

where $I_{rms,s}$ denotes the root mean square (RMS) current of the switch, and $R_{DS(on)}$ denotes the on-resistance of the switch.

2.9.2. Switching Loss of Transistors

In the implemented converter, GaN E-HEMTs switches are employed. As an advantage of GaN switches, they do not have a body diode, as well as the reverse recover charge, the loss caused by the reverse recovery charge of the body diode can be neglected. Other contributors to the switching loss in a GaN switches can be listed as follows: (1) the overlap of current and voltage during turn-on and turn-off; (2) gate charge loss; and (3) the loss caused by the parasitic capacitance of switch. The total switching loss of the switches of the proposed converter can be achieved from:

$$P_{Sw,S} = \left[0.5 V_s I_s (t_r + t_f) + 0.5 C_{oss} V_s^2 + Q_T V_G \right] f_s \quad (46)$$

where f_s is the switching frequency, t_r , and t_f are the rise and fall times of the transistor, Q_T is the gate charge, V_s the voltage stress of switch, and V_G is the gate driver voltage.

2.9.3. Diode Losses

The switching and capacitive charge (Q_C) losses of the SiC diodes can be estimated by:

$$P_{Di} = Q_C V_D f_s + V_{fi} I_{D,rms} \quad (47)$$

where V_{fd} , and V_D are the forward voltage and the voltage stress of the diode, respectively. It is noteworthy to mention that the reverse recovery switching loss of the SiC diodes can be ignored.

2.9.4. Inductor Losses

The losses of inductors include two main factors, the copper loss and the core loss. The conduction loss, P_{L_cond} , is caused by the DC current component flowing in the inductors' windings, while the core loss, P_{L_core} , is caused by the inductors' ripple currents, which is given in datasheet. The losses of inductor can be expressed as:

$$P_{Cond,L} = R_{L,ESR} I_{rms,L}^2 \quad (48)$$

$$P_{Core,L} = \frac{f_s}{\frac{a}{B^3} + \frac{b}{B^{2.3}} + \frac{c}{B^{1.5}}} + d f_s^2 B^2 \quad (49)$$

where $R_{L,ESR}$ and $I_{L,rms}$ are the series parasitic resistances and the RMS current of inductor, respectively. Additionally, the coefficients a , b , c , and d are given by manufacturer.

2.9.5. Transformer Losses

Similar to the inductor, the losses of transformer include two main contributors, the copper loss and the core loss, which are express as:

$$P_{Cond,T} = R_{T,ESR} I_{dc}^2 \left\{ 1 + \sum_{n=1}^{\infty} \frac{R_{wn}}{R_{T,ESR}} \left(\frac{I_n}{I_{dc}} \right)^2 \right\} \quad (50)$$

$$P_{Core,T} = \frac{f_s}{\frac{a}{B^3} + \frac{b}{B^{2.3}} + \frac{c}{B^{1.65}}} + d f_s^2 B^2 \quad (51)$$

where $R_{T,ESR}$, R_{wn} , I_{dc} , and I_n are the series parasitic resistances, the AC winding resistance, the RMS current of transformer, and the RMS current of the n th frequency component, respectively.

The theoretical breakdown of total loss at half-load and full-load conditions are shown in Figure 8a,b, respectively. It can be seen that the switches and diodes are the major contributors to power loss in the proposed converter.

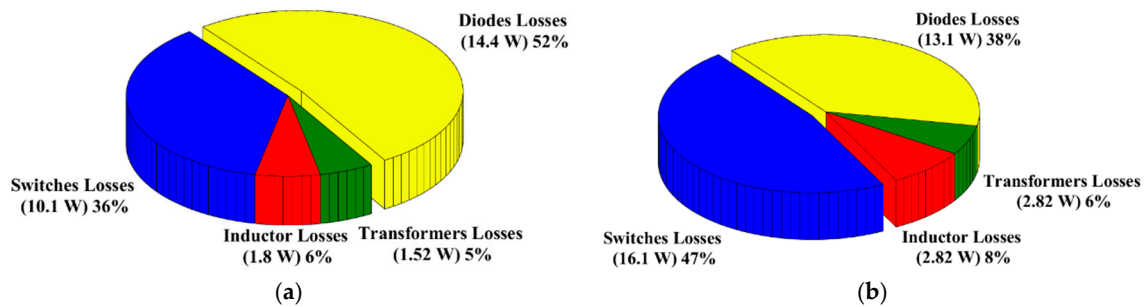


Figure 8. Loss breakdown (a) half-load condition ($P_o = 500$ W); and (b) full-load condition ($P_o = 1000$ W).

3. Design Considerations

3.1. Selection of Turns Ratio

The proper selection of the turns ratio helps employ the switches with lower voltage rating. The turns ratio can be achieved from (31), and expressed as:

$$n = \frac{V_o(1-D) - V_{in}}{4V_{in}} \quad (52)$$

3.2. Choice of Leakage Inductance

The leakage inductance plays an important role in the operation of converter regarding ZVS performance and voltage gain. It can be calculated from (29) and is given by:

$$L_k = \frac{nDV_{in}(1 - (1 - 2k)^2)}{8I_o f_s} \quad (53)$$

3.3. Choice of Magnetizing Inductance

A good criterion for selecting the magnetizing inductance is to help the switches to obtain ZVS. Thus, it can be derived from Equation (39) as follows:

$$L_{m1} = L_{m2} > \frac{T_s DV_{in}}{\frac{2L_B P_o - DT_s V_{in}^2}{2V_{in} L_B} - \frac{8nP_o}{(1-D)V_o}} \quad (54)$$

3.4. Choice of Boost Inductance

The boost inductance is adopted to reduce the input current ripple, so to have 20% current ripple ratio, the required boost inductance can be obtained from:

$$L_B = \frac{V_{in} D_{max} T_s}{20\% I_{in}} \quad (55)$$

3.5. Design of Capacitors

From the operating principle of proposed converter along with charge-second balance on the capacitors, the capacitance can be selected as:

$$C_{o1} = \frac{(1 - D + d_1 - d_2)I_o}{f_s \Delta V_{o1}} \quad (56)$$

$$C_{o2} = \frac{(1 - D + d_1 - d_2)I_o}{f_s \Delta V_{o2}} \left(\frac{4n + 1}{1 - D} I_o - \frac{d_2 I_{D02} - (1 - D - d_2) I_{D01}}{2} \right) \quad (57)$$

$$C_{o3} = \frac{(1 - D + d_1 - d_2)I_o}{f_s \Delta V_{o3}} \quad (58)$$

$$C_{o4} = \frac{(D - d_1 + d_2)I_o}{f_s \Delta V_{o4}} \quad (59)$$

$$C_{m1} = C_{m2} = \frac{(D - d_1 + d_2)I_{D01}}{2f_s \Delta V_{cm1}} \quad (60)$$

$$C_r = \frac{(d_2 I_{D02} - (1 - D - d_2) I_{D01})(1 - D)}{2f_s \Delta V_{cr}} \quad (61)$$

where ΔV_{o1} , ΔV_{o2} , ΔV_{o3} , ΔV_{o4} , ΔV_{cm1} , and ΔV_{cr} denote the maximum allowed voltage ripples allowed for C_{o1} , C_{o2} , C_{o3} , C_{o4} , C_{m1} , and C_r , respectively. Additionally, f_s is the switching frequency.

4. Simulation and Experimental Results

To demonstrate the operation modes of the proposed converter along with its effectiveness, a scaled-down laboratory prototype is simulated and implemented. The specifications and components of studied converter are given in Table 2.

4.1. Simulation Results

To investigate the performance of the proposed converter, two simulations in full load and light load condition are done. In these simulations, the GaN switch model introduced by the company is used. The specifications of the converter is given in Table 2.

Table 2. Parameters and components of implemented converter.

Parameter	Value
Input DC-voltage (V_{in})	15–30 V
Output voltage (V_o)	400 V
Output power (P_o)	1000 W
Switching frequency (f_s)	100 kHz
Magnetizing inductance (L_{m1} and L_{m2})	100 μ H
Leakage inductance (L_{k1} and L_{k2})	10 μ H
Turns ratio of coupled inductors (n)	1.5
Switches	EPC2047 (200 V, 160 A, 10 m Ω)
Diodes	C3D10065E
Output capacitors (C_{o1} , C_{o2} , C_{o3} , and C_{o4})	47 μ F
Switched capacitors (C_{m1} and C_{m2})	10 μ F

4.1.1. Full Load Condition ($V_{in} = 22$ V, $P_o = 1000$ W, and $D = 0.65$)

Figure 9 demonstrates the functional current and voltage waveforms of simulated converter at the rated output power ($P_o = 1000$ W), including the ZVS performance of switches, the boost current i_{LB} , the secondary current i_{Sec} , and the current of diodes. From Figure 9a, it can be seen that the output voltage is adequately regulated by the control circuit. Figure 9b shows the current of boost inductor L_B and leakage inductor L_k , which confirms that the design of boost inductor is carried out correctly. Moreover, the leakage inductor current is varying linearly, following the theoretical analysis. The current of output diodes are demonstrated in Figure 9c, implying that ZCS performance at turn-off instant is realized for output diodes leading to the efficiency improvement. The soft-switching operation for main and clamp switches is shown in Figure 9b,c. It is clear that the voltage stress of switches becomes zero before the gate pulse of related switches is applied. Moreover, confirming the equations given in previous section, the voltage stress of switches is around 65 V, which is much lower than output voltage (400 V). Therefore, switches with smaller on-resistance can be used, contributing to fewer conduction losses.

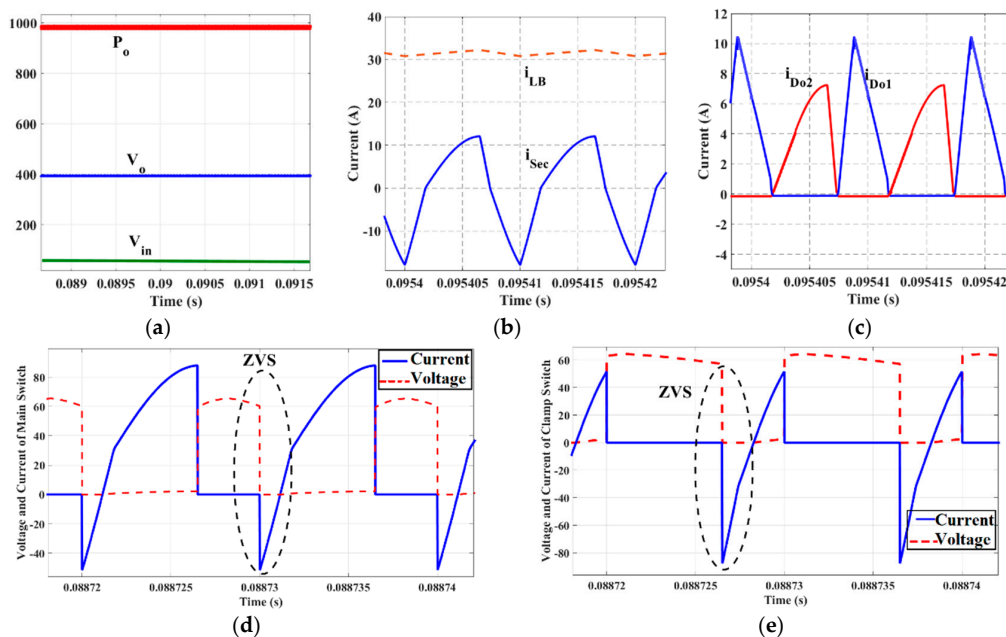


Figure 9. Simulation results. (a) Input voltage, output voltage, and output power; (b) the input current i_{LB} and the secondary side current i_{Sec} ; (c) current of the output diodes I_{Do1} and I_{Do2} ; (d) voltage and current of the main switch; and (e) voltage and current of the clamp switch.

4.1.2. Light Load condition ($V_{in} = 22\text{ V}$, $P_o = 100\text{ W}$, and $D = 0.48$)

Figure 10 shows the functional current and voltage waveforms of simulated converter during light loading ($P_o = 100\text{ W}$), including the ZVS performance of switches and the voltage of output diodes V_{D01} and V_{D02} . The soft-switching operation for main and clamp switches is shown in Figure 10a,b. It is clear that the voltage stress of switches becomes zero before the gate pulse of related switches is applied. Moreover, confirming the equations given in previous section, the voltage stress of switches is around 42 V , which is much lower than output voltage (400 V). Therefore, switches with smaller on-resistance can be used contributing to less conduction losses. Figure 10c illustrates the voltage stress of the output diodes, which is 180 V that is much lower than the output voltage. From Figure 10d, it can be seen that the voltage of capacitors is regulated enough with low ripple, implying the selection of the output capacitors are carried out correctly.

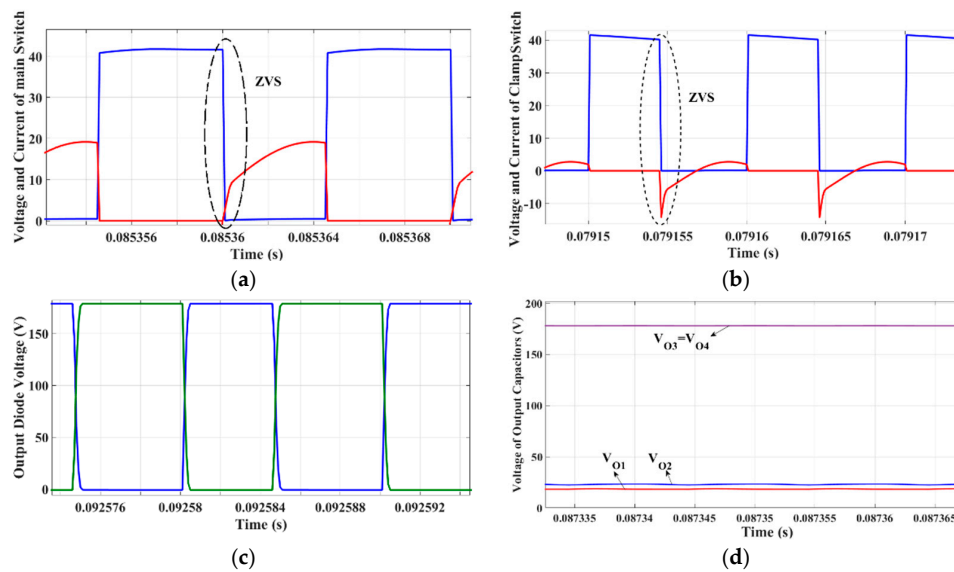


Figure 10. Simulation results during light loading when $P = 100\text{ W}$, $D = 0.45$, $V_{in} = 22\text{ V}$, and $V_o = 400\text{ V}$. (a) Voltage and current of the main switch; (b) voltage and current of the clamp switch. (c) voltage of the output diodes V_{D01} and V_{D02} ; and (d) voltage of the output capacitors V_{O1} – V_{O4} .

4.2. Experimental Results

In this section, the experimental results of implemented prototype with the specifications given in Table 2 are demonstrated. A photo of prototype converter is presented in Figure 11.

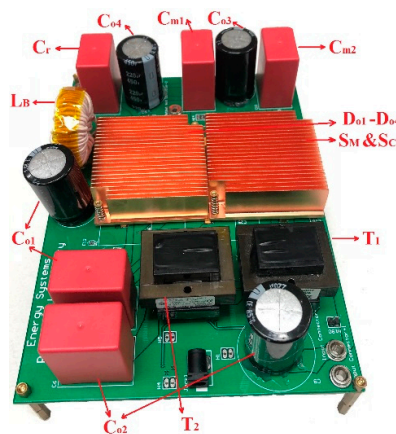


Figure 11. Photo of the implemented prototype.

The results demonstrating the performance of converter at full-load are shown in Figure 12. The gate pulse of switches is given in Figure 12a, implying the driver circuit is effectively generating the signals for GaN switches. Moreover, it can be observed that there is no ringing in the gate-pulse; thus, a false turn-on or turn-off is avoided. Figure 12b demonstrates the current of boost inductor L_B and the current of leakage inductor L_k . The input current has a low ripple that proves the validity of equation given for designing the boost inductor. Regarding the impact of current ripple on the efficiency and lifetime of PV source, the proposed topology can be a perfect candidate for power conversion in the PV-based DC microgrid. The voltage of output capacitors and input voltage are shown in Figure 12c. It is apparent from this figure that the voltage ripple of capacitors is in the acceptable range. Figure 12d,e show the drain-source voltage and current of switches S_M and S_C , respectively. The turn-on instant clearly indicates that the voltage across switch becomes zero before the gate pulse of switch is applied, implying ZVS is achieved. This can lead to a considerable improvement in the efficiency of converter since the switching loss is the main contributor to the loss of the high step-up converters. Moreover, the voltage stress across the switches are confined properly by adopting an active-clamp configuration. The voltage stress and the current of output diodes D_{O1} and D_{O2} are presented in Figure 12f. It is clear that the falling slope of diodes current is controlled by the leakage inductance; consequently, the turn-off loss of the diodes is reduced.

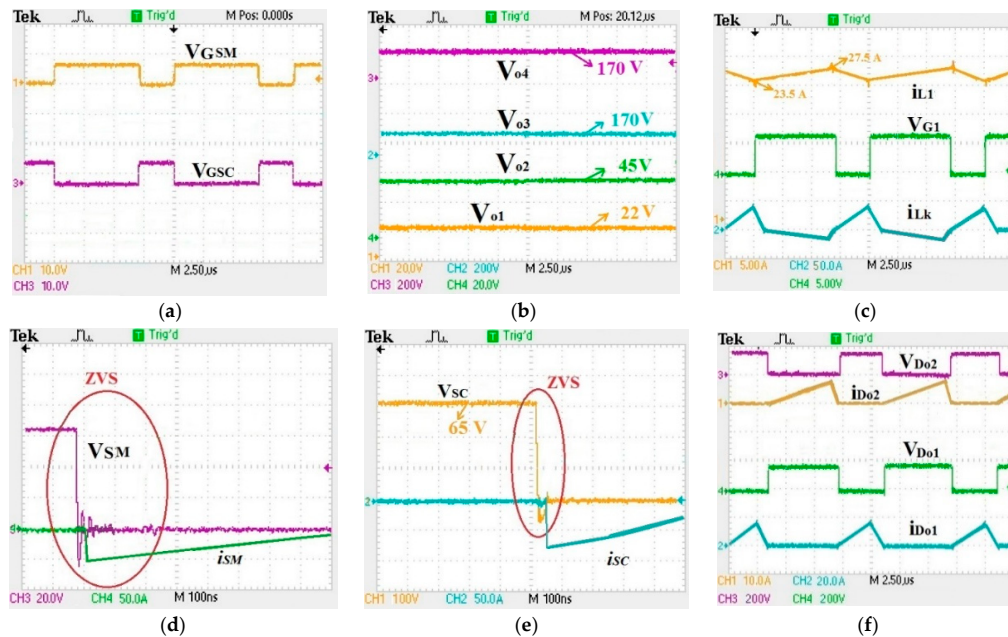


Figure 12. Experimental results for rated power when $V_{in} = 20$ V, $D = 0.65$, and $P_{out} = 1000$ W. (a) Gate-source voltage of switches S_M and S_C ; (b) the voltage of output capacitors; (c) the current of boost inductor and leakage inductor, and gate pulse of main switch; (d) gate-source and drain-source voltage of switch S_M ; (e) gate-source and drain-source voltage of switch S_C ; and (f) the voltage and current of output diodes D_{O1} and D_{O2} .

Since the soft-switching at light load is critical for high step-up converters, the performance of converter at half of rated power is investigated. Figure 13 shows the results for a test done at half load ($P_o = 500$ W). Figure 13a demonstrates the gate pulse of switches S_M and S_C , and the output voltage V_o . It indicates that the duty cycle (D) of main switch is equal to 0.5, which confirms the Equation (31). The drain-source voltage and current of switches S_M and S_C are illustrated in Figure 13b,c, respectively. The turn-on instant clearly indicates that the voltage across the switch becomes zero before the gate pulse of switch is applied. This means ZVS is obtained for this loading condition, which can greatly lead to improvement in the efficiency of converter since the switching loss is responsible for major

losses of the high step-up converters, especially at light load. Figure 13d shows the voltage and currents flowing through the output diodes $I_{D_{O1}}$ and $I_{D_{O2}}$. This figure reveals that the current of the diodes is controlled by the leakage inductance of the transformers; thus, the overlap between the voltage and current during turn-off process can be reduced.

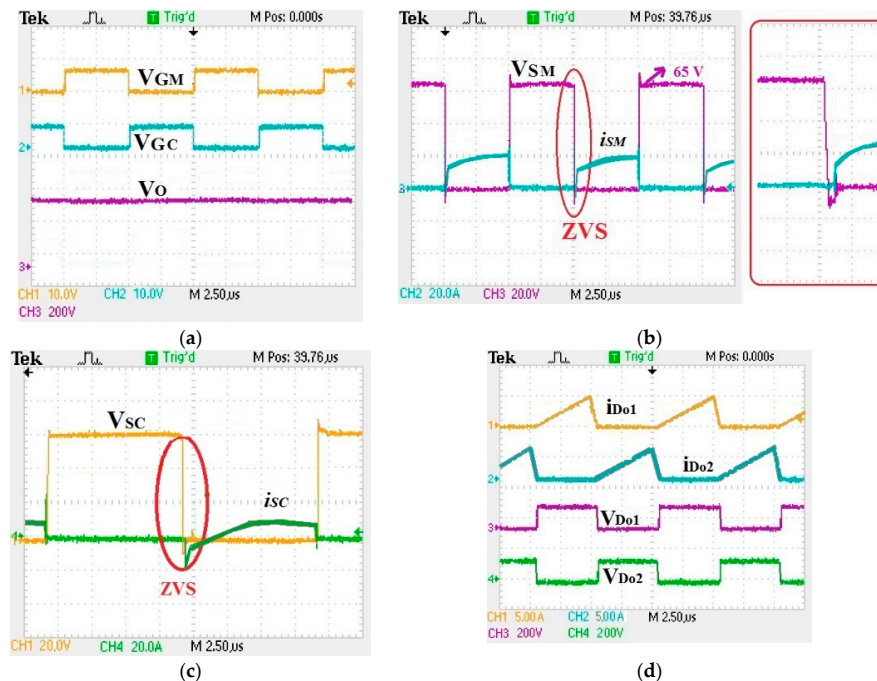


Figure 13. Experimental results for half load power when $V_{in} = 30$ V, $D = 0.5$, and $P_{out} = 500$ W. (a) Gate-source voltage of switches S_M and S_C , and output voltage V_O ; (b) gate-source and drain-source voltage of switch S_M ; (c) gate-source and drain-source voltage of switch S_C ; and (d) the voltage and current of output diodes D_{O1} and D_{O2} .

Figure 14 exhibits the measured and calculated efficiency using the equations given in Section 2.9. From Figure 14, the theoretical and measured efficiencies at full-load are 96.3% and 96.7%, respectively. It is noteworthy to mention that the maximum efficiencies achieved at an output power of 600 W are 97.3% and 97.1%, associated with the theoretical and measurement, respectively.

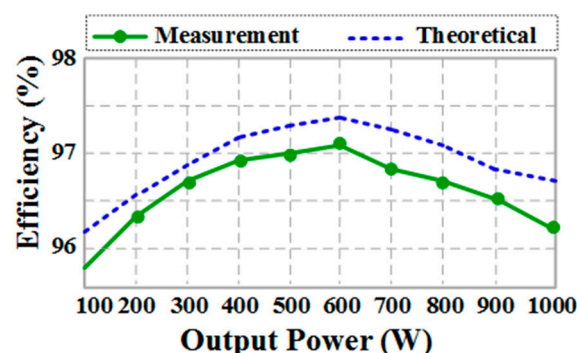


Figure 14. Calculated and measured efficiency versus output power.

5. Conclusions

A soft-switched high step-up DC/DC converter based on the dual half-bridge circuit is proposed in this paper. Presenting a high voltage gain, as well as the soft-switching performance for a wide range of input voltage and output power, the proposed converter is an excellent candidate for a DC/DC

converter as the front-end of the inverter in DC microgrid applications. The voltage multiplier concept and dual half-bridge are combined at the output stage to increase the voltage gain and reduce the voltage stress across the switches and diodes. To suppress the voltage ringing resulting from the leakage inductance of transformers, the active-clamp circuit is adopted, thus, switches with lower rated voltage can be used. To minimize the voltage stress of output capacitors, the symmetrical voltage multiplier is implemented at the rectifier stage that can ensure the voltage distribution evenly among output diodes. Furthermore, this stage increases the voltage gain by recycling the leakage energy to the output capacitors as well. The voltage stress of switches. A comparison is carried out to show the effectiveness of the proposed topology compared to state-of-the-art converters for EV applications. A 1-kW laboratory prototype of the proposed converter is implemented using GaN E-HEMTs and SiC Schottky diodes to validate the theoretical analysis.

Author Contributions: H.M. and N.E. developed the proposed research concept with a complete theoretical study. The hardware implementation is carried out by the same authors. O.M. is the supervisor who led the project, identified the ideas, checked the results, and edited the manuscript.

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