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A Dynamic Control Strategy for Active Balancing of Lithium-Ion Battery Packs with Energy Closed-Loop and Scenario-Adaptive Control

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Abstract

To address the usable capacity degradation and energy loss of lithium-ion battery packs caused by cell inconsistencies, this paper proposes a dynamic control strategy based on switch-array active balancing technology. First, a 16S (16-series-cell) standalone active balancing hardware system with a dual-transformer coupling architecture is designed to achieve bidirectional energy flow. Second, a phased control principle incorporating forced sequencing, pack energy closed-loop management, and interlocking mechanisms is proposed, and differentiated dynamic control strategies are formulated for two typical resting scenarios of energy storage battery packs, i.e., fully charged and fully discharged states. Simulation results show that the proposed strategy can effectively reduce the deviations in cell voltage and state of charge (SOC) within 24 h: in the high-SOC scenario, the maximum voltage difference among cells decreases from 94.46 mV to 4.73 mV, while the pack loses only 1.14% SOC; in the low-SOC scenario, the SOC deviation converges to within 0.6%, effectively preventing deep discharge of individual cells. The balancing topology and its repair effectiveness are further verified experimentally on a 16S platform. This study provides a theoretical basis and engineering reference for improving the consistency and energy utilization of lithium-ion battery packs.

Keywords: lithium-ion battery pack; active balancing; control strategy; scenario adaptation; energy closed-loop; hardware system

1. Introduction

With the development of new power systems and the new energy vehicle industry, lithium iron phosphate (LFP) batteries have been widely used in large-scale energy storage power stations and power battery applications owing to their high safety, long cycle life, and low cost [1]. In engineering practice, multiple cells are connected in series and in parallel to meet system voltage and capacity requirements [2,3]. Owing to differences in manufacturing processes, ambient temperature, cycling aging, and connection impedance, the state of charge (SOC), internal resistance, capacity, and open-circuit voltage of individual cells in a battery pack gradually diverge, giving rise to the cell inconsistency problem [4]. This not only reduces the overall energy utilization efficiency of the battery pack and causes energy loss, but also easily induces cell overcharging, overdischarging, and thermal safety hazards, significantly shortening the service life of the system [5]. Therefore, research on battery pack equalization technology for cell consistency management has become a research focus and engineering challenge in the field of battery management systems (BMSs).

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Meanwhile, it should be emphasized that advances in battery materials and electrode design—such as structural batteries, high-loading electrodes, and interface stabilization—mainly improve the intrinsic performance of individual cells, whereas the usable capacity of a series-connected pack is still governed by cell-to-cell inconsistencies arising from manufacturing tolerances, self-discharge differences, and temperature gradients; even with improved intrinsic cell performance, the weakest cell still limits the extractable pack capacity. Pack-level balancing is therefore complementary rather than alternative to material-level improvements: it recovers the usable capacity of the pack by reconciling the cell inconsistencies that material-level advances cannot eliminate.

Battery equalization technologies are mainly divided into passive equalization and active equalization. Passive equalization consumes excess electrical energy through shunt resistors. It features a simple structure and low cost, but suffers from low energy utilization and a small equalization current, making it suitable only for small, low-voltage battery packs and unable to meet the requirements of large-capacity, long-series energy storage batteries [6]. Active equalization realizes bidirectional transfer of energy across cells with the aid of inductors, transformers, switch arrays, and other components, effectively solving the energy-wasting problem of passive equalization. With the advantages of a large equalization current and flexible control, it has become the mainstream technical route in the industry [7]. Among these approaches, switch-array active equalization allows independent control of any individual cell and combines high equalization efficiency, a high degree of modularity, and moderate implementation cost, giving it broad application prospects in energy storage scenarios [8,9]. Existing studies have completed the hardware circuit design and performance verification of this topology, and have modeled the dynamic characteristics of batteries based on the second-order resistance–capacitance equivalent circuit model, laying a theoretical foundation for equalization algorithm simulation [10,11].

Although the hardware topology of switch-array active equalization is relatively mature, the supporting control strategies still have obvious deficiencies [3]. Most schemes adopt fixed thresholds and a single control logic without designing differentiated rules for typical idle conditions such as high-SOC and low-SOC states, resulting in poor scenario adaptability [12]. Some strategies lack energy closed-loop and circuit interlock designs, so that energy loss during the equalization process is not well controlled and the total energy of the battery pack is easily lost [13]. In addition, most studies provide insufficient quantitative analysis of the multiple inconsistencies in SOC, internal resistance, and capacity, and the parameter settings of equalization strategies mostly rely on experience and simplified assumptions [14]. At the module level, battery energy storage systems based on modular reconfigurable architectures also face challenges from multidimensional state inconsistencies in SOC, temperature, and aging rate. Yuan et al. [15] established a multi-dimensional feature model integrating electrical, thermal, and lifetime loss for modular reconfigurable battery energy storage systems, constructed a multi-objective optimization model that balances SOC equalization, temperature equalization, and lifetime loss cost, and introduced a successive convexification algorithm for efficient solving, providing a new idea for the refined management of energy storage systems under modular reconfigurable architectures. Overall, existing research has not yet formed a complete solution integrating topology modeling, quantitative analysis, and scenario-based equalization.

To address the above problems, this paper conducts research based on a 16S switch-array standalone active equalization hardware platform, using 320 Ah LFP cells as the research object. First, a phased dynamic equalization strategy is designed according to the hardware characteristics. Then, three control principles—phase ordering, energy closed-loop management, and circuit interlock—are introduced, and differentiated control logic is developed for high-SOC and low-SOC scenarios. Finally, a 24 h simulation case study is

used to verify the comprehensive performance of the strategy in converging voltage and SOC deviations and controlling energy loss. The balancing topology is further validated on the built 16S experimental platform. The research results can provide a reference for the algorithm development and engineering application of active equalization for large-capacity LFP battery packs. The main contributions of this work are threefold: (i) At the topology level, the superiority of the transformer-based balancing topology is verified through experimental comparison under identical conditions, demonstrating that the proposed balancing scheme outperforms the capacitor-based and inductor-based counterparts in both convergence speed and accuracy. (ii) At the control framework level, a two-phase deterministic balancing control framework is proposed, consisting of three constraints—charge/discharge mutual exclusion, energy closed-loop management, and an interlocking mechanism—wherein charge/discharge mutual exclusion eliminates control contention, energy closed-loop management minimizes the net energy loss of the pack, and the interlocking mechanism prevents false triggering and residual conduction paths at the hardware logic level; the combination of the three endows the balancing process with determinism, traceability, and safety. (iii) A scenario-adaptive mechanism is proposed, which adopts a charging-dominant, discharge-assisted balancing mode according to the SOC region of the pack.

2. Materials and Methods

2.1. Architecture of the 16S Standalone Active Equalization System

For a 16-series LFP energy storage module, this study designs a 16S switch-array active equalization hardware system. The system adopts a modular design and possesses the capabilities of bidirectional energy transfer, independent cell control, high-precision sampling, and low-power operation, which can meet the equalization requirements of large-capacity battery packs [8,9]. The core principle of switch-array equalization technology is shown in Figure 1a. Through the switch array, the target cells are selected: cells with obviously high voltage or high voltage at the end of charging are equalized by discharging, while cells with obviously low voltage or low voltage at the end of discharging are equalized by charging. Compared with traditional passive equalization and inductor-based active equalization topologies, this technical solution has the significant advantages of high transfer efficiency, a large equalization current, independent control, and moderate cost.

The hardware system adopts a dual-transformer coupling architecture to realize bidirectional energy flow, as shown in Figure 1b. During charging equalization, energy is drawn from the pack bus and, after step-down and isolation through the transformer, charges the lagging cells in constant-current/constant-voltage (CC/CV) mode at 3 A/3.65 V. During discharging equalization, the energy of the high-voltage cells is fed back to the pack bus at a constant current of 1 A through step-up isolation via the transformer, realizing energy recovery and utilization. The dual-transformer design ensures electrical isolation between the charging and discharging loops, avoiding circuit interference during mode switching.

The hardware is equipped with an independent switch array that can select any individual cell for equalization charging or discharging, avoiding the circuit interference caused by simultaneous multi-channel operation and ensuring control stability. The main functional parameters of the system are listed in Table 1. The system integrates 16-channel voltage sampling and one-channel temperature sampling, and exchanges data with the BMS via the Modbus protocol. The static (standby) current consumption of the whole unit is lower than 6 μA, corresponding to a standby power of only about 22 μW at a cell voltage of 3.65 V, and it supports timed wake-up and manual wake-up, making it suitable for the long-term idle operation of battery packs.

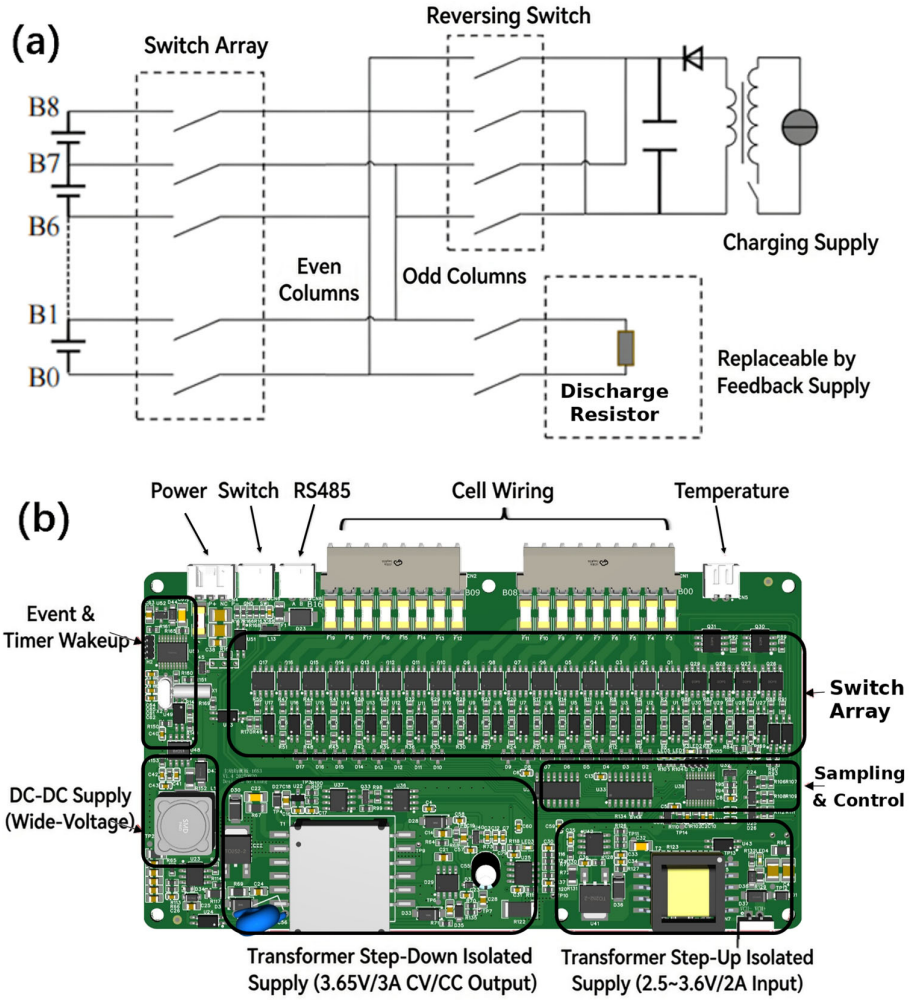


Figure 1. (**a**) Principle of switch-array active equalization technology; (**b**) 16S standalone active equalization hardware system.

Table 1. Key specifications of the 16S standalone active equalization hardware system.

Module	Item	Specification
Voltage sampling	Number of channels/range/accuracy	16 channels, 0–5 V, error <10 mV
Temperature sampling	Number of channels/range/accuracy	1 channel, −45–135 °C, ±1 °C
CC/CV charging	Current range/voltage range	1–3 A (factory setting)/3.65–4.2 V (factory setting)
Constant-resistance/ current discharging	Resistance range/current range	1–3 Ω (factory setting)/1–2 A (factory setting)
RS-485 communication	Protocol/usage	Modbus protocol, parameter setting and status reading
Low-power operation	Static power consumption/wake-up	<6 μA, timed wake-up or manual wake-up

The power switches of the switch array are N-channel MOSFETs of model AGM408MN; channel selection and polarity reversal in the array are controlled by 74HC138B 3-to-8 line decoders; the transformer of the isolated supply is a custom-wound EFD15-5+5; and the cell wiring terminals are of model XHB-2AW.

AGM408MN, 74HC138B and XHB-2AW are general-purpose, commercially available types that can be procured by model number, and no manufacturer was specified in the design; EFD15-5+5 is a custom-wound part. As the prototype was built as a single unit, the

components were supplied by the JLC platform together with PCB fabrication and assembly and were not purchased separately by the authors; the manufacturers were therefore not traced individually, and component provenance is reported here at the level of model and specification. The components are general-purpose types produced to the same specification by multiple manufacturers and are electrically interchangeable, so the manufacturer does not constitute a variable affecting the reproducibility of the experiments.

To validate the effectiveness of the equalization strategy, this paper conducts simulation analysis based on the battery equivalent circuit model established in previous research. The model has been experimentally verified and can accurately reflect the dynamic characteristics of LFP batteries during charging and discharging [10].

2.2. Simulation Circuit Model of the Equalizer

The equalization simulation circuit model is shown in Figure 2. The model simulates the dual-transformer coupling architecture (T1/T2) to realize bidirectional energy flow control between the battery pack and individual cells. The charging loop is isolated and coupled through transformer T1, and a CC/CV source provides controlled charging energy; cells are charged in CC/CV mode at 3 A/3.65 V through switch SW1 and current-limiting resistor R1. The discharging loop is isolated and coupled through transformer T2, and a constant-current load actively discharges the cells at 1 A, with the energy fed back to the pack bus. The topology adopts switch Q1 and freewheeling diode D1 to form a chopper/rectifier topology, and uses changeover switches SW1/SW2 to select between the charging and discharging modes, ensuring that the two processes do not interfere with each other and are electrically isolated.

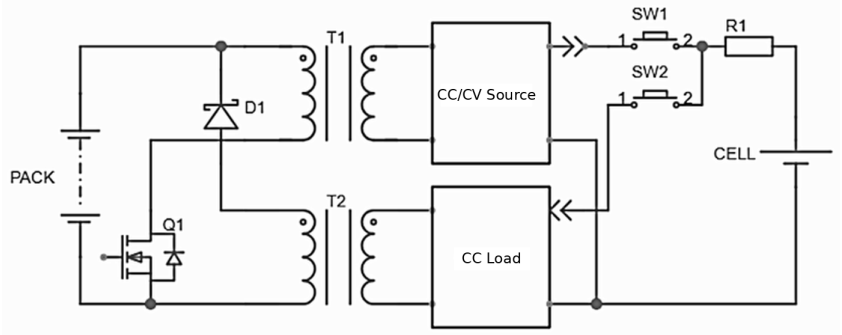


Figure 2. Equalization simulation circuit model.

The model parameters are listed in Table 2. The charging efficiency of 80% and discharging efficiency of 65% are set comprehensively based on the measured conversion efficiency range of the direct-current–direct-current (DC–DC) converter in the hardware platform and the typical efficiency values in similar transformer-based equalization topology studies.

Table 2. Parameters of the equalization circuit model.

Parameter	Symbol	Value	Unit
Balancing loop resistance	R_1	100	mΩ
Charging efficiency	η_{charge}	80	%
Discharging efficiency	$\eta_{discharge}$	65	%
CC charging current	I_{cc}	3	A
DC/DC output voltage limit	V_{cv}	3.65	V
Discharging current	I_{dis}	1	A

2.3. Charging and Discharging Equalization Characteristics of a Single Cell

To reasonably set the parameters of the equalization strategy, the characteristics of a single cell under the charging equalization and discharging equalization modes are first analyzed.

(1) Charging equalization characteristics.

Figure 3 compares the charging equalization effects of a single cell in the low-SOC region (<5%) and the high-SOC region (>95%). The simulation results show that in the low-SOC region, the voltage difference among the 16 cells is quickly narrowed within 2 h, whereas in the high-SOC region, only a 1.71% SOC gap is compensated within 2 h and the remaining 1.29% gap is not eliminated; moreover, the DC/DC conversion loss increases in the high-voltage region, reducing the overall efficiency. This is because the slope of the open-circuit voltage (OCV)–SOC curve in the low-SOC region is relatively steep, so the same current induces a larger voltage change and a faster equalization speed. In addition, the target cell voltage is low, leaving sufficient output voltage margin for the DC/DC converter to maintain the 3 A constant charging current for a longer time. In contrast, in the high-SOC region, the voltage approaches the charging cutoff voltage, the DC/DC voltage limit intervenes earlier, and the actual current may be lower than 3 A.

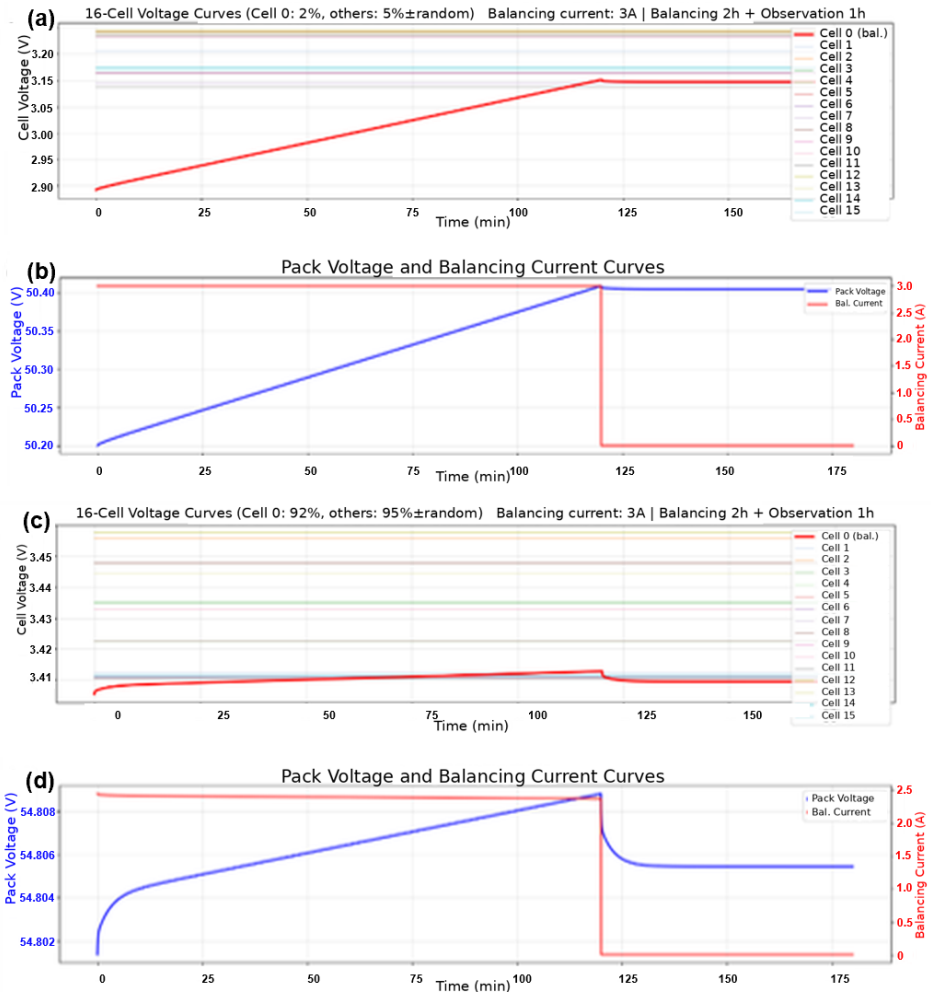


Figure 3. Comparison of charging equalization effects at high and low SOC levels: (**a**) cell voltage comparison in the low-SOC region; (**b**) pack voltage and current curves in the low-SOC region; (**c**) cell voltage comparison in the high-SOC region; (**d**) pack voltage and current curves in the high-SOC region.

(2) Discharging equalization characteristics.

Figure 4 compares the discharging equalization effects of a single cell in the low-SOC and high-SOC regions. Under the same discharging current of 1 A, the SOC drop of the cell is 0.71% within 2 h in both regions, but the voltage drop in the high-SOC region is 34 mV, which is more obvious than the 11 mV drop in the low-SOC region, owing to the larger slope of the OCV–SOC curve in the high-SOC region. This characteristic implies that in the voltage plateau region, the discharging equalization effect judged by voltage is less sensitive than in the high-SOC region, and SOC estimation needs to be combined for a more accurate equalization judgment.

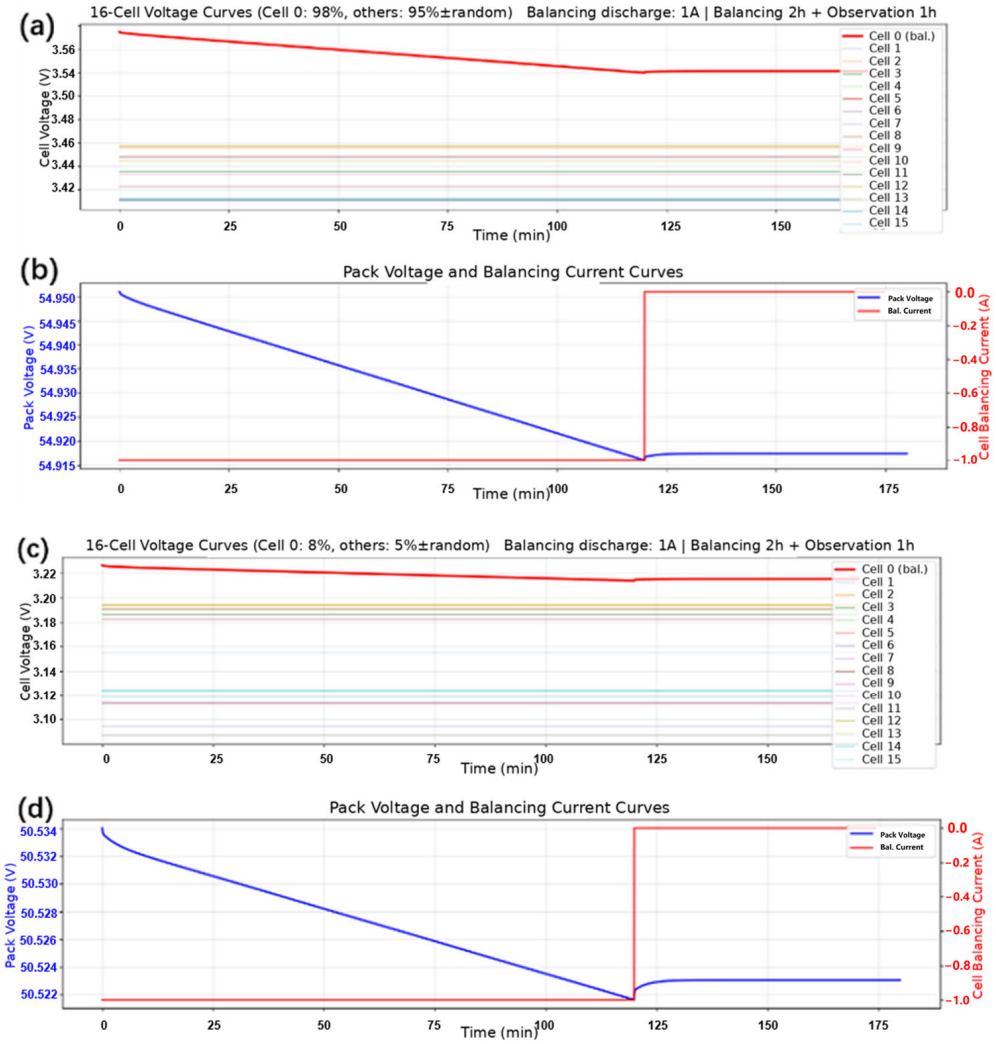


Figure 4. Comparison of discharging equalization effects at high and low SOC levels: (**a**) cell voltage comparison in the high-SOC region; (**b**) pack voltage and current curves in the high-SOC region; (**c**) cell voltage comparison in the low-SOC region; (**d**) pack voltage and current curves in the low-SOC region.

Based on the above characteristics, charging equalization should be prioritized in the low-SOC region to take advantage of the steep slope to converge the voltage quickly, while in the high-SOC region, discharging equalization combined with SOC judgment should be adopted.

2.4. Phased Balancing Control Logic and Three Constraint Principles

Based on the above analysis of the charging and discharging equalization characteristics, this paper proposes a phased balancing control logic that includes two phases and three constraint principles.

It should be noted that 5 mV is the target convergence threshold of the balancing control rather than a criterion triggered by a single sampling. Since the voltage sampling error of the hardware is less than 10 mV, to avoid false equalization actions caused by sampling noise, the control algorithm adopts a multi-sampling confirmation mechanism: the voltage judgment is based on the moving average of multiple consecutive samplings, and both the trigger and stop actions need to continuously satisfy the threshold condition before execution, thus ensuring the reliability of the control criterion under the existing sampling accuracy. Specifically, the cell voltages are sampled at 10 Hz, and a moving-average filter with a window of $n = 16$ consecutive samples is applied before the threshold judgment, which reduces the equivalent random sampling error to approximately $1/\sqrt{n}$ (about 25%) of the single-sample error, i.e., to below 2.5 mV—well within the 5 mV threshold. In addition, a trigger or stop action is executed only when the threshold condition is continuously satisfied for five consecutive filtered judgments ($n = 5$), and the filter window is re-initialized after each phase switching so that stale samples cannot cause false actions.

Phase (1) (charging equalization): Energy flows from the pack bus to the target cells whose voltage is lower than the pack average by more than 5 mV, compensating for their energy deficit. The controller traverses all cells and selects the cell with the lowest voltage deviation from the average for priority charging until the difference between the cell voltage and the average is less than 5 mV or the charging cutoff condition is reached. The trigger condition can be expressed as Equation (1):

$$V_i \leq V_{avg} - \Delta V_{th}, \ \ \Delta V_{th} = 5 \text{ mV} \tag{1}$$

where V_i is the voltage of cell i and V_{avg} is the average voltage of all cells. The 5 mV trigger threshold is set with reference to the cell factory sorting consistency requirements and the engineering practice of energy storage, striking a balance between convergence speed and equalization action frequency.

Phase (2) (discharging equalization): After Phase I is completed, the energy of the cells whose voltage is higher than the average by more than 5 mV is fed back to the pack bus to lower their voltage. The cell with the highest voltage is preferentially selected for discharging equalization until the voltage difference is less than 5 mV or the discharging cutoff condition is reached. The trigger condition can be expressed as Equation (2):

$$V_i \geq V_{avg} + \Delta V_{th}, \ \ \Delta V_{th} = 5 \text{ mV} \tag{2}$$

The above two-phase control follows three constraint principles, as shown in Figure 5.

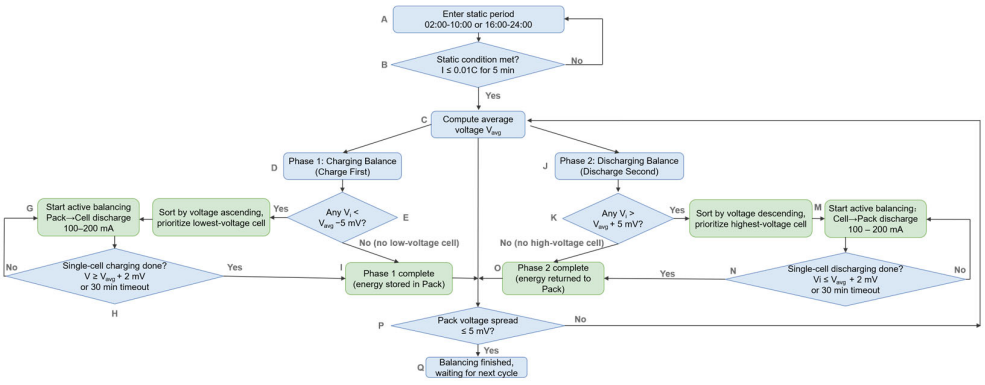


Figure 5. Balancing control logic and constraint principles.

Principle 1—Forced phase ordering: Regardless of whether the pack is in a fully charged or fully discharged state, the controller must strictly follow the "charge first, then discharge" order; even if a certain phase has no execution target, the logic judgment must still be completed. This principle ensures the determinism and traceability of the balancing process and avoids over-equalization or under-equalization caused by logic confusion. The order is designed based on both safety and efficiency considerations: charging first can promptly raise the voltage of lagging cells and prevent them from sliding into deep discharge in low-SOC scenarios; meanwhile, establishing an energy margin before executing discharge feedback can improve the recovery effect of the pack energy closed-loop management.

Principle 2—Pack energy closed-loop management: In Phase I, energy is drawn from the pack bus to charge low-voltage cells, and the total energy of the pack temporarily decreases; in Phase II, the energy of high-voltage cells is fed back to the pack bus, and the total pack energy recovers. The net SOC loss of the pack is negligible, realizing energy closed-loop management. Hereinafter, "energy closed-loop management" denotes the mechanism by which the balancing energy is drawn from and fed back to the pack bus so that the net pack energy loss is minimized, while "scenario-adaptive balancing strategy" denotes the rule set that selects charging-dominant or discharging-assisted equalization according to the pack SOC region.

Principle 3—Interlocking mechanism: Charging cell A and discharging cell B are not allowed at the same time; a 5 min interval is set between Phase I and Phase II for voltage sampling stabilization and circuit topology switching, avoiding electrical interference and safety hazards caused by the simultaneous conduction of the charging and discharging loops.

Principle 4—Cell voltage safety clamping: During Phase I charging equalization, the equalization current of the selected cell is regulated in a closed loop; when the cell voltage approaches 3.60 V, the equalization current is ramped down, and upon reaching 3.65 V the charging equalization of this cell is terminated immediately and the controller switches to the discharging phase for this cell. Together with the forced phase ordering of Principle 1, this clamping mechanism guarantees that the "charge first" sequence never drives any cell into overvoltage, which addresses the overvoltage concern in both the high-SOC and the low-SOC scenarios.

2.5. Scenario-Adaptive Balancing Strategy

In the typical daily operation of energy storage battery packs, there are two key balancing periods: full-charge idle and full-discharge idle. According to the cell state characteristics in these two periods, this paper designs a differentiated scenario-adaptive balancing strategy, as shown in Figure 6.

The two scenarios are defined by explicit pack-level SOC criteria: when the pack SOC is not lower than 90%, the pack is considered to be in the high-SOC scenario, in which all cells reside on the charging voltage plateau, the OCV–SOC curve is flat, and the sensitivity of the voltage criterion decreases, so the controller selects the charging–discharging combined rule set with charging equalization as the main mode (Period A); when the pack SOC is not higher than 20%, the pack is in the low-SOC scenario, in which deep discharge of individual cells is the dominant risk, so the controller selects the charging-equalization-dominant rule set (Period B) and monitors the total pack SOC to prevent over-discharge. During operation, the scenario-adaptive controller first reads the pack SOC, determines the scenario according to these criteria, and then executes the corresponding rule set. It should be additionally emphasized that the proposed strategy is in principle not restricted to idle conditions. The choice to conduct the balancing analysis during rest periods in this work is made solely out of consideration for methodological rigor.

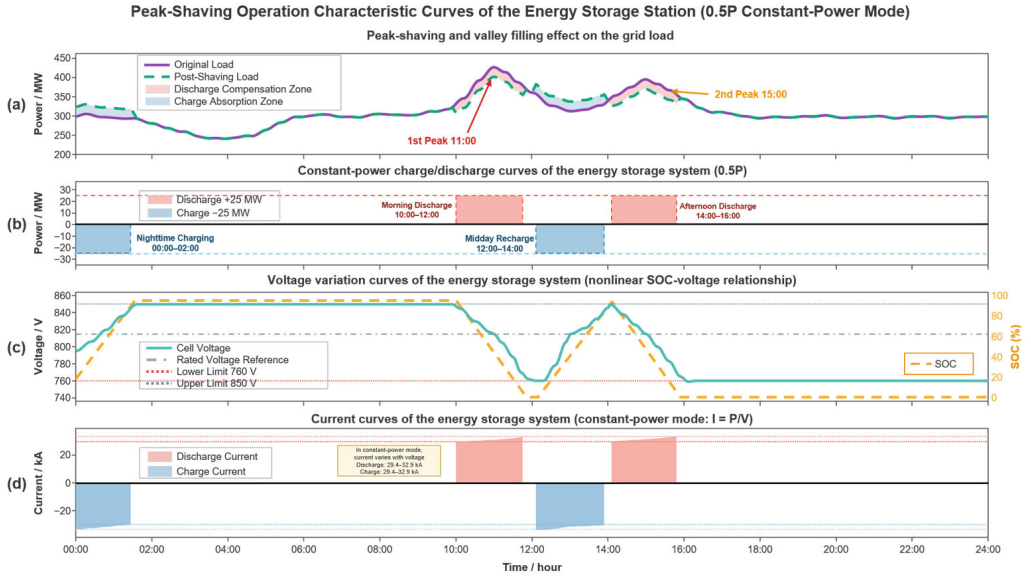


Figure 6. Peak-shaving operating characteristic curves of an energy storage power station (0.5P constant power mode): (**a**) grid load peak-shaving and valley-filling effect; (**b**) constant power charging/discharging curves of the energy storage system (0.5P); (**c**) voltage curve of the energy storage system (nonlinear SOC–voltage relationship); (**d**) current curve of the energy storage system (constant power mode: I = P/V).

Period A (02:00–10:00, full-charge idle, SOC ≈ 100%): All cells are in the full-charge plateau, and the voltage difference mainly originates from capacity decay and self-discharge differences. The equalization strategy combines charging and discharging, with charging equalization as the main mode (top equalization): if there are obviously lagging cells, energy is drawn from the pack to replenish them, with a single-cell voltage upper limit of 3.65 V; the charging phase stops immediately once the limit is reached. Subsequently, the energy of overcharged or high-voltage cells is drawn back to the pack so that the whole pack voltage converges. This scenario focuses on the overcharging risk.

Period B (16:00–24:00, full-discharge idle, SOC ≈ 0–20%): All cells are in the discharged plateau or low-SOC state. The equalization strategy mainly adopts charging equalization (bottom equalization): lagging cells are replenished with energy from the pack to prevent deep inconsistency and deep discharge; during execution, the total pack SOC must be monitored to prevent pack over-discharge caused by excessive energy extraction. If high-voltage cells exist, their energy is fed back to the pack. This scenario focuses on the deep-discharge risk.

3. Results

To validate the effectiveness of the proposed strategy, typical cases were designed and analyzed by simulation, complemented by experimental validation on the built hardware platform. The simulation platform is based on the battery equivalent circuit model and the equalization circuit model, taking 16 series-connected 320 Ah LFP cells as the object with a discharge operating parameter of 0.5C, and is used to verify the scenario-level dynamic behavior of the complete control strategy under controlled conditions (Sections 3.1 and 3.2). The hardware platform consists of an actual battery module formed by 16 series-connected 280 Ah cells connected to an active balancing module; the battery module is charged and discharged by a battery charge–discharge tester to support the experimental topology comparison presented in Section 3.3. The equivalent circuit parameters for battery cells and the setup conditions for high- and low-SOC scenarios are shown in Tables 3 and 4.

Table 3. Cell equivalent-circuit parameters.

Parameter	Symbol	Value
Number of cells	N	16, series-connected (16S)
Nominal capacity	Q	320 Ah
Ohmic resistance	R_0	0.22 mΩ
Fast polarization resistance	R_{ps}	0.45 mΩ
Fast polarization capacitance	C_{ps}	15 kF
Slow polarization resistance	R_{pl}	0.75 mΩ
Slow polarization capacitance	C_{pl}	250 kF
Terminal voltage equation	—	$V = OCV(SOC) + u_{ps} + u_{pl} + I \cdot R_0$

Table 4. High- and low-SOC scenario settings.

Parameter	High-SOC Scenario	Low-SOC Scenario
Initial SOC baseline	95% ± 2%	5% ± 2%
Initial SOC of the 16 cells (%)	94.50, 96.80, 95.93, 95.39, 93.62, 93.62, 93.23, 96.46, 95.40, 95.83, 93.08, 96.88, 96.33, 93.85, 93.73, 93.73	4.50, 6.80, 5.93, 5.39, 3.62, 3.62, 3.23, 6.46, 5.40, 5.83, 3.08, 6.88, 6.33, 3.85, 3.73, 3.73
SOC spread	3.80 percentage points	3.80 percentage points
Initial terminal voltage	3.4076~3.5021 V	2.995~3.209 V
Initial maximum voltage deviation	94.46 mV	213.41 mV
Initial pack voltage	55.01 V	49.99 V

3.1. Balancing Performance in the High-SOC Scenario

The initial conditions of the high-SOC scenario set the SOC of the 16 cells to 95% ± 2%, with an initial maximum voltage deviation of 94.46 mV and a relatively dispersed cell voltage distribution. The balancing strategy triggers charging equalization when the cell voltage is 5 mV below the average (confirmed by multiple samplings), prioritizing the lowest-voltage cell; it triggers discharging equalization when the voltage is 5 mV above the average, prioritizing the highest-voltage cell. Charging and discharging are not performed simultaneously; charging takes priority, and charging equalization is dominant.

Figure 7 shows the voltage and SOC evolution trends of the 16 cells during the 24 h balancing process in the high-SOC scenario. It can be seen that the voltage dispersion of the cells is large in the initial stage and gradually converges as the balancing process proceeds. In the early stage, charging equalization dominates, continuously replenishing low-voltage cells; in the later stage, a small number of cells trigger discharging equalization, feeding excess energy back to the pack. The whole balancing process lasts about 18 h, including 17 h of charging and 1 h of discharging, after which all cells enter a stable state.

The energy-loss index is defined as the ratio of the net charge drawn from the pack terminals during the balancing process to the pack capacity, with the charging and discharging efficiencies taken as 80% and 65%, respectively. Taking the high-SOC scenario as an example, the balancing energy loss is calculated in the following equation, and the energy transfer values during the balancing process are shown in Table 5.

$$\text{SOC loss} = \frac{Q_{ch}/\eta_c - Q_{dis}\cdot\eta_d}{16 \times 320\ \text{Ah}} = \frac{48.75/0.80 - 4.00 \times 0.65}{5120} = \frac{60.94 - 2.60}{5120} = 1.14\% \quad (3)$$

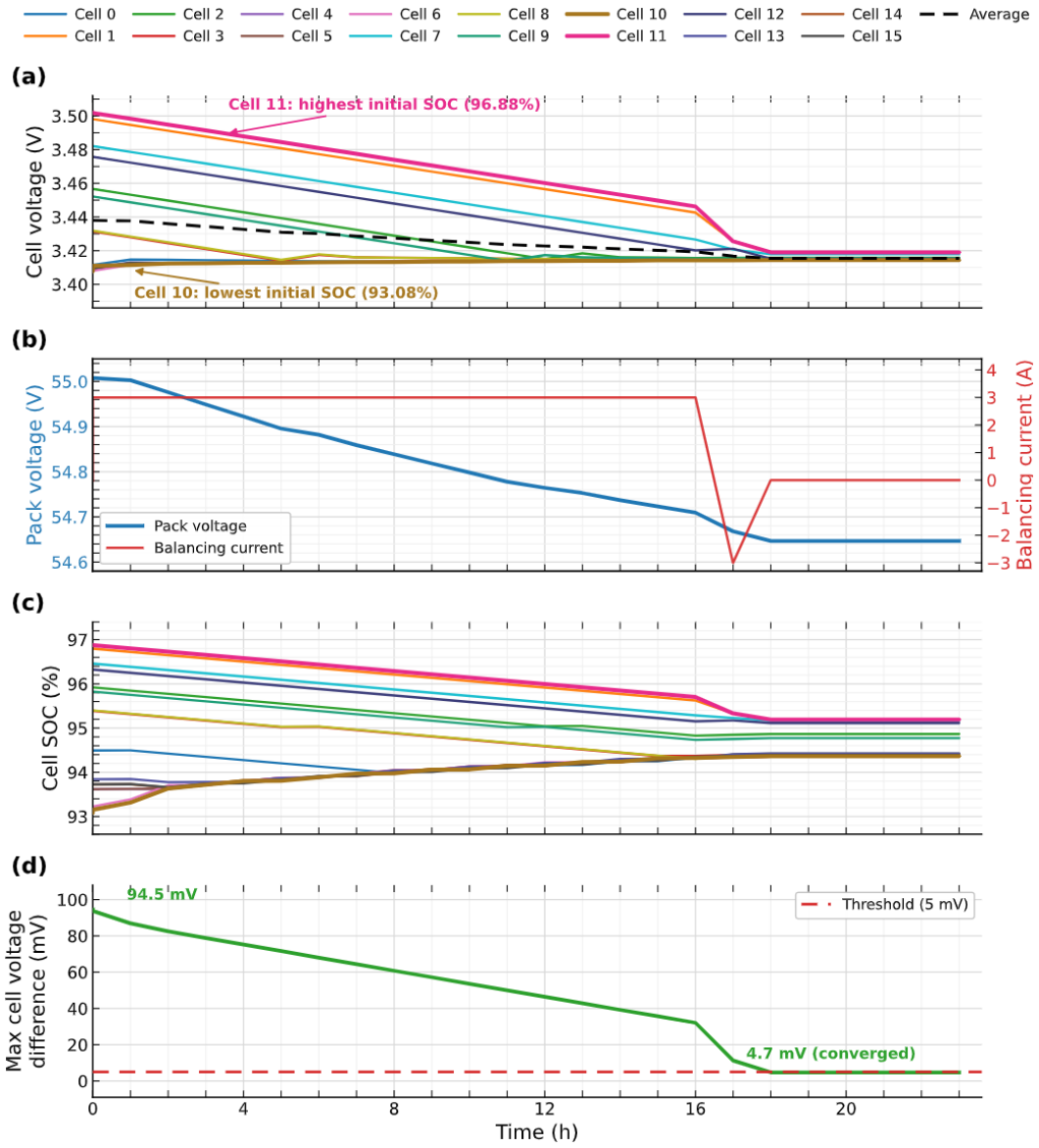


Figure 7. Voltage and SOC evolution during the 24 h balancing process in the high-SOC scenario: (**a**) voltage variation in the 16 cells (SOC = 95% ± 2%, 24 h balancing, including pack efficiency); (**b**) pack voltage and balancing current; (**c**) SOC variation in each cell (considering pack efficiency: charging 80%, discharging 65%); (**d**) maximum voltage difference between cells.

Table 5. Charge and energy balance of the 24-h high-SOC equalization case.

Item	Charge (Ah)	Energy (kWh)
Charging equalization: charge delivered into the lowest cells	48.75	2.67
Charging equalization: drawn from the pack (48.75/0.80)	60.94	3.34
Charging conversion loss (20%)	12.19	0.67
Discharging equalization: charge removed from the highest cell	4.00	0.22
Discharging equalization: charge returned to pack (4.00 × 0.65)	2.60	0.14
Discharging conversion loss (35%)	1.40	0.08
Net withdrawal from the pack (the 1.14% metric)	**58.34**	**3.20**
Irreversible loss (12.19 + 1.40)	**13.59**	**0.74**

The simulation results show that the proposed strategy can effectively reduce the maximum voltage difference among cells in the high-SOC scenario from 94.46 mV to 4.73 mV within 24 h, a convergence of 95%, successfully converging to within the 5 mV threshold. The SOC deviation converges from an initial maximum of about 3.8% to about 0.8%, and the consistency is significantly improved. Regarding pack energy loss, owing to the charging equalization efficiency of about 80%, the pack loses about 1.14% SOC in total, and the energy loss is controlled within a reasonable range. In terms of time allocation, charging equalization accounts for 17 h and discharging equalization only 1 h, indicating that in the high-SOC scenario, low-voltage cells are mainly replenished by charging, with less demand for discharging equalization, which is consistent with the scenario characteristics.

3.2. Balancing Performance in the Low-SOC Scenario

The initial conditions of the low-SOC scenario set the SOC of the 16 cells to 5% ± 2%, with an initial maximum voltage deviation of 213.41 mV, and some cells are at risk of deep discharge. The low-SOC scenario adaptive strategy is adopted for the 24 h simulation, in which only charging equalization is performed.

Figure 8 shows the voltage and SOC evolution trends of the 16 cells during the 24 h balancing process in the low-SOC scenario. It can be seen that the SOC of the lagging cells gradually increases during the balancing process and the overall consistency continues to improve. However, owing to the large slope of the OCV–SOC curve in the low-SOC region, the same SOC difference leads to a larger voltage difference, and the voltage convergence speed is relatively slow. After balancing, the voltage difference remains at 56 mV, which has not yet converged to the 5 mV threshold, and a longer time is required for complete convergence.

The simulation results show that the SOC equalization effect in the low-SOC scenario is better than that in the high-SOC scenario: the SOC of all cells converges to the 4.4–5.1% range with a deviation of only 0.6%, effectively avoiding deep discharge of individual cells. However, since only charging equalization is performed in the low-SOC region, the pack energy continues to flow out, and the pack SOC drops by about 1.76% within 24 h, which is higher than the 1.14% in the high-SOC scenario. This indicates that there is room for further improvement in the voltage convergence speed and energy efficiency of the low-SOC scenario, which can be optimized by appropriately increasing the proportion of discharging equalization when the voltage difference permits.

Regarding the residual voltage difference of 56 mV after balancing, three points should be clarified. First, the slope of the OCV–SOC curve in the low-SOC region is relatively large, and a SOC deviation of 0.6% corresponds to a voltage difference of tens of millivolts in this region; the voltage-domain criterion amplifies the SOC deviation, and the residual voltage difference does not mean that the SOC consistency is not up to standard. Second, from the safety perspective, under this residual voltage difference, all cell voltages are far from the discharge cutoff boundary, and there is no deep-discharge risk. Third, although continuing charging equalization can further compress the voltage difference, the marginal benefit diminishes and it is accompanied by continuous pack energy loss; comprehensively weighing these factors, the residual voltage difference is within the acceptable range for engineering. If further convergence is required, the equalization time can be extended or an SOC-domain equalization criterion can be introduced, and related work has been included in the follow-up research plan.

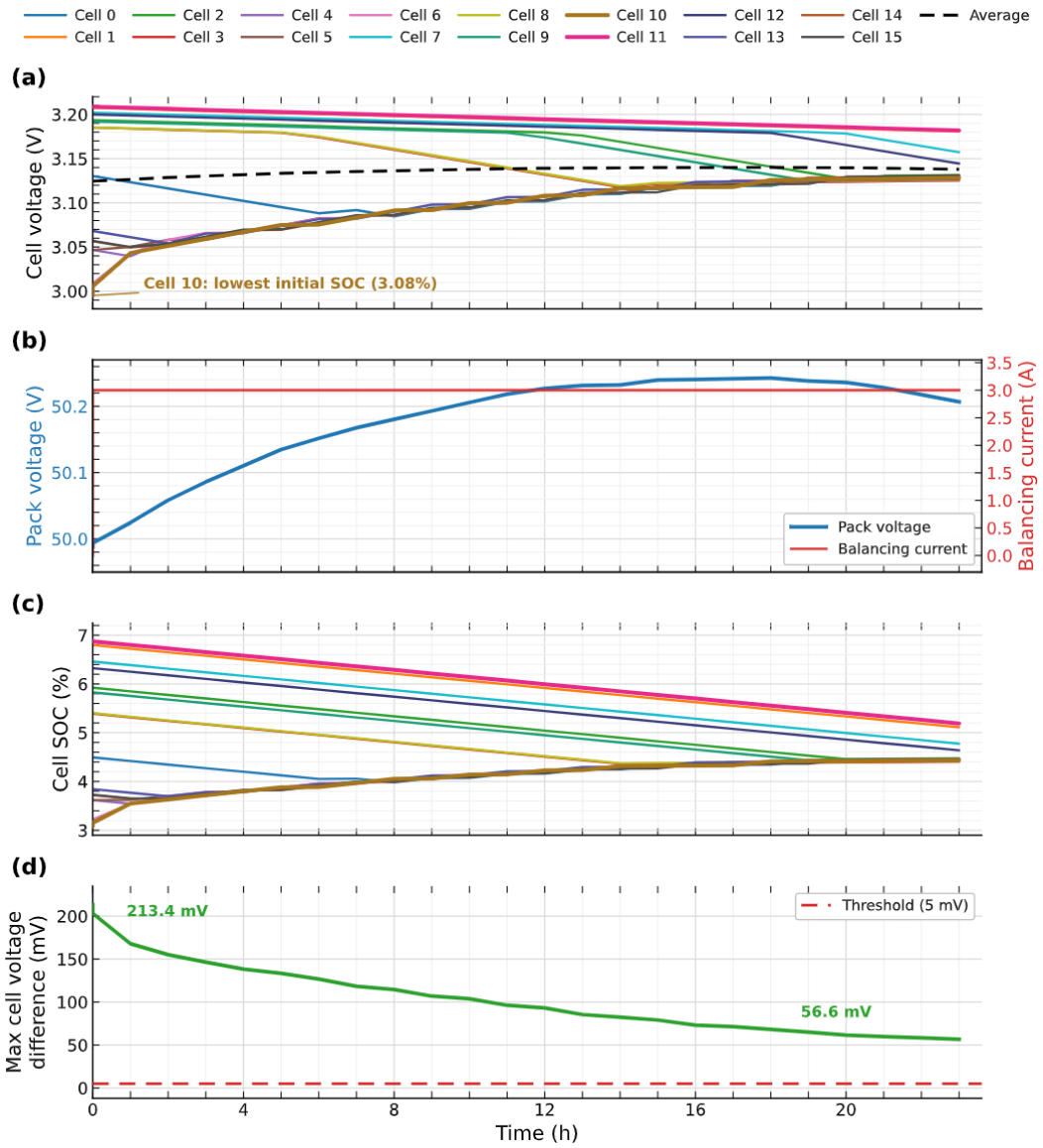


Figure 8. Voltage and SOC evolution during the 24 h balancing process in the low-SOC scenario: (**a**) voltage variation in the 16 cells (SOC = 5% ± 2%, 24 h balancing, including pack efficiency); (**b**) pack voltage and balancing current; (**c**) SOC variation in each cell (considering pack efficiency: charging 80%, discharging 65%); (**d**) maximum voltage difference between cells.

3.3. Comparative Analysis of the Two Scenarios

Combining the simulation results of the two scenarios, the following conclusions can be drawn:

(1) Voltage convergence performance: In the high-SOC scenario, the voltage difference converges significantly from 94.46 mV to 4.73 mV, a convergence rate of 95%, and the voltage deviation can converge to within the 5 mV threshold within 24 h. In the low-SOC scenario, affected by the voltage plateau characteristics, the voltage convergence speed is slower, and a residual voltage difference of 56 mV remains after 24 h, requiring a longer equalization time or the introduction of an SOC-domain equalization criterion for further convergence.

(2) SOC consistency: In the low-SOC scenario, the SOC deviation converges to 0.6%, better than the 0.8% in the high-SOC scenario, indicating that the strategy dominated by charging equalization is more effective in aligning SOC. In the high-SOC scenario,

although discharging equalization can recover energy, the SOC convergence effect is slightly inferior owing to the limited DC/DC conversion efficiency.

(3) Energy efficiency: The pack SOC loss in the high-SOC scenario is 1.14%, lower than the 1.76% in the low-SOC scenario. This is because the high-SOC scenario includes a discharging equalization stage in which part of the energy is fed back to the pack, whereas the low-SOC scenario only performs charging equalization with one-way energy outflow, resulting in a greater loss. The energy losses of both scenarios are within the acceptable range for engineering.

(4) Safety: The high-SOC scenario effectively prevents the overcharging risk, and the low-SOC scenario effectively avoids deep discharge; no cell enters the dangerous region in either scenario, verifying the safety guarantee capability of the scenario-adaptive strategy.

(5) Hardware measurement support: To further improve the credibility of the simulation conclusions, comparative experiments on three typical active equalization topologies—transformer, capacitor, and inductor—were carried out based on the hardware platform of this study, and the results are shown in Figure 9. The initial maximum voltage difference in all three experiments was approximately 260 mV. In the measurements, the transformer-based equalization circuit converged the maximum voltage difference of the 16 cells from about 260 mV to 10 mV within about 18 h, with a fast equalization speed and sufficient convergence; the capacitor-based balancing circuit still failed to fully converge after 54 h of operation, with the maximum voltage difference remaining at approximately 50 mV; and the inductor-based equalization circuit could not achieve convergence after 66 h of operation. The measurement results verify the engineering feasibility of the transformer-based equalization topology selected in this paper and provide hardware application test data support for the aforementioned simulation analysis. In terms of implementation cost, owing to the multi-winding transformer and the switch array, the circuit cost of the transformer-based solution is approximately 100–200% higher than that of the capacitor- and inductor-based counterparts; this premium is regarded as acceptable for large-capacity energy storage applications, in which balancing speed, convergence accuracy, and energy recovery capability dominate.

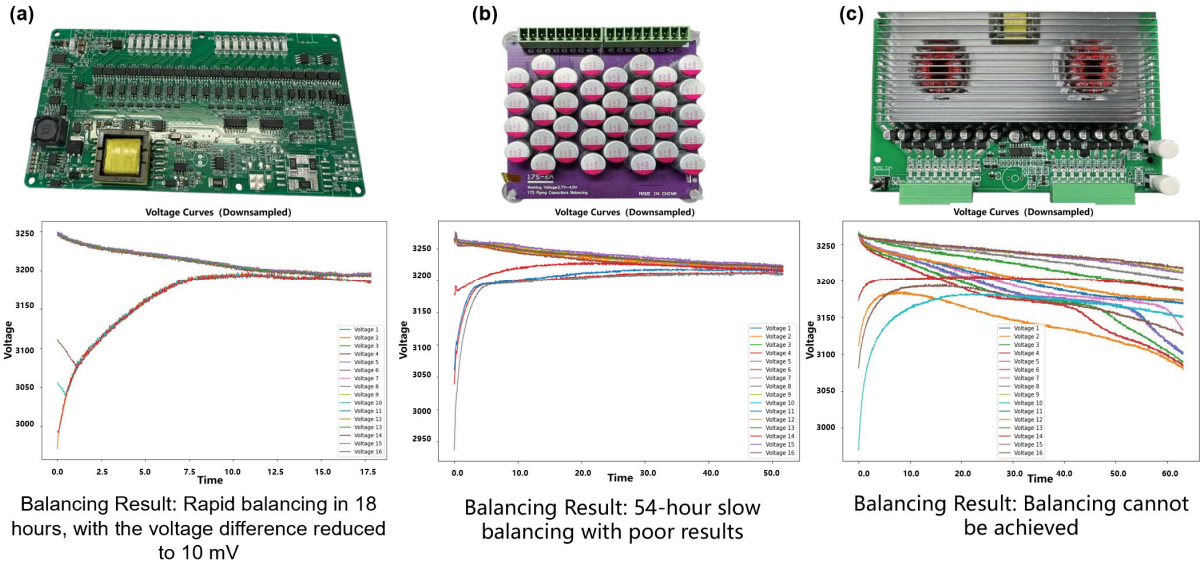


Figure 9. (**a**) Transformer equalization circuit and diagram showing its equalization effect; (**b**) capacitor equalization circuit and diagram showing its equalization effect; (**c**) inductor equalization circuit and diagram showing its equalization effect.

To clearly define the application advantages of the proposed strategy, the proposed method is compared with existing typical equalization strategies in five dimensions—trigger basis, energy flow direction, applicable scenario, safety, and energy consumption control—as shown in Table 6.

Table 6. Mechanism comparison between the proposed strategy and existing typical equalization strategies.

Dimension	Fixed-Threshold Equalization	Top/Bottom Equalization	SOC-Based Equalization	Proposed Strategy
Trigger basis	Cell voltage compared with a fixed threshold	Only acts on the highest/lowest voltage cells	Based on SOC deviation calculation	Dual criterion of voltage deviation and scenario SOC interval
Energy flow	One-way (resistor dissipation)	One-way (only top/bottom action)	Bidirectional transfer by SOC deviation	Bidirectional; charge first then discharge; pack energy closed loop
Applicable scenario	General, no scenario differentiation	Specific idle/end-of-charging conditions	Dynamic operating conditions	Adaptive switching for full-charge/full-discharge idle scenarios
Over-charge/overdis-charge risk	High	Medium	Medium	Low
Energy consumption control	Poor	Medium	Medium	Good

3.4. Robustness Validation of the Balancing Strategy

To demonstrate that balancing is still achieved when conditions deviate from the ideal case, the investigation proceeds from two aspects, namely the magnitude of the initial imbalance and variations in internal resistance and capacity; in addition, hardware experiments are conducted on eight modules with unknown combined SOC, resistance, and capacity imbalances to verify the effectiveness of the strategy.

(1) Influence of the initial imbalance magnitude

To examine whether the strategy converges over a wider range of initial imbalances, the 16 initial cell SOCs are drawn from uniform distributions of ±1%, ±2%, ±3%, and ±4% around a 5% base SOC, with three random draws per level; the cell capacity is 320 Ah, together with the model, the balancing current of 3 A, the 5 mV threshold, and the 300 s step size. The resulting initial SOC spreads are 1.8–1.9, 3.7–3.8, 5.5–5.7, and 7.3–7.6 percentage points; in the low-SOC region, where the OCV slope is about 96 mV per percentage point of SOC, they correspond to initial voltage spreads of 98–427 mV.

As can be seen from the results in Table 7, one balancing step of 3 A for 300 s changes the cell SOC by 0.078 percentage points, which corresponds to about 7.5 mV in the low-SOC region and therefore exceeds the 5 mV threshold; convergence in this region is thus reported in terms of the SOC spread. The time needed to reduce the SOC spread below 1 percentage point increases with the charge to be redistributed, which ranges from 24 Ah to 126 Ah: 4.0–5.5 h at ±1%, 17–20 h at ±2%, and beyond 24 h at ±3% and ±4%. The residual spread after 24 h is at most 0.70 percentage points for the ±1–2% levels. In the high-SOC region, where one step corresponds to only about 2.0 mV, the strategy reduces an initial spread of 94.46 mV below the 5 mV threshold within 17 h.

Table 7. Sweep results for 16-cell initial spreads.

Nominal Spread	Initial SOC Spread, pp	Initial Voltage Spread, mV	Charge to Redistribute, Ah	Time to Spread <1 pp, h	Residual Spread After 24 h, pp
±1%	1.82–1.90	98–107	24–31	4.0–5.5	0.12–0.13
±2%	3.65–3.80	197–214	49–63	17.2–20.2	0.56–0.70
±3%	5.47–5.70	295–320	73–94	>24	1.61–2.07
±4%	7.30–7.59	393–427	98–126	>24	2.85–3.62
±1%	1.82–1.90	98–107	24–31	4.0–5.5	0.12–0.13
±2%	3.65–3.80	197–214	49–63	17.2–20.2	0.56–0.70
±3%	5.47–5.70	295–320	73–94	>24	1.61–2.07

(2) Influence of resistance and capacity variations

To verify that the strategy responds only to SOC imbalance and does not act erroneously on resistance or capacity variations, resistance mismatches of 1.5× and 2.0× and capacity mismatches of −5% and +5% are introduced in simulation, and hardware experiments are conducted on a 16S/280 Ah LFP module connected to an active balancing unit based on a flyback converter, with a balancing current of 2 A, a cell-voltage limit of 3.6 V, a converter efficiency of about 70%, and a cell-voltage sampling accuracy of ±10 mV; SOC-, resistance-, and capacity-mismatch conditions are constructed respectively.

As can be seen from the simulated and measured comparison in Table 8, a pure resistance mismatch does not satisfy the balancing criterion during idle periods and therefore triggers no balancing action, and the resulting capacity and energy deviations are small and reversible. Enabling balancing in the capacity-mismatch case raised the measured capacity by only 1.51 Ah, i.e., 0.54%, indicating that capacity imbalance cannot be corrected by charge transfer. In contrast, a voltage-extreme threshold strategy repeatedly balanced a high-resistance cell in both directions for 10 days, discharging 127.2 Ah and charging 126.2 Ah, without any improvement in the SOC imbalance, which highlights the discrimination capability of the proposed strategy.

Table 8. Simulated and measured results of the three mismatch experiments.

Scenario	Metric	Simulated	Measured	Deviation
SOC mismatch, after balancing	Capacity	278.77 Ah	281.73 Ah	1.05%
	Energy per cell	908.31 Wh	920.52 Wh	1.33%
Resistance mismatch 1.5×	Capacity	277.32 Ah	280.67 Ah	1.51%
	Energy per cell	892.58 Wh	921.90 Wh	1.72%
Capacity mismatch, balancing off	Capacity	279.96 Ah	281.23 Ah	0.45%
Capacity mismatch, balancing on	Capacity	283.28 Ah	282.74 Ah	−0.19%

(3) Verification of the balancing performance under compounded unknown influences

Finally, the accuracy of the diagnosis, balancing, and re-verification procedure is validated under compounded unknown imbalances in practice. Closed-loop experiments are conducted on eight 16S/280 Ah modules with unknown combined SOC, resistance, and capacity imbalances; the imbalance sources are diagnosed from the measured pack current and cell voltages alone, the required balancing charge is predicted, and the capacity and energy are re-measured after balancing.

As can be seen from the results in Table 9, the deviations between the predicted and measured capacity and energy of the eight modules are all within 5%, with a maximum of 4.10%, indicating that the diagnosis and balancing procedure remains accurate under compounded imbalance conditions.

Table 9. Closed-loop validation results of the eight modules.

Module	Orig. Cap. Ah	Orig. Energy Wh	Pred. Cap. Ah	Pred. Energy Wh	Meas. Cap. Ah	Meas. Energy Wh	Cap. Dev.	Energy Dev.
1	202.58	660.00	273.41	887.73	283.32	911.05	3.50%	2.56%
2	208.71	680.39	269.93	876.90	270.75	879.55	0.30%	0.30%
3	204.86	666.56	270.16	876.48	276.82	898.96	2.40%	2.50%
4	206.61	672.65	269.86	875.66	270.06	877.34	0.08%	0.19%
5	193.93	630.49	267.36	867.99	278.76	905.06	4.09%	4.10%
6	221.54	721.12	260.97	847.50	272.04	883.25	4.07%	4.05%
7	197.34	642.64	272.64	884.93	267.87	870.47	−1.78%	−1.66%
8	202.13	657.51	271.29	880.78	277.94	902.63	2.39%	2.42%

4. Discussion

4.1. Significance of the Phased and Scenario-Adaptive Design

The simulation results in Section 3 confirm that the proposed strategy can effectively handle the two most typical idle scenarios of energy storage battery packs. In the high-SOC scenario, the voltage difference converged from 94.46 mV to 4.73 mV (a 95% convergence) within 24 h, while the pack SOC loss was limited to 1.14%, indicating that the "charge first, then discharge" ordering combined with the pack energy closed-loop principle can achieve voltage convergence at an acceptable energy cost. In the low-SOC scenario, although the voltage convergence was slower (a residual difference of 56 mV), the SOC deviation was controlled within 0.6%, which is the key indicator for preventing deep discharge of individual cells. The complementary advantages of the two scenarios demonstrate the necessity of the scenario-adaptive design: a single fixed-threshold strategy cannot simultaneously achieve fast voltage convergence and deep-discharge prevention in both regions because of the nonlinear OCV–SOC relationship of LFP cells. Regarding the balancing duration, the 18 h balancing shown in Figure 9 results from the initial voltage deviation being set excessively large; in practical engineering, such a long balancing time is not necessarily required. Moreover, the strategy is not restricted to idle conditions in principle. When permitted, balancing can also proceed during operating periods, and the effective convergence speed can be further improved by increasing the single-cell equalization current.

4.2. Comparison with Existing Strategies

As summarized in Table 3, compared with fixed-threshold equalization, the proposed strategy introduces scenario awareness and adaptively switches between charging-dominant and discharge-assisted modes; compared with top/bottom equalization, it covers both full-charge and full-discharge idle states with complete energy closed-loop management; compared with pure SOC-based equalization, it reduces the dependence on the accuracy of SOC estimation by using a voltage-domain criterion with multi-sampling confirmation, while still effectively aligning SOC. The measured comparison of the three topologies (Figure 9) further supports the selection of the transformer-based topology: it achieved convergence in about 18 h, whereas the capacitor-based and inductor-based topologies failed to converge within 54 h and 66 h, respectively. This is consistent with the higher

energy transfer capability of transformer-based equalization and explains why it was chosen as the hardware foundation of this study.

4.3. Limitations and Future Work

Several limitations should be acknowledged. First, the voltage convergence in the low-SOC scenario is relatively slow, and the residual voltage difference of 56 mV requires either a longer equalization time or an SOC-domain criterion. Second, the current strategy does not yet incorporate long-term cell aging information; the equalization decisions are based only on voltage and SOC, and the capacity inconsistency caused by different aging rates is not explicitly considered. In addition, the scenario-level analyses in Sections 3.1 and 3.2 are based solely on simulation; only the topology comparison was verified on a hardware balancing test platform, while long-term real closed-loop operation integrated with a complete commercial BMS remains to be verified. Future work will focus on: (i) optimizing the low-SOC strategy by increasing the discharging equalization proportion when the voltage difference permits, so as to reduce pack energy loss; (ii) introducing a long-cycle equalization strategy based on the state of health (SOH) to include cell aging factors in equalization decisions; and (iii) conducting hardware-in-the-loop tests in an actual BMS to verify the robustness and real-time performance of the algorithm under real operating conditions.

5. Conclusions

Based on the 16S switch-array active equalization hardware and a high-precision simulation model, this paper proposes and validates a dynamically controlled equalization strategy. The main conclusions are as follows:

(1) The proposed "phased, scenario-adaptive" equalization strategy achieves efficient voltage and SOC convergence through the three constraints of forced ordering, energy closed-loop management, and interlocking. The analysis of the single-cell charging and discharging characteristics reveals a law: charging equalization is efficient in the low-SOC region and discharging equalization has a faster voltage response in the high-SOC region, providing a theoretical basis for the scenario-differentiated strategy. The special treatment of the high-/low-SOC scenarios enhances the adaptability and safety of the strategy: the voltage difference converges by more than 95% in the high-SOC scenario.

(2) The simulation cases show that the strategy can reduce the voltage difference from 94.46 mV to 4.73 mV within 24 h in the high-SOC scenario, with a pack SOC loss of only about 1.14%; in the low-SOC scenario, the SOC consistency is significantly improved, with the deviation converging to 0.6%, effectively avoiding deep discharge of individual cells, although the pack SOC loss is 1.76% and there is room for further improvement in the voltage convergence speed and energy efficiency. In both scenarios, no cell enters the dangerous region during the balancing process, verifying the safety guarantee capability of the strategy.

This study provides a complete theoretical framework, a hardware model, and validation examples for the algorithm development of active equalization systems for lithium-ion battery packs. Future work can focus on optimizing the low-SOC strategy, introducing long-cycle equalization based on SOH, and hardware-in-the-loop testing in actual BMSs.

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Abbreviations

The following abbreviations are used in this manuscript:

BMS	Battery Management System
CC/CV	Constant Current/Constant Voltage
DC/DC	Direct Current to Direct Current
LFP	Lithium Iron Phosphate
OCV	Open-Circuit Voltage
SOC	State of Charge
SOH	State of Health

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