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An Adaptive Bi-Band Doherty PA with Main-Peak Amplifier Swapping and Extended Bandwidth Performance

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Abstract

This paper presents the design, implementation, and characterization of a broadband power amplifier (PA) with a reconfigurable architecture, capable of efficient operation across a wide frequency range of 0.2–3.6 GHz. Leveraging Gallium Nitride (GaN) devices, the PA achieves high efficiency and power, essential for broadband and high-frequency applications. By swapping the roles of the main and peak amplifiers, the PA achieves Doherty behavior at two related frequencies, 1.4 and 2.8 GHz, where the first is exactly half of the second, while maintaining consistent efficiency and output power across the remaining band in non-Doherty modes. Characterization results confirm the reliability and versatility of the proposed design, showcasing its ability to deliver robust performance across both Doherty and non-Doherty operational ranges. This combination of GaN technology and innovative reconfigurability makes the PA highly suitable for broadband applications requiring high efficiency, flexibility, and wideband coverage. Moreover, the simplicity of the proposed design makes it not only practical for implementation but also highly competitive among state-of-the-art solutions.

Keywords: power combining; Doherty; power amplifiers; GaN; GaAs; millimeter-wave

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1. Introduction

Broadband power amplifiers (PAs) are crucial components in modern wireless communication systems, where efficiency and adaptability across wide frequency ranges are of paramount importance. Traditional PA architectures, including the Doherty Power Amplifier (DPA), have demonstrated remarkable performance in specific frequency bands, but their operation is often limited by narrowband design constraints [1–13].

The design of broadband and efficient DPAs has become a central focus in RF power amplifier research, particularly for 5G and future wireless communication systems. One innovative approach introduces a shunt $\lambda/2$ microstrip line at the combiner of a traditional DPA, enabling wideband impedance transformation for the carrier amplifier. This technique enhances both bandwidth and back-off efficiency, achieving saturated output powers above 43 dBm and drain efficiencies between 65% and 72% across 3.1–3.7 GHz [2]. Similarly, a wideband class AB-C DPA design addresses the non-ideal output impedance of the auxiliary amplifier due to parasitic effects. By optimizing the output matching network, this design achieves a 25% fractional bandwidth (2.8–3.6 GHz), with saturated drain efficiencies up to 76.5% and strong linear gain performance [6].

Beyond traditional DPA architectures, alternative load modulation strategies have emerged to overcome inherent bandwidth limitations. The pseudo-Doherty Load-

Modulated Balanced Amplifier (PD-LMBA) introduces a novel configuration that decouples the carrier and peaking amplifiers, enabling optimal load modulation with a static phase offset. This architecture achieves high efficiency (up to 72%) over a wide frequency range (1.5–2.7 GHz) and maintains 47–61% efficiency under modulated signals [5]. Complementing this, a simplified design methodology for broadband DPAs leverages linear simulations to estimate bandwidth and uses the device's output capacitance to guide the Doherty combiner design. A GaN-based prototype using this method demonstrated an 87% bandwidth (1.5–3.8 GHz), with 6 dB back-off efficiencies between 33% and 55%, and confirmed linearizability under modulated signals [14].

This work focuses on the design, implementation, and characterization of a broadband PA that overcomes traditional limitations by incorporating a reconfigurable amplifier configuration and leveraging advanced Gallium Nitride (GaN) devices [14–21]. The proposed architecture allows the roles of the main and peak amplifiers to be interchanged, enabling the PA to achieve Doherty-like behavior at two harmonically related frequencies, 1.4 and 2.8 GHz, while maintaining consistent efficiency and output power across the broader 0.2–3.6 GHz range. These configurations optimize performance at targeted frequency bands and ensure reliable operation outside Doherty modes, effectively addressing challenges associated with broadband operation and delivering robust performance across varying conditions. Table 1 compares this work with several state-of-the-art DPAs, demonstrating that the proposed approach is competitive.

Table 1. Comparison with State-of-the-Art DPAs.

Ref	[14]	[2]	[5]	[6]	This Work
BW (GHz)	1.5–3.8	3.1–3.7	1.5–2.7	2.8–3.6	0.2–3.6
$DE_{@OBO}$ (%)	33–55 @6 dB	40–45 @8 dB	47–61 @6 dB	44–56 @6 dB	30–44 @6 dB
DE_{sat} (%)	42–63	65–72	58–72	62–76.5	41–72
P_{OUT} (dBm)	42.3–43.4	43.13–44.65	43	43–44.2	41–44.5
S. Gain (dB)	10–13.8	9–9.5	6–11	8–13.5	8–14

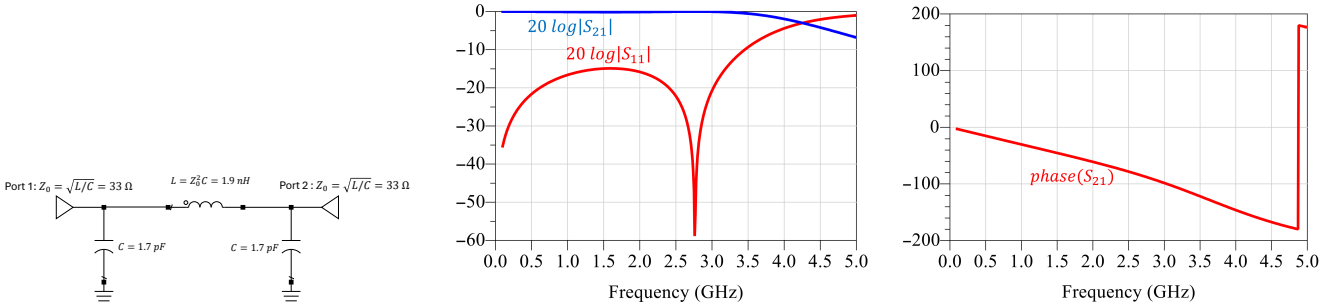
2. Design

2.1. Transmission Line Equivalence and Impedance Inversion

Let us consider the Capacitance-Inductance-Capacitance (CLC) low-pass network shown in Figure 1a, where a series inductor is placed between two shunt capacitors. This network behaves as an impedance inverter at a frequency $\omega_0 = 1/\sqrt{(LC)}$. In addition, it exhibits characteristics similar to a transmission line with characteristic impedance $Z_0 = \sqrt{L/C}$, over a range of frequencies up to $\omega_0/(2\pi)$ GHz and beyond, due to the gentle slope near the cutoff frequency. To demonstrate this behavior, Figure 1b illustrates S_{11} and S_{21} for a low-pass CLC network with capacitors of 1.7 pF and $Z_0 = 33\ \Omega$, which means an inductor of 1.9 nH. In this case $f_0 = \omega_0/(2\pi) = 2.8$ GHz, it means a perfect matching at that frequency, as demonstrated by the sharp drop in S_{11} in Figure 1b. The phase of S_{21} is presented in Figure 1c, where a $-90°$ response is obtained at 2.8 GHz.

Thus, the proposed CLC network, shown in Figure 1a, can emulate a 33 Ω transmission line. When terminated with the same 33 Ω, it achieves quasi-complete impedance matching with an input impedance of 33 Ω. Notably, this 33 Ω termination can be realized within a 50 Ω system by employing a real-to-real impedance transformation across an arbitrary bandwidth (with an arbitrary number of sections), valid for the frequency band from 0 to beyond ω_0. Furthermore, assuming the capacitor C represents the typical output capacitance of a FET, this low-pass filter emerges as a compelling choice for achieving broadband matching, paving the way for the design of a broadband power amplifier.

In this framework, as anticipated, cascading the CLC network with an identical copy results in a 180 ° (at ω_0) equivalent transmission line with a characteristic impedance of 33 Ω. This approach can be effectively utilized to extend the equivalent length of the transmission line.



(**a**) CLC network (**b**) Magnitudes of S_{11} and S_{21}. (**c**) Phase of S_{21}

Figure 1. A CLC network which mimics a transmission line up to beyond ω_0, with $Z_0 = 25\ \Omega$.

2.2. Utilizing the Equivalent Reactive Output Network of FETs to Emulate a Low-Pass CLC Network

As discussed in the literature [10,14,17,20], the equivalent output network of a FET is typically modeled as a shunt capacitor and a series inductor, referred to as C_O and L_O, respectively. These components can be employed to synthesize the CLC network illustrated in Figure 1a by incorporating an additional series inductor L_x and a subsequent shunt capacitor with a value of C_O. The inductance L_x can be calculated using the following formula:

$$L_x = {Z_0}^2 C_O - L_O \tag{1}$$

Ensure that the value of L_x remains positive by appropriately selecting the frequency ω_0. Notice that $L = {Z_0}^2 C_O$.

For implementation purposes, it is crucial to account for the challenges associated with incorporating lumped components, particularly when they must be directly connected to a transistor. Therefore, it becomes necessary to identify a distributed equivalent to replicate the effects of L_x and C_O beyond the drain pin of the transistor. Thus, the proposed distributed network considers a series transmission line followed by an open shunt transmission line, as will be shown later.

2.3. DPA Architecture Based on CLC Networks

Figure 2 illustrates the proposed Doherty Power Amplifier (DPA) combiner architecture based on the CLC network. The CLC network described in the previous section serves as the foundational element for the proposed Doherty Power Amplifier (DPA) architecture. In this configuration, the output matching network of the main amplifier branch is implemented using a single CLC section, effectively emulating a 90° (impedance inverter) transmission line with a characteristic impedance of Z_0 = 33 Ω. To achieve the necessary phase alignment and impedance transformation required for Doherty operation, the peak amplifier branch incorporates two cascaded CLC sections, thereby doubling the electrical length relative to the main path. This arrangement ensures a 90° phase shift between the main and peak paths at the chosen frequency, enabling proper load modulation and power combining. The outputs of both branches are combined at a common node and delivered to a transformed load impedance of $Z_0/2$, consistent with Doherty operation principles. This impedance transformation ensures that the final 50 Ω system load is appropriately matched to the combiner.

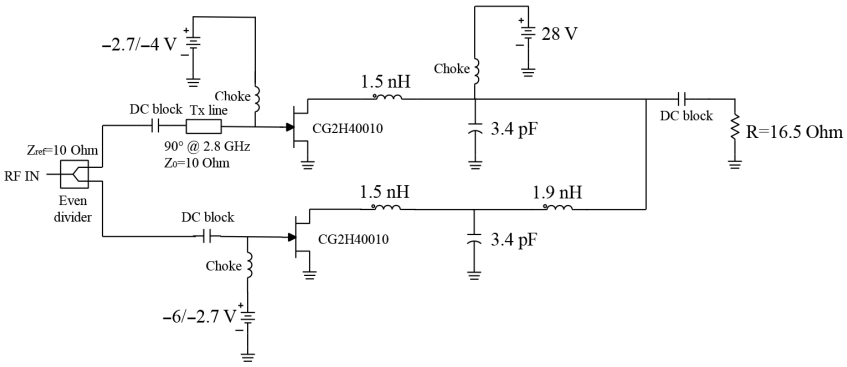


Figure 2. Lumped components DPA combiner structure.

In this case, the selected device for both the main and peak amplifiers is the CG2H40010. Consequently, the reactive output equivalent network is modeled with a capacitance of C_O = 1.7 pF and an inductance of L_O = 0.4 nH. The optimal impedance for this device is considered in this case of 33 Ω, while the selected frequency is 2.8 GHz. As shown in Figure 2, an inductor L_x = 1.5 nH is connected directly to the drain pin of the device, forming a total inductance of 1.9 nH for the CLC network, as illustrated in Figure 1a. Following this, a 1.7 pF capacitor is shunted to complete the CLC network.

Note that in Figure 2, a 3.4 pF capacitor is depicted. This value represents the parallel combination of two 1.7 pF capacitors—one from the upper branch and the other from the lower branch. It is important to highlight that in the peak branch, the CLC network is synthesized twice to achieve the 180° phase shift required for the peak output.

In Figure 2, the gate bias voltages are indicated for each operating mode. For the frequency band from 0.2 to 1.5 GHz, the upper (peak) device is biased at −4 V, while the lower (main) device is biased at −2.7 V. For the band from 1.5 to 3.2 GHz, the upper device is biased at −2.7 V (main) and the lower one at −6 V (peak). These values were intentionally optimized to achieve the best DPA performance using the proposed configuration.

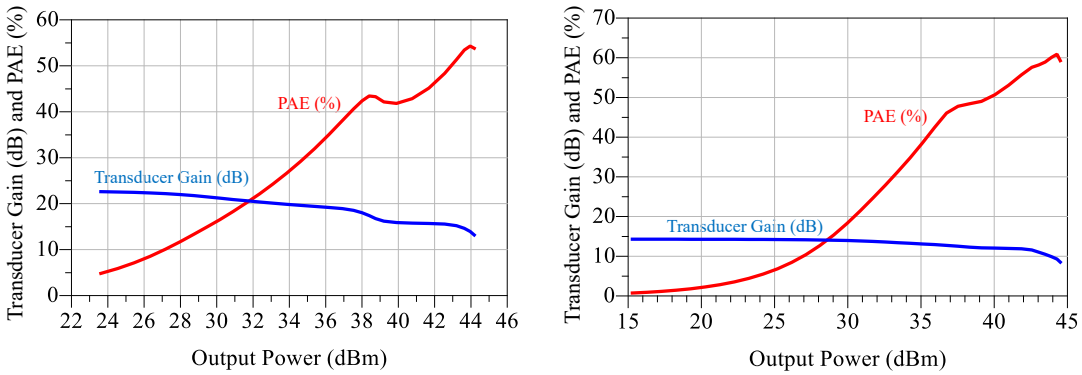
To achieve adequate input matching for both amplifiers in this preliminary design, a 10 Ω reference impedance has been adopted, as shown in Figure 2. A 10 Ω 90° transmission line is implemented in the main branch to adjust the current phase, ensuring proper signal combining at the output. An ideal even power divider with a 10 Ω reference impedance is also employed. In practice, using an even division ratio contributes to improved bandwidth performance [14].

Figure 3b presents the PAE and transducer gain profiles obtained for the proposed DPA structure at 2.8 GHz. As shown, a characteristic DPA performance is achieved. When the main and peak amplifiers are swapped and the simulation is repeated at 1.4 GHz, DPA profiles for both PAE and transducer gain are again observed, as illustrated in Figure 3a. This behavior is attributed to the 180° equivalent transmission line at 2.8 GHz in the lower branch, which becomes equivalent to a 90° transmission line at 1.4 GHz.

In the upper branch, the combiner structure introduces a 45° equivalent transmission line at 1.4 GHz, resulting in an imaginary impedance component for the lower amplifier at back-off. However, as seen in Figure 3a, this imaginary component does not degrade the efficiency profile, since the resulting impedance remains within the high-efficiency region. These results demonstrate the effectiveness of the proposed combiner in achieving bi-band DPA performance.

Additionally, some chokes are used as part of the bias circuit to eliminate the effects of the bias-tees on the PA's bandwidth behavior. As can be observed, when both devices operate at maximum power, the load seen by each device is closely the optimal 33 Ω over the CLC network bandwidth. This characteristic of the combiner ensures broadband performance of the PA. Consequently, the design not only achieves a bi-band DPA but also

functions as a broadband amplifier. Specifically, DPA behavior is observed near 1.4 and 2.8 GHz, while a combined PA behavior is exhibited outside these frequencies. The expected bandwidth of the PA extends from 0 to 3.5 GHz, which corresponds to the bandwidth of the CLC network.



(**a**) 1.4 GHz (**b**) 2.8 GHz

Figure 3. CW simulation of the DPA using the proposed Lumped components combiner.

3. Implementation and Characterization

As mentioned earlier, it is necessary to transform the lumped components obtained from the CLC network into distributed elements, which are easier to implement on a typical substrate. In this case, the RF-35 Taconic substrate, with a relative dielectric constant of 3.5 and h = 0.76 mm, is used. A straightforward methodology is applied: each series inductor, together with a shunt capacitor, is replaced by a series transmission line and a shunt open-terminated transmission line, as shown in Figure 4. The widths and lengths of the transmission lines are tuned to replicate the response of the original lumped component network. Additionally, the chokes are implemented using high-value inductors, as illustrated in Figure 5. Note that the tail-like structure at the output of the circuit shown in the figure is a six-section transformer, designed to convert the 50 Ω system reference impedance to the 16.5 Ω required as the common load for the DPA.

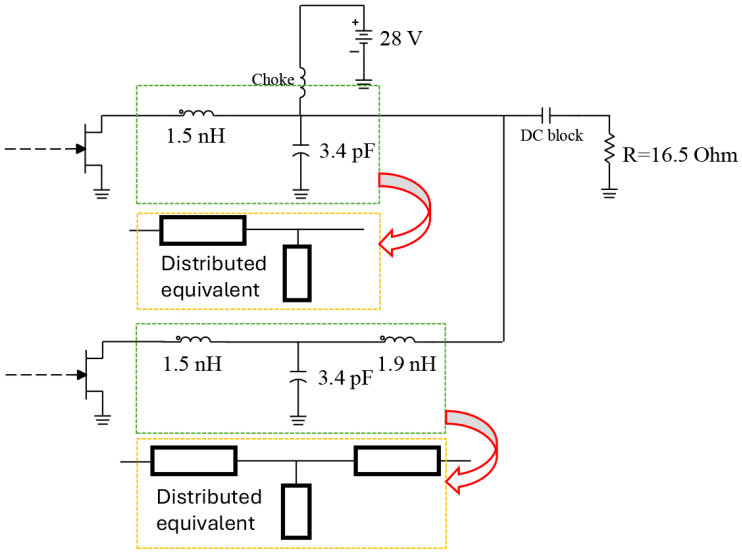


Figure 4. Lumped to distributed components transformation.

The input matching network shown in Figure 2 is redesigned to have a 50 Ω reference. Additionally, a stabilization network is included, which is always necessary when working with this type of device.

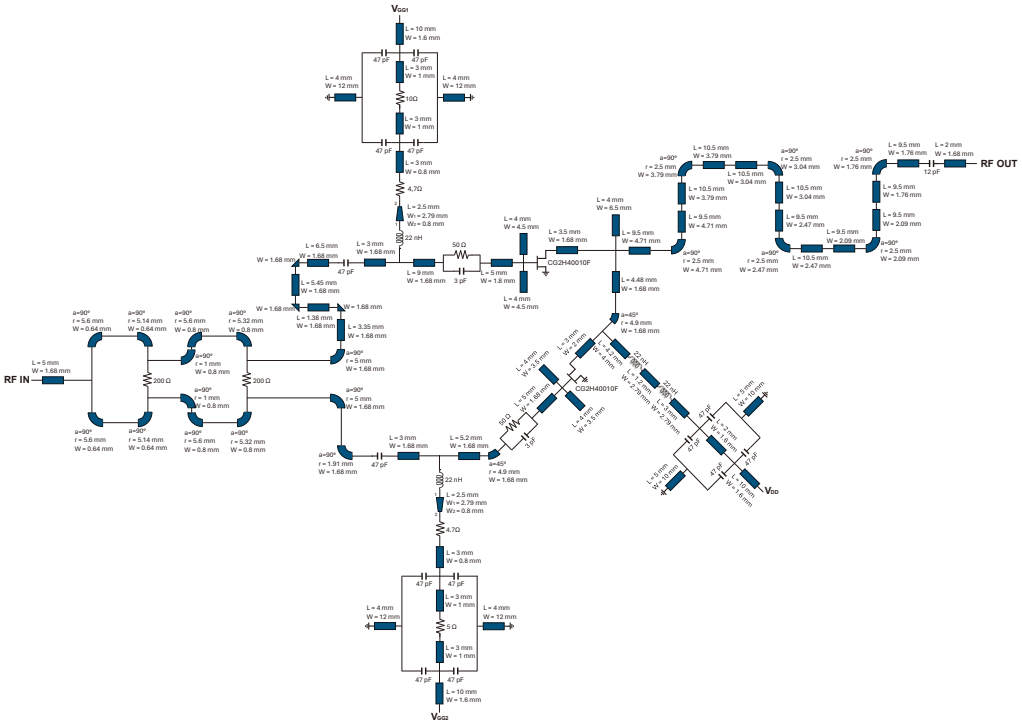
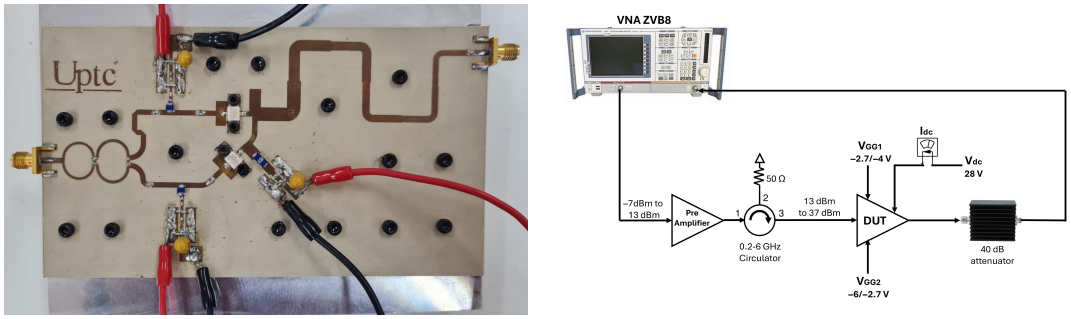


Figure 5. Schematic of the implemented DPA.

The complete schematic of the designed DPA is shown in Figure 5. This schematic was implemented, and a photograph of the fabricated circuit is also presented in Figure 6, along with a block diagram of the measurement setup. A continuous wave (CW) characterization was carried out. For the first band (0.2–1.5 GHz), the saturated transducer gain ranged from 8 to 14 dB, while the output power was between 41 and 44 dBm. The drain efficiency at 6 dB output back-off (OBO) ranged from 31% to 42%, and at saturation, it ranged from 60% to 72%. In the second band (1.5–3.5 GHz), where the main and peak amplifiers are swapped, the saturated transducer gain was between 8 and 10 dB, and the output power again ranged from 41 to 44 dBm. The drain efficiency at 6 dB OBO ranged from 30% to 42%, while at saturation it ranged from 42% to 52%. Some measured efficiency and gain profiles are presented in Figure 7. The results, including saturated output power, saturated gain, saturated drain efficiency, and drain efficiency at 6 dB of output back-off, are presented in Figure 8, alongside comparative simulation data.

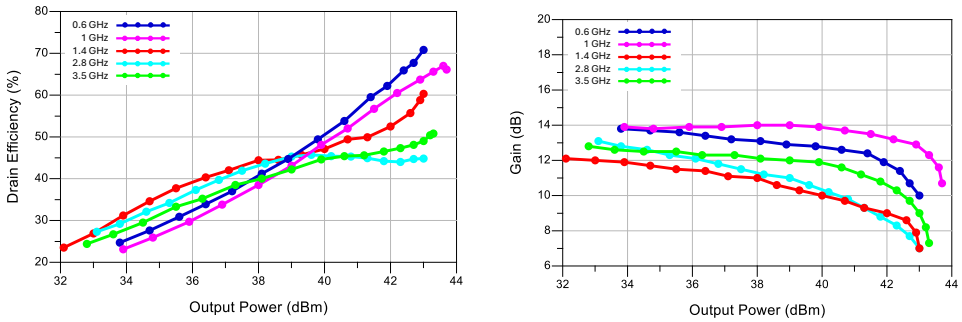


(**a**) Photo of the designed DPA. (**b**) Measurement Setup.

Figure 6. Photo of the circuit and setup measurement.

The system performance of the design was evaluated using the Keysight ADS 2025 DPD Explorer simulation tool, employing a Generalized Memory Polynomial (GMP) model with a memory depth of 3 and an order of 7. This model is robust across wideband signals,

ensuring effective linearization even under bandwidth expansion [22]. The simulation involved two 100 MHz 5G NR signals with carrier frequencies of 1 and 3 GHz, a Peak-to-Average Power Ratio (PAPR) of 9 dB, and an average available power of 24 dBm.



(**a**) Some efficiency profiles (**b**) Some gain profiles

Figure 7. Measured efficiency and gain profiles.

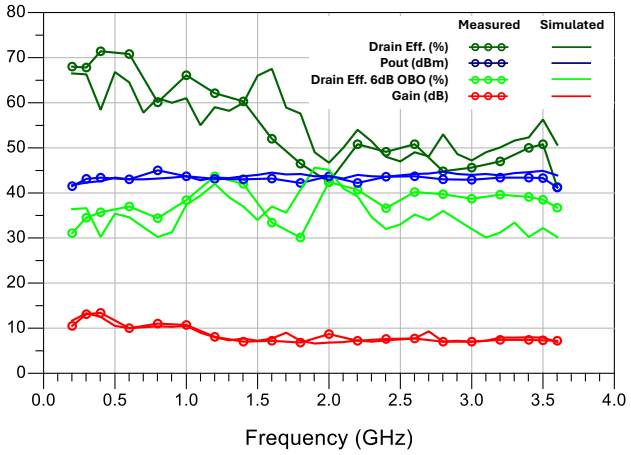


Figure 8. CW characterization of DPA over the band.

As shown in Figure 9, the results compare the power spectral density of the PA output with and without the application of Digital Predistortion (DPD). The application of DPD significantly improved the Adjacent Channel Leakage Ratio (ACLR), increasing it from 32.3 to 46.6 dBc at 1 GHz, and from 29.2 to 50.1 dBc at 3 GHz. Similarly, the Error Vector Magnitude (EVM) improved from −26.38 to −47.32 dB at 1 GHz, and from −22.42 to −46.5 dB at 3 GHz. The average simulated output power was 36 dBm for 1 GHz and 35 dBm for 3 GHz, with a PAE averaging approximately 33% and 30% respectively.

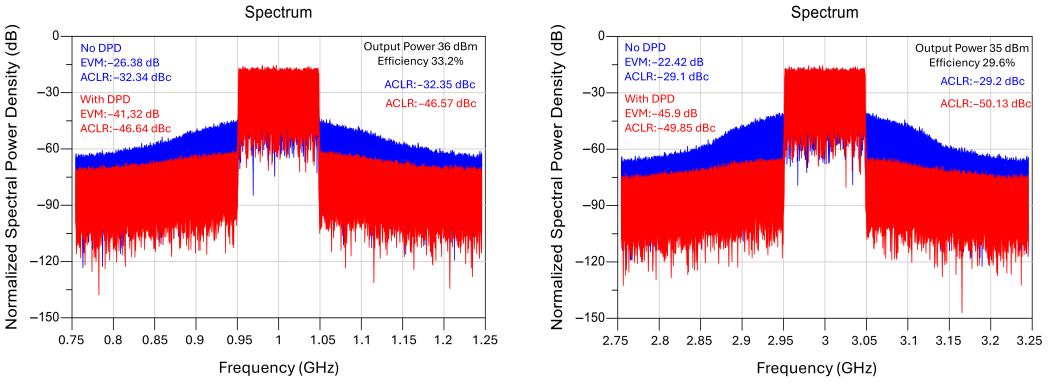


Figure 9. Normalized output power spectral density of the designed PA at 1 GHz and 3 GHz carrier frequency, with and without DPD.

4. Conclusions

This work has introduced a reconfigurable broadband power amplifier architecture that effectively combines the benefits of Doherty operation with the flexibility of wideband performance. By strategically swapping the roles of the main and peak amplifiers, the design achieves efficient Doherty behavior at two harmonically related frequencies while maintaining consistent performance across the entire 0.2–3.6 GHz range. The use of GaN technology further enhances the amplifier's power and efficiency, making it well-suited for demanding broadband applications. Experimental results validate the robustness and adaptability of the proposed solution. Most notably, the simplicity of the architecture not only facilitates practical implementation but also positions it as a highly competitive alternative among state-of-the-art designs.

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