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Design of a 2–4 Decoder Based on All-Spin Logic and Magnetic Tunnel Junction

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Abstract: A 2–4 decoder based on all-spin logic (ASL) and magnetic tunnel junction (MTJ) is proposed. The decoder employs five-input minority gates to realize three-input NOR gates, which reduces the circuit size compared to the three-input minority gates. Simultaneously, the inputs of the original and reverse variables are implemented by initializing the MTJ fixed layer magnetization in different directions, which avoids the use of inverters. In addition, the 2–4 decoder adopts a single-input single-fan-out (SISF) structure, which reduces the channel length. To illustrate the advantages of the five-input minority gate, inverter-free structure, and SISF structures in designing the proposed 2–4 decoder, a second 2–4 decoder is proposed that uses three-input minority gates, inverters, and a single-input multiple-fan-out structure. Compared with the second decoder, the first decoder has the layout area reduced to 37.9%, the total channel length reduced to 40.8%, and the number of clock cycles reduced to one-third. Importantly, the design methods used in this work, such as multi-input minority gates, SISF structure, and inverter-free structure, provide an interesting approach for designing large-scale ASL logic circuits.

Keywords: all-spin logic; magnetic tunnel junction; logic design; magnetic devices

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1. Introduction

As CMOS technology approaches its physical limits, many researchers are beginning to explore alternative technologies. Spin-based devices possess the advantages of robustness, ultra-low power consumption, and non-volatility, and are likely to become important candidates in the post-CMOS era [1–7]. Many spin-based devices have been proposed, such as spin field-effect transistors [8], nanomagnetic logic [9], magnetic domain wall logic [10], all-spin logic (ASL) [11], spin-wave-bus devices [12], spin gain transistors [13], etc.

In particular, ASL does not require additional hardware for repeated spin-charge conversion, which has attracted considerable attention [14–24]. Various types of logic circuits based on ASL have been proposed, such as inverter, majority/minority gate [11], D flip-flop [25], full adder [26], RS flip-flop [27], and XOR gate [28]. However, as an important element in logic circuits, the decoder has not been reported in the public as much as we know. A possible reason for this is as follows: decoders are medium-scale circuits that require the combination of several basic logic gates through non-magnetic channels, which usually require long channels to transmit spin information. However, due to the dramatic dissipation of the spin current in the channel, the use of long channels will offset any possible advantage and even cause the circuit to malfunction.

In addition, ASL circuits use the magnetization direction to represent binary information, so it is necessary to initialize the magnetization direction to determine the initial values

of ASL circuits. Ref. [29] proposed a single-input single-fan-out (SISF) structure based on a magnetic tunnel junction (MTJ) to provide input signals for ASL circuits. The SISF structure can reduce the channel length in large-scale ASL circuits with multiple identical inputs, which in turn reduces the dissipation of spin current in the channel.

Unlike traditional CMOS technology, the basic logic gates in ASL circuits are no longer NAND/NOR gates but inverter/buffer and majority/minority gates, as shown in Figure 1. Each device consists of four parts, namely a ferromagnet (FM), channel, spacer, and ground. The magnetization of every FM has two stable states representing binary data, "1" and "0", respectively. If the polarity of the supply voltage V_{ASL} is positive, as in Figure 1a, the magnetization direction of the output FM will be opposite to the magnetization of the input FM, and the inverter can be realized [11]. In Figure 1b, the magnetization direction of the output FM will be opposite to the majority of the magnetization directions of the three input FMs; that is, the minority gate is realized [27].

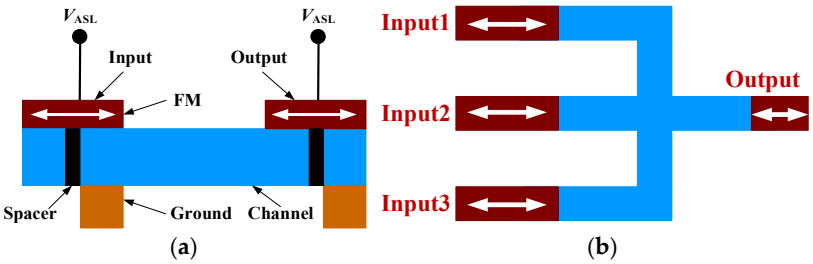

Figure 1. Layout of ASL circuits: (**a**) main view of an inverter; (**b**) top view of a 3-input minority gate.

Based on the three-input minority gate as shown in Figure 1b, a two-input NOR gate can be implemented [27]. However, it would be more convenient to implement a 2–4 decoder using three-input NOR gates. Therefore, it is necessary to use a five-input minority gate to implement three-input NOR gates. Inspired by the above analysis, a 2–4 decoder based on ASL is proposed, which employs SISF structure and five-input minority gates.

2. Design of the Proposed 2–4 Decoder

The truth table of a 2–4 decoder is shown in Table 1. The decoder has an enable terminal S, two inputs A_1 and A_0, and four outputs Y_0~Y_3.

Table 1. The truth table of 2–4 decoder.

S	A_1	A_0	Y_3	Y_2	Y_1	Y_0
1	×	×	0	0	0	0
0	0	0	0	0	0	1
0	0	1	0	0	1	0
0	1	0	0	1	0	0
0	1	1	1	0	0	0

According to Table 1, the expressions for each output can be written as follows:

$$\begin{aligned} Y_0 &= \overline{SA_1A_0} = \overline{S + A_1 + A_0} \\ Y_1 &= \overline{SA_1}A_0 = \overline{S + A_1 + \overline{A_0}} \\ Y_2 &= \overline{S}A_1\overline{A_0} = \overline{S + \overline{A_1} + A_0} \\ Y_3 &= \overline{S}A_1A_0 = \overline{S + \overline{A_1} + \overline{A_0}} \end{aligned} \tag{1}$$

Moreover, if two inputs are set to 1, the expression for the 5-input minority gate becomes

$$M_5(A, B, C, 1, 1) = \overline{A + B + C} \tag{2}$$

and the 3-input NOR logic function is realized. Therefore, to realize Y_0 to Y_3 with 5-input minority gates, the expression for Y_0 to Y_3 can be written as follows:

$$\begin{aligned} Y_0 &= \overline{S + A_1 + A_0} = M_5(S, A_1, A_0, 1, 1) \\ Y_1 &= \overline{S + A_1 + \overline{A_0}} = M_5(S, A_1, \overline{A_0}, 1, 1) \\ Y_2 &= \overline{S + \overline{A_1} + A_0} = M_5(S, \overline{A_1}, A_0, 1, 1) \\ Y_3 &= \overline{S + \overline{A_1} + \overline{A_0}} = M_5(S, \overline{A_1}, \overline{A_0}, 1, 1) \end{aligned} \tag{3}$$

According to the Equation (3), the schematic of the 2–4 decoder is shown in Figure 2.

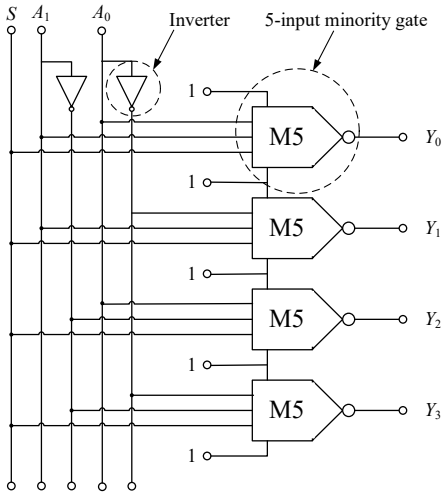

Figure 2. Schematic of 2–4 decoder based on inverter and 5-input minority gate.

As shown in Figure 2, the 2–4 decoder consists of four 5-input minority gates, two inverters, and several connecting lines. Additionally, there are several minority gates that share the same input signal. In ASL circuits, a common method is to use channels to connect input ports and minority gates, resulting in the use of long channels to transmit spin signals. However, as the length of the channel increases, the spin current decays exponentially, leading to a large increase in energy dissipation. In particular, when the length of the channel exceeds the spin diffusion length, the spin current cannot effectively rotate the magnetization direction of the FM.

Moreover, it is necessary to initialize the magnetization direction of FMs in ASL circuits. To avoid the use of long channels and to initialize the magnetization direction of the 2–4 decoder, an SISF structure is used, as shown in Figure 3a. Here, an MTJ is used to realize the charge-to-spin conversion, and there is only one fan-out for each input. Figure 3b is the front view of Figure 3a. The white arrow indicates the magnetization direction of the FMs, where the magnetization direction of the fixed layer remains unchanged, while the magnetization direction of the free layer is determined by the polarity of current *I*.

Figure 4 shows the variation of the magnetization of the free layer in the SISF with the polarity of the current density flowing into the MTJ. It can be seen that the magnetization direction of the free layer is opposite to the polarity of the current density when the magnetization direction of the fixed layer points to the +x axis, while the magnetization direction of the free layer is the same as the polarity of the current density when the magnetization direction of the fixed layer points to the −x axis. Based on this, an original or a reverse variable can be input by setting the initial magnetization direction of the fixed

layer. Specifically, when the magnetization direction of the fixed layer is set to the +x axis, the inverse variable is input, and when the magnetization direction of the fixed layer is set to the −x axis, the original variable is input.

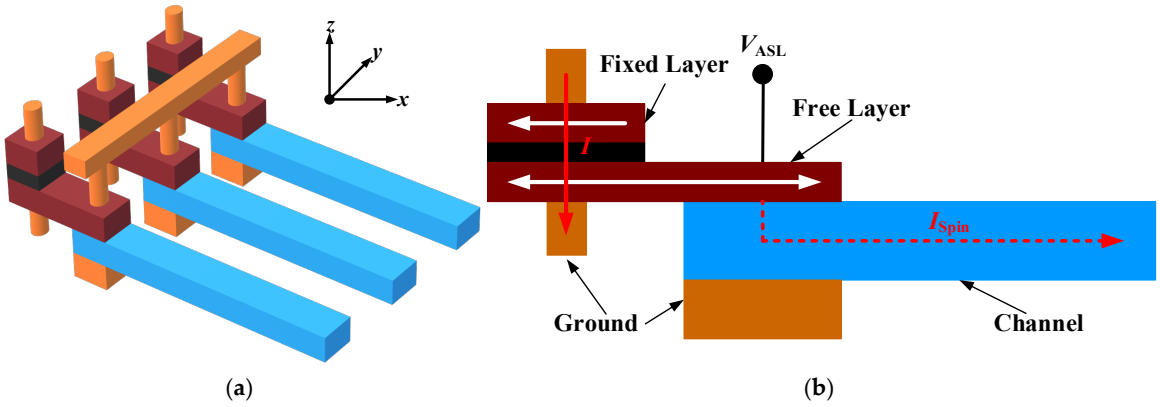

Figure 3. Schematic of SISF structure: (**a**) three-dimensional schematic diagram of SISF structure; (**b**) front view of SISF structure.

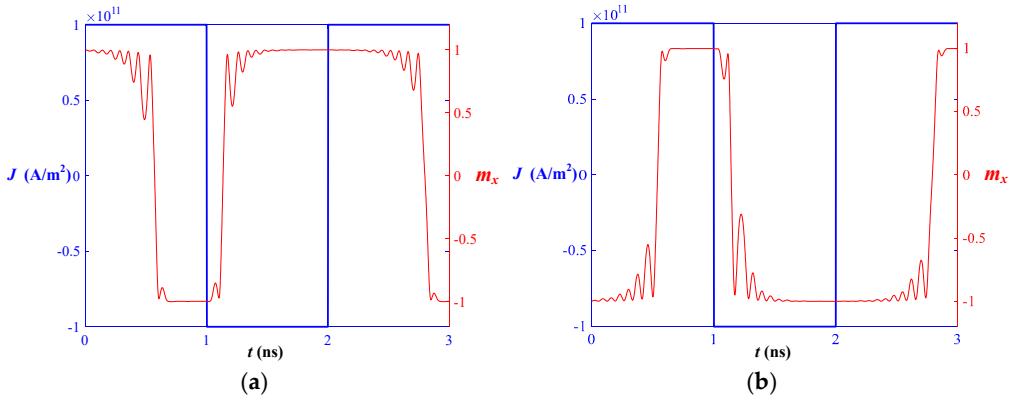

Figure 4. The magnetization of the free layer varies with the polarity of the current density. From (**a**) to (**b**), the magnetization of the fixed layer is in the +x-axis and −x-axis directions, respectively.

According to Equation (3), the inputs of the original variable and the inverse variable are necessary for the decoder. The general practice is to use inverters to transform original variables into inverse variables, as shown in Figure 2. However, according to the above, it is possible to implement the inputs of the original and inverse variables by initializing the MTJ fixed layer in different directions, which eliminates the use of an inverter, thus reducing the signal transmission path and shortening the clock cycle.

Based on the above description, Figure 5 shows the local layouts of Y_0 to Y_3, where each local layout is a 5-input minority gate with an SISM structure. FM1, FM2, and FM3 are both the free layers of the MTJ and the inputs of the 5-input minority gate. Their magnetization directions are determined by the input signals S, A_1, and A_0, respectively. FM4 and FM5 are the inputs of the minority gate, and their magnetizations are fixed to the +x axis direction, representing input logic 1. FM6 is the output of the minority gate, and its magnetization direction is determined by the magnetization direction of the five inputs. When a positive voltage V_{ASL} is applied, the 3-input NOR logic function shown in Equation (2) can be realized.

It should be noted that although all four local layouts are structurally the same, the magnetization direction of the fixed layer is different in each local layout. If the input is an original variable, the magnetization of the fixed layer connected to that input is initialized

to the −x axis direction, and if the input is an inverse variable, the magnetization of the fixed layer is initialized to the +x axis direction.

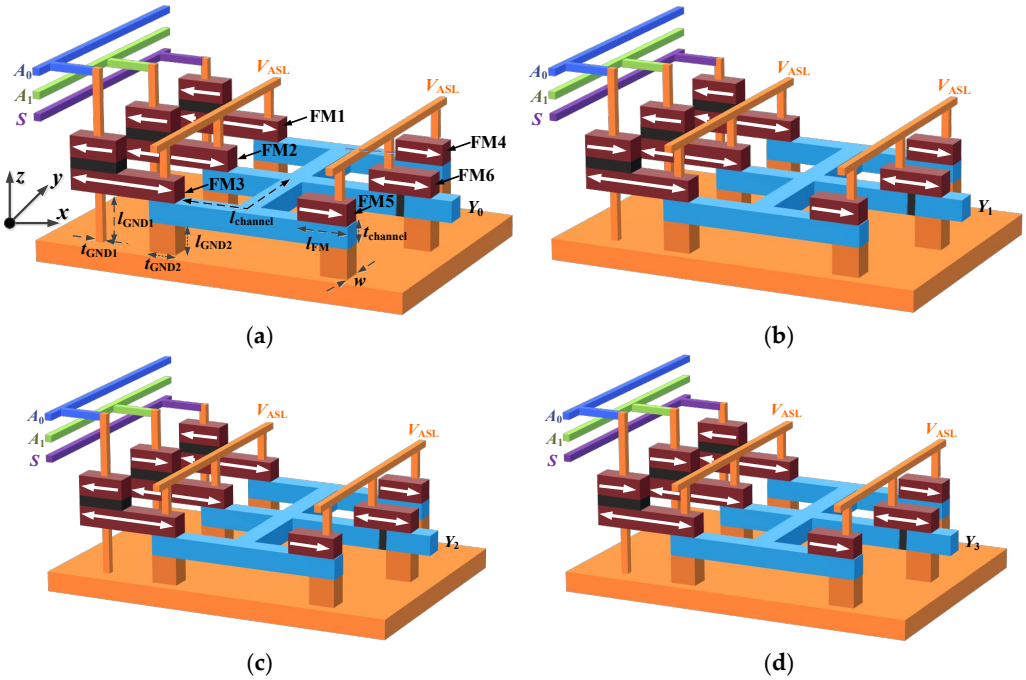

Figure 5. The local layout of Y_0 to Y_3: (**a**) the magnetizations of all three MTJ fixed layers are initialized to the −x axis; (**b**) the magnetizations of the fixed layers connected to the S and A_1 point to the −x axis, while the magnetization of the fixed layer connected to the A_0 points to the +x axis; (**c**) the magnetizations of the fixed layers connected to the S and A_0 point to the −x axis, and the magnetization of the fixed layer connected to the A_1 points to the +x axis; (**d**) the magnetization of the fixed layer connected to the S points to the −x axis direction, while the magnetizations of the fixed layers connected to the A_0 and A_1 point to the +x axis.

The four local layouts shown in Figure 5 are connected together to form a complete 2–4 decoder, as shown in Figure 6.

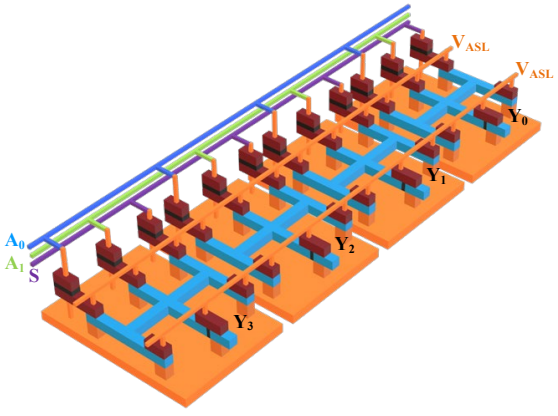

Figure 6. The overall layout of the 2–4 decoder.

3. Functional Verification of the 2–4 Decoder

The proposed 2–4 decoder consists of four identical 5-input minority gates, and in each minority gate, the magnetizations of FM1~FM3 are affected by the current flowing through the MTJ and the operating voltage V_{ASL}, and their magnetization dynamic behavior can be described as follows [29]:

$$\frac{\mathrm{d}\boldsymbol{m}_n}{\mathrm{d}t} = -\gamma\mu_0\boldsymbol{m}_n \times \boldsymbol{H}_{\mathrm{eff}} + \alpha\boldsymbol{m}_n \times \frac{\mathrm{d}\boldsymbol{m}_n}{\mathrm{d}t} + \xi\boldsymbol{m}_n \times (\boldsymbol{m}_n \times \boldsymbol{M}_n) + \frac{1}{qN_S}\boldsymbol{m}_n \times (\boldsymbol{I}_{Sn} \times \boldsymbol{m}_n) \quad n = 1,2,3 \tag{4}$$

where γ, μ_0, α, q, and N_s represent the electron gyromagnetic ratio, the free space permeability, the Gilbert damping of the magnetic material, the magnitude of the electron charge, and the number of Bohr magnetons of FMs, respectively; $\boldsymbol{m}_n$ and $\boldsymbol{M}_n$ are the normalized magnetization of the nth MTJ free-layer and fixed-layer magnets, respectively; and $\boldsymbol{I}_{Sn}$ is the spin current flowing into the nth FM. $\boldsymbol{H}_{\mathrm{eff}}$ is the effective magnetic field of FM, and ξ is the asymmetric Slonczewski type torque coefficient [19,29].

FM4~FM6 are only affected by the spin current in channels, and their magnetization dynamic behavior can be described as follows [30]:

$$\frac{\mathrm{d}\boldsymbol{m}_n}{\mathrm{d}t} = -\gamma\mu_0\boldsymbol{m}_n \times \boldsymbol{H}_{\mathrm{eff}} + \alpha\boldsymbol{m}_n \times \frac{\mathrm{d}\boldsymbol{m}_n}{\mathrm{d}t} + \frac{1}{qN_\mathrm{S}}\boldsymbol{m}_n \times (\boldsymbol{I}_{Sn} \times \boldsymbol{m}_n) \quad n = 4,5,6 \tag{5}$$

From Equations (4) and (5), it can be seen that to obtain the magnetization precession trajectory of the FMs, it is also necessary to know the spin current $\boldsymbol{I}_S$. This requires a spin transport model [30] to obtain the spin currents. The equivalent spin transport model for the 5-input minority gate is constructed as shown in Figure 7. $\boldsymbol{G}_k^{\mathrm{FM}}(k = 1,2,\cdots,9)$ is the interface conductance matrix of the interface, $\boldsymbol{G}_k^{\mathrm{seg}}(k = 1,2,\cdots,8)$ and $\boldsymbol{G}_k^{\mathrm{shg}}(k = 1,2,\cdots,8)$ are the series conductance matrix and shunt conductance matrix of the GNDs, and $\boldsymbol{G}_k^{\mathrm{sec\,h}}(k = 1,2,\cdots,6)$ and $\boldsymbol{G}_k^{\mathrm{shch}}(k = 1,2,\cdots,6)$ are the series conductance matrix and shunt conductance matrix of channels [17].

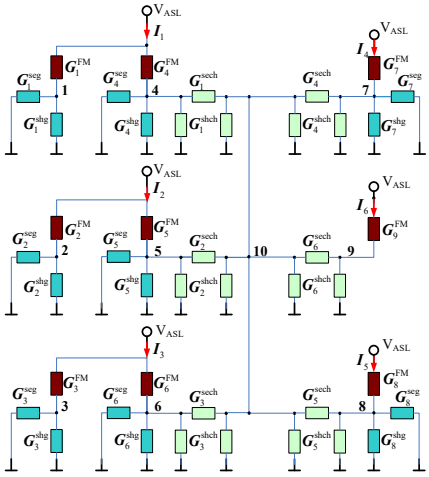

Figure 7. The equivalent spin transport model for 5-input minority gate.

The voltage vector of each node in Figure 7 can be obtained by a node analysis. And the currents flowing into the FMs can be obtained by the voltage vectors. With the obtained currents, the magnetizations of the FMs are obtained by Equations (4) and (5). By iteratively solving the spin transport model and the magnetization dynamics model, which is usually called the magnetization dynamics/spin transport simulation framework [25,30], the magnetization precession trajectory of the FMs can be obtained.

To make the 2–4 decoder work properly, an asynchronous clock control scheme is proposed, as shown in Figure 8, where the input signals are divided into three phases, called "Reset", "Input", and "Hold", and the operating voltage is divided into two phases, called "Keep" and "Switch". One clock cycle is assumed to be 6ns. It is important to note that the assumed clock period is merely a conservative estimate based on the parameters listed in Table 2, ensuring the decoder's normal operation. By optimizing the magnet's size

or material [17], or opting for materials with long spin diffusion lengths, such as grapheme, as the channel [16], the clock period can be further shortened.

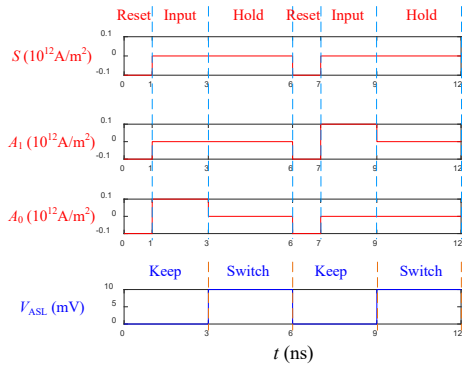

Figure 8. The asynchronous clock control scheme for the 2–4 decoder.

Table 2. Default dimension and material parameters for 2–4 decoder.

Parameters	Description	Values	Parameters	Description	Values
l_{FM_L} (nm)	length of FM 1, 2, and 3	100	α	Gilbert damping constant of Py	0.007
l_{FM_R} (nm)	length of FM 4, 5, and 6	50	χ	TMR asymmetry parameter	4
l_{FM_F} (nm)	length of MTJ fixed layers	40	λ_{Cu} (nm)	spin flip length of Cu	350
$l_{channel\_L}$ (nm)	length of channel 1, 3, 4, and 5	250	T (K)	Kelvin temperature	300
$l_{channel\_S}$ (nm)	length of channels 2 and 6	200	ε	spin polarization efficiency constant	0.35
l_{GND1} (nm)	length of MTJ GND	70	ρ_{Cu} ($\Omega \cdot$ nm)	resistivity of Cu	34
$t_{channel}$ (nm)	thickness of channel	50	M_S (A·m^{-1})	saturation magnetization of Py	8×10^5
t_{FM} (nm)	thickness of FMs	0.8	TMR	tunnel magneto-resistance of MTJ	10%
t_{GND1} (nm)	thickness of MTJ GND	20	K_μ (Jm^{-3})	uniaxial anisotropy parameter for FMs	1.923×10^4
t_{GND2} (nm)	thickness of minority GND	40	$\boldsymbol{N}_{d1}$	demagnetizing tensor for FM1~3	[0.012 0.041 0.947]
w(nm)	width of device	30	$\boldsymbol{N}_{d2}$	demagnetizing tensor for FM4~6	[0.023 0.039 0.938]
l_{GND2} (nm)	length of minority GND	20	RA (Ωm^2)	resistance area product of MTJ	0.8×10^{-12}

For the input signal, during the "Reset" phase, the current density is -0.1×10^{12} A/m^2, which causes the magnetization direction of the MTJ free layer to rotate from the initial state to the same direction as that of the MTJ fixed layer, which is called "Reset".

In the "Input" phase, if the input is a logic "0", the current density is 0, which causes the magnetization of the free layer to remain constant; if the input is a logic "1", the current density is 0.1×10^{12} A/m^2, which causes the magnetization direction of the free layer to be opposite to that of the fixed layer.

In the "Hold" phase, the current densities of S, A_1, and A_0 are all zero, and the magnetizations of FM1, FM2, and FM3 remain unchanged in preparation for the minority gate operation.

For the operating voltage, during the "Keep" phase, the operating voltage V_{ASL} applied to the minority gate is 0, the minority gate does not operate, and the magnetization of the FM6 remains unchanged.

In the "Switch" phase, the operating voltage applied to the minority gate becomes 10 mV, and the minority gate starts to operate. The magnetization of FM6 depends on the magnetizations of the five inputs.

In the 2–4 decoder, the parameters of the four 5-input minority gates are completely identical except for the different magnetization directions of the fixed layer. The default parameters are shown in Table 2.

Suppose that the initial magnetization directions of FM4 and FM5 are both $+x$ axis, and the initial magnetization directions of the other FMs are all $-x$ axis. Figure 9 shows the time evolution of magnetization in the x-direction of the 2–4 decoder under the signals shown in Figure 8. Due to space limitations, Figure 9 shows only the time evolution of the x-direction magnetization of six FMs in Y_1 (Figure 5b). Assume that when the x-direction magnetization is 1, it means logic 1, and when it is -1, it means logic 0.

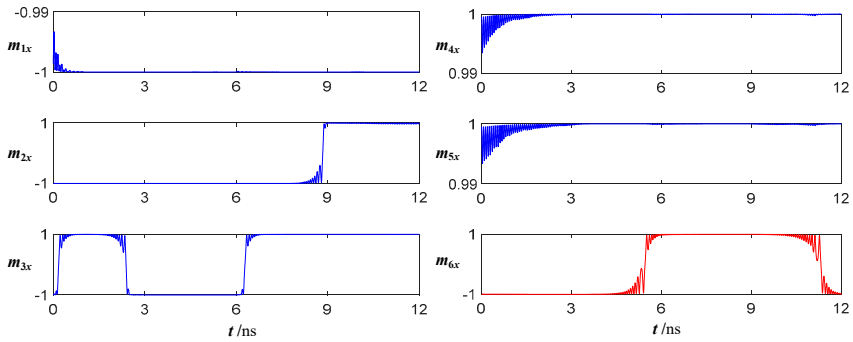

Figure 9. Simulation result of the Y_1.

During 0~1 ns, the input signals are in the "Reset" phase and the magnetization directions of the MTJ fixed layers are as shown in Figure 5b, so m_{1x} and m_{2x} basically remain at -1, while m_{3x} rotates from -1 to +1. At this time, the operating voltage is in the "Keep" phase, the minority gate does not operate, and m_{4x}, m_{5x}, and m_{6x} remain unchanged.

During 1~3 ns, the input signals are in the "Input" phase, the current density of S and A_1 is 0, and the current density of A_0 is 1×10^{11} A/m^2, so that m_{1x} and m_{2x} remain basically unchanged at -1, while m_{3x} rotates from +1 to -1. At this time, the operating voltage is still in the "Keep" phase, and m_{4x}, m_{5x}, and m_{6x} remain unchanged.

During 3~6 ns, the input signals are in the "Hold" phase, so that m_{1x}, m_{2x}, and m_{3x} remain at -1. At this time, the operating voltage is in the "Switch" phase, and the minority gate begins to operate. Since two of the five input FMs' magnetization directions point to the +x axis, which is a minority, m_{6x} rotates from -1 to +1.

During the period of 6~12 ns, it is the next clock cycle, and the analysis is basically the same as above, so it does not need to be repeated here. In addition, as can be seen in Figure 9, m_{4x} and m_{5x} remain approximately +1 throughout the cycle, indicating that the magnetization directions of FM4 and FM5 always point to the +x axis direction, which is consistent with our expectations.

To verify the function of each subcircuit shown in Figure 5, Figure 10 shows the time evolution of the x-direction magnetization of outputs Y_0, Y_1, Y_2, and Y_3 under different inputs.

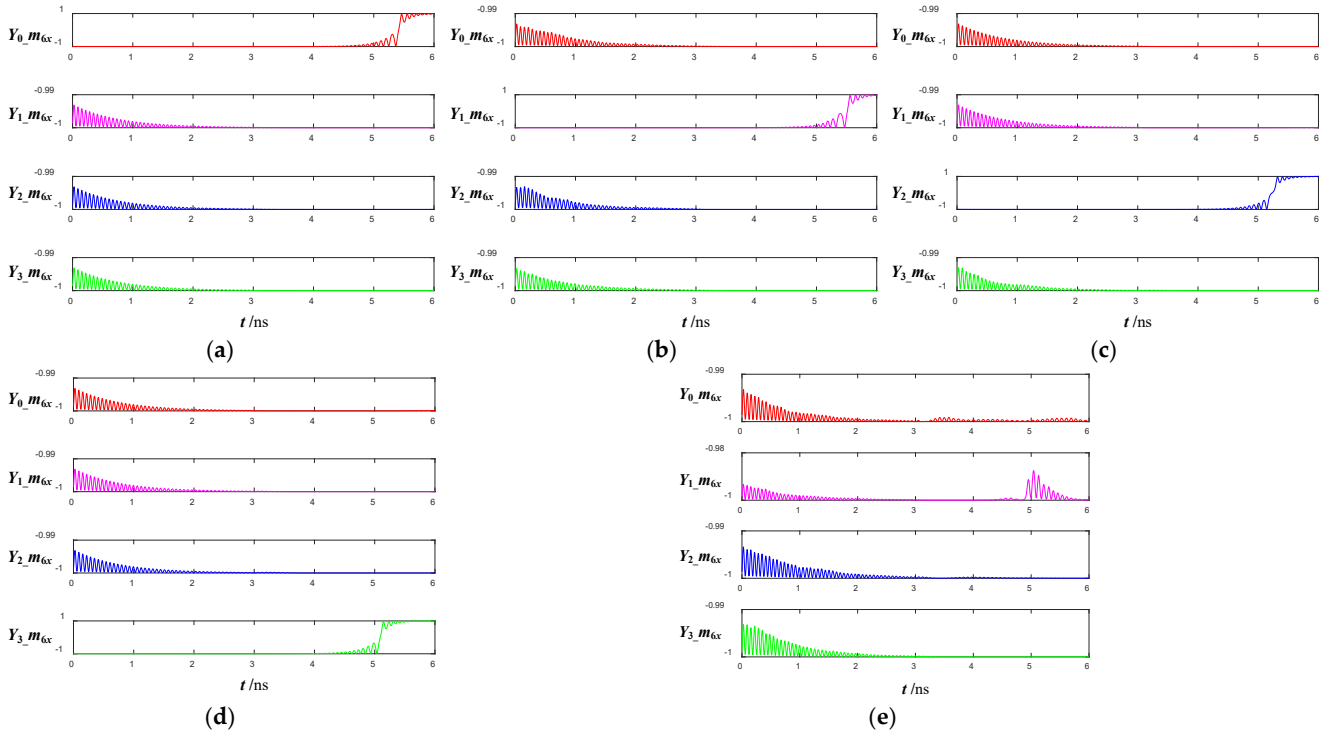

Figure 10. The 2–4 decoder simulation results for different inputs. During 1~3 ns, the logic value of S, A_1, and A_0 in (**a**–**d**) is 000~011, respectively, and the logic value of S, A_1, and A_0 in (**e**) is 110.

From Figure 10a–d, in the "switch" phase, when SA_1A_0 = 000, $Y_0Y_1Y_2Y_3$ = 1000; when SA_1A_0 = 000 = 001, $Y_0Y_1Y_2Y_3$ = 0100; when SA_1A_0 = 000, $Y_0Y_1Y_2Y_3$ = 0010; and when SA_1A_0 = 000 = 011, $Y_0Y_1Y_2Y_3$ = 0001. Moreover, Figure 10e shows that there is $Y_0Y_1Y_2Y_3$ = 0000 when SA_1A_0=110. (Due to space limitations, only the simulation results of SA_1A_0 = 110 are shown. If SA_1A_0 = 100, SA_1A_0 = 101, or SA_1A_0 = 111, there is still $Y_0Y_1Y_2Y_3$ = 0000.) This is entirely consistent with Table 1, which verifies that the 2–4 decoder functions correctly.

4. The Results and Discussions

The total energy dissipation of the 2–4 decoder consists of the energy dissipation of the MTJs and the energy dissipation of the minority gates, as follows:

$$E_{\text{total}} = E_{\text{MTJ}} + E_{\text{Minority}} \tag{6}$$

The energy dissipation of the MTJs is

$$E_{\text{MTJ}} = \int_0^T \sum_{k=1}^{3} I_k^2 R_k^{\text{MTJ}} \mathrm{d}t = \int_0^T \sum_{k=1}^{3} \left(J_k S_k^{\text{MTJ}}\right)^2 R_k^{\text{MTJ}} \mathrm{d}t \tag{7}$$

where T is the clock cycle, S_k^{MTJ} is the cross-sectional area of the k-th MTJ, and R_k^{MTJ} is the resistance of the k-th MTJ, and can be expressed as

$$R^{\text{MTJ}} = R_{\text{P}} + \frac{1}{2}(R_{\text{AP}} - R_{\text{P}})(1 - \cos\theta(t)) \tag{8}$$

R_{P} and R_{AP} are the MTJ resistances when the magnetization directions of the fixed layer and the free layer are parallel and anti-parallel, respectively. And $\theta(t)$ is the angle between the magnetization vectors of free layer and fixed layer, which varies with time.

The energy dissipation of minority gates is

$$E_{\text{Minority}} = \sum_{i=0}^{3} \int_0^T \sum_{k=1}^{6} V_{\text{ASL}} I_{i,k}^C \mathrm{d}t \tag{9}$$

where $I_{i,k}^C$ is the charge current flowing into the k-th FM in the i-th minority gate.

Table 3 shows the energy dissipation of the MTJs and minority gates under different inputs. It can be seen that the E_{Minority} is basically the same under different inputs, which is about 9.30 pJ. This is because the energy dissipation of minority gates is mainly determined by the charge currents flowing into FMs and the operating voltage V_{ASL} applied to them, and the charge currents are not affected by the inputs, so different inputs have little effect on the energy dissipation of minority gates. However, the E_{MTJ} varies greatly under different inputs, because when the input signal changes, the current density flowing into the MTJs changes accordingly, and it can be seen from Equation (8) that the E_{MTJ} will be different.

Table 3. The energy dissipation of MTJs and minority gates under different inputs.

SA_1A_0	E_{MTJ} (pJ)	E_{Minority} (pJ)	SA_1A_0	E_{MTJ} (pJ)	E_{Minority} (pJ)
000	0.116	9.299	100	0.194	9.297
001	0.195	9.299	101	0.272	9.297
010	0.195	9.299	110	0.272	9.296
011	0.273	9.299	111	0.351	9.297

The energy dissipation of the MTJ, which is also the energy dissipation of the SISF structure, only has an average value of about 0.23 pJ, which is about 1/40 of the energy dissipation of the MTJs and minority gate. This shows that the increase in the energy dissipation of the MTJs due to the increase in the number of MTJs resulting from the employment of the SISF structure is negligible.

In addition, according to the research findings presented in Refs. [31,32], replacing the insulating layer in the MTJ with Sr2RuO4, an unconventional superconducting material, could potentially eliminate the charge current and only retain the spin current within the MTJ, thereby further reducing its energy consumption. Consequently, the marginal increase in energy consumption resulting from an increase in the number of SISFs will become even more negligible.

To illustrate the advantages of the five-input minority gate and SISF structure in designing the 2–4 decoder, another 2–4 decoder designed using three-input minority gates, inverters, and a single-input multi-fan-out (SIMF) structure is given below and is called the second decoder for convenience. The logical expression for the second decoder is

$$\begin{aligned}
Y_0 &= \overline{S + A_1 + A_0} = M_3\left(\overline{M_3(S, A_1, 1)}, A_0, 1\right) \\
Y_1 &= \overline{S + A_1 + \overline{A_0}} = M_3\left(\overline{M_3(S, A_1, 1)}, \overline{A_0}, 1\right) \\
Y_2 &= \overline{S + \overline{A_1} + A_0} = M_3\left(\overline{M_3(S, \overline{A_1}, 1)}, A_0, 1\right) \\
Y_3 &= \overline{S + \overline{A_1} + \overline{A_0}} = M_3\left(\overline{M_3(S, \overline{A_1}, 1)}, \overline{A_0}, 1\right)
\end{aligned} \tag{10}$$

where $M_3(A, B, C)$ denotes a three-input minority gate, and when one of the inputs is set to 1, its logical expression becomes

$$M_3(A, B, 1) = \overline{A + B} \tag{11}$$

According to Equation (11), the 2D schematic diagram of the second decoder is shown in Figure 11. To avoid the crossover of channels, the three inputs are not in the same plane.

The channel connected to A_1 is in the top layer, A_0 is in the middle layer, and S is in the bottom layer. The white arrow indicates that the input FM of the three-input minority gate is magnetized in the +x-axis direction, representing logic 1.

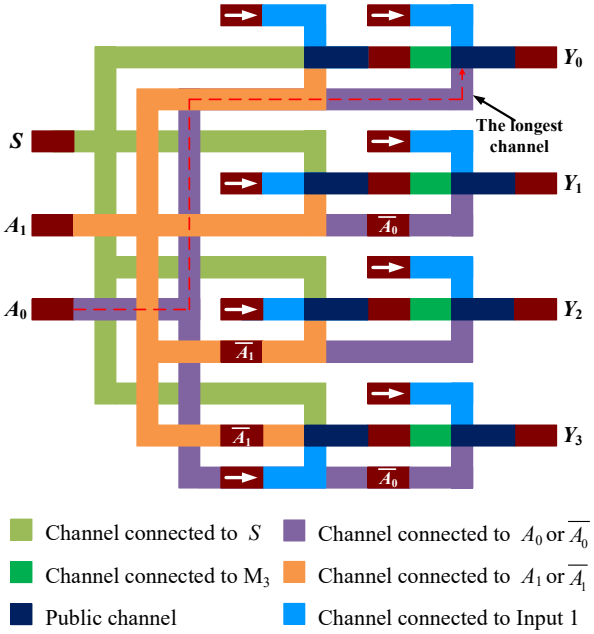

Figure 11. The 2D schematic diagram of the second decoder.

Table 4 shows the performance comparison of the two types of 2–4 decoders. The dimensional parameters in Table 2 are used for both decoders, and in addition, the spacing between each minority gate is assumed to be 20 nm. Compared to the second decoder, the first decoder (decoder shown in Figure 5) reduces the total channel length to 40.8%, the layout area to 37.9%, and the number of clock cycles to one-third. In particular, the second decoder has a maximum channel length of 1430 nm, which exceeds the spin diffusion length of most currently known metallic materials, which would cause the decoder to fail. Therefore, the simulation results for the operation of the second decoder are not provided here. In addition, despite the increase in the number of FMs in the first decoder, mainly by nine MTJs, its impact on energy dissipation is negligible according to the previous description.

Table 4. Performance comparison of the two decoders.

Performance	First Decoder	Second Decoder
Maximum channel length (nm)	250	1430
Total length of channels (nm)	5200	12,740
Number of FMs	36	26
Layout area (um^2)	0.319	0.841
Number of clock cycles	1	3

In summary, for logic circuits such as 2–4 decoders with multiple identical inputs, the use of the SISF structure and multiple-input minority gates can result in significant improvements in terms of layout area, clock cycles, and so on.

5. Conclusions

In this paper, a 2–4 decoder based on ASL and a MTJ is proposed, and its logic function is verified by a magnetization dynamics/spin transport self-consistent simulation

framework. The proposed 2–4 decoder employs an SISF structure to provide input to the circuit, thus reducing the channel length of the circuit. At the same time, five-input minority gates are employed, which greatly simplifies the circuit scale. In addition, the original variables and the inverse variables are realized by setting the magnetization of the MTJ fixed layer in different directions, which avoids the use of inverters and further reduces the circuit scale. Compared to the 2–4 decoder using three-input minority gates, inverters, and the SIMF structure, the proposed 2–4 decoder shows significant improvement in maximum channel length, total channel length, layout area, and the number of clock cycles, except for the number of FMs. Most importantly, the design methods used in this paper, such as the SISF structure, multi-input majority/minority gate, and inverter-free structure, provide a way to design more large-scale ASL circuits in the future.

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