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Gel-Based PVA/SiO_2/p-Si Heterojunction for Electronic Device Applications

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Abstract: The current work presents a new structure based on Au/PVA/SiO_2/p-Si/Al that has not been studied before. An aqueous solution of polyvinyl alcohol (PVA) polymer gel was deposited on the surface of SiO_2/Si using the spin-coating technique. The silicon wafer was left to be oxidized in a furnace at 1170 k for thirty minutes, creating an interdiffusion layer of SiO_2. The variations in the dielectric constant (ϵ'), dielectric loss (ϵ''), and dielectric tangent (tanδ) with the change in the frequency, voltage, and temperature were analyzed. The results showed an increase in the dielectric constant (ϵ') and a decrease in the dielectric loss (ϵ'') and tangent (tanδ); thus, the Au/PVA/SiO_2/p-Si/Al heterostructure has opened up new frontiers for the semiconductor industry, especially for capacitor manufacturing. The Cole–Cole diagrams of the ϵ'' and ϵ' have been investigated at different temperatures and voltages. The ideality factor (n), barrier height (Φ_b), series resistance (R_s), shunt resistance (R_{sh}), and rectification ratio (RR) were also measured at different temperatures.

Keywords: gel materials; heterojunction diode; I–V and C–V characterization; polyvinyl alcohol (PVA); polymer oxide semiconductor

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Citation: Ashery, A.; Gaballah, A.E.H.; Turky, G.M.; Basyooni-Murat Kabatas, M.A. Gel-Based PVA/SiO_2/p-Si Heterojunction for Electronic Device Applications. *Gels* **2024**, *10*, 537. https://doi.org/10.3390/gels10080537

Academic Editor: Esmaiel Jabbari

Received: 27 June 2024
Revised: 11 August 2024
Accepted: 17 August 2024
Published: 20 August 2024

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1. Introduction

In recent years, there has been significant progress in developing materials and techniques for sensor applications, particularly those involving thin films and nanostructures [1,2]. Polymer oxide semiconductor (POS) structures consist of a thin oxide film between a polymer and a semiconductor [3]. The oxide layer prevents inter-diffusion between the polymer and semiconductor substrate and improves the electric field reduction inside the structures [4–6]. It enhances the electrical and dielectric properties of devices such as capacitors [7–9], which increases the electric charge's storage capacity. The creation of oxide thin films on Si substrates using traditional methods of oxidation or deposition cannot passivate the active hanging bonds on the surface of semiconductors [10,11]. The carrier lifetime remains more prolonged at high angular frequencies than the period (T = 1/x). Thus, the charges at the border states cannot track an AC sign [12]. Contrarily, the charges at minor frequencies could follow the AC signal, and thus, the effect of these charges on the capacitance of devices increases with decreasing frequency [13].

Consequently, the electrical and dielectric characteristics depend on the frequency, making accuracy and trust results very significant. The interface states at the Si/SiO_2,

PVA/SiO_2 interfaces, and device contacts cause deviation from the perfect case [14,15]. These interfaces commonly cause a bias change and frequency dispersal of the C–V and G–V curves [16]. Thus, it is noteworthy to incorporate the effect of the frequency and thoroughly inspect the frequency dispersal of the dielectric properties. The frequency dependence of the dielectric constant (ϵ'), dielectric loss (ϵ''), and dielectric tangent (tanδ) is dominated by a small frequency dispersal, whose physical origin has long been in question. The innovation in this paper is that we have synthesized the Au/PVA/SiO_2/p-Si/Al structure, which has not been investigated before. We present a whole study of the dielectric constant (ϵ'), dielectric loss (ϵ''), and dielectric tangent (tanδ) with the variation of the frequency, voltage, and temperature. We also succeeded in improving the dielectric constant (ϵ') and reducing the dielectric loss (ϵ'') and the tangential component (tanδ); thus, the current structure is considered a promising material for the development of capacitors. The Cole–Cole diagrams of the ϵ'' and ϵ' at different voltages and temperatures have been examined. In addition to that, the I–V measurements were performed to retrieve information about its electrical properties, such as the ideality factor (n), barrier height (Φ_b), series resistance (R_s), shunt resistance (R_{sh}), and rectification ratio (RR) over different temperatures.

2. Results and Discussion

2.1. Scanning Electron Microscope and X-ray Diffraction Pattern

SEM Analysis: Figure 1 shows the surface topography of the PVA layer on the SiO_2/Si substrate. The SEM micrograph reveals a uniform distribution across the surface, with some cracks visible. These cracks are assumed to have originated from the drying process of the PVA film as the solvent evaporated, causing shrinkage and resulting in stress-induced cracks. The surface morphology of the PVA is relatively smooth, with minimal porosity, indicating a dense film formation.

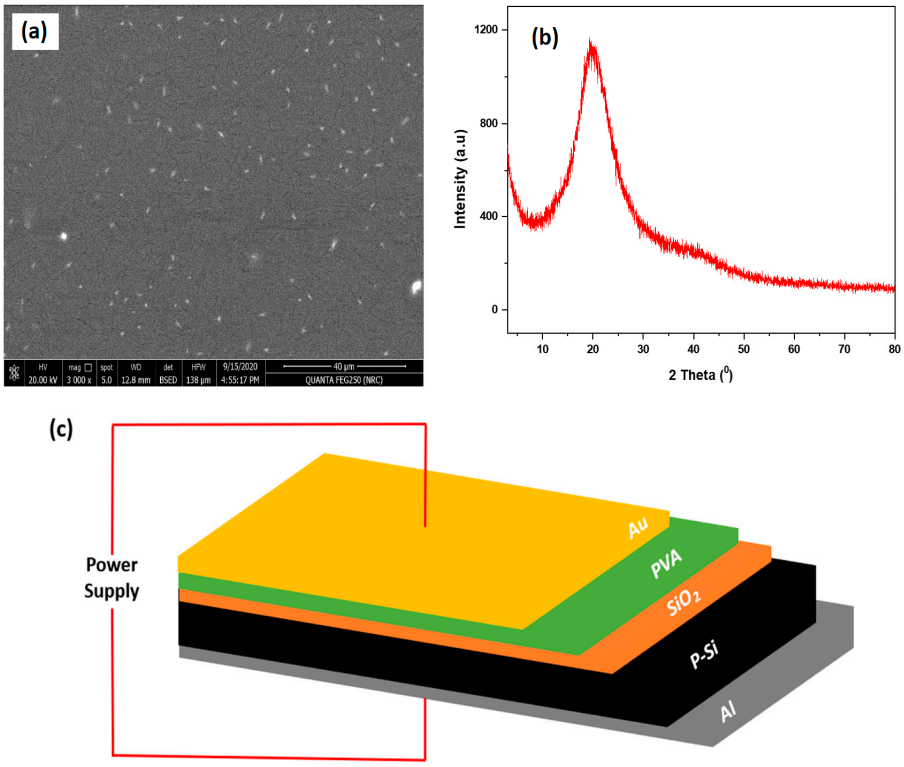


Figure 1. (**a**) SEM of the Au/PVA/SiO_2/p-Si/Al structure, (**b**) XRD of the Au/PVA/SiO_2/p-Si/Al structure, and (**c**) Au/PVA/SiO_2/p-Si/Al structure.

XRD Analysis: Figure 2 presents the XRD pattern of the PVA/SiO_2/Si thin film. The XRD spectrum exhibits a prominent peak at 2θ = 19.7°, which is characteristic of the semi-crystalline nature of the PVA film. The broadening of the halo and the absence of sharp

diffraction peaks confirm the semi-crystalline structure of the PVA, suggesting that the material has both amorphous and crystalline regions [17].

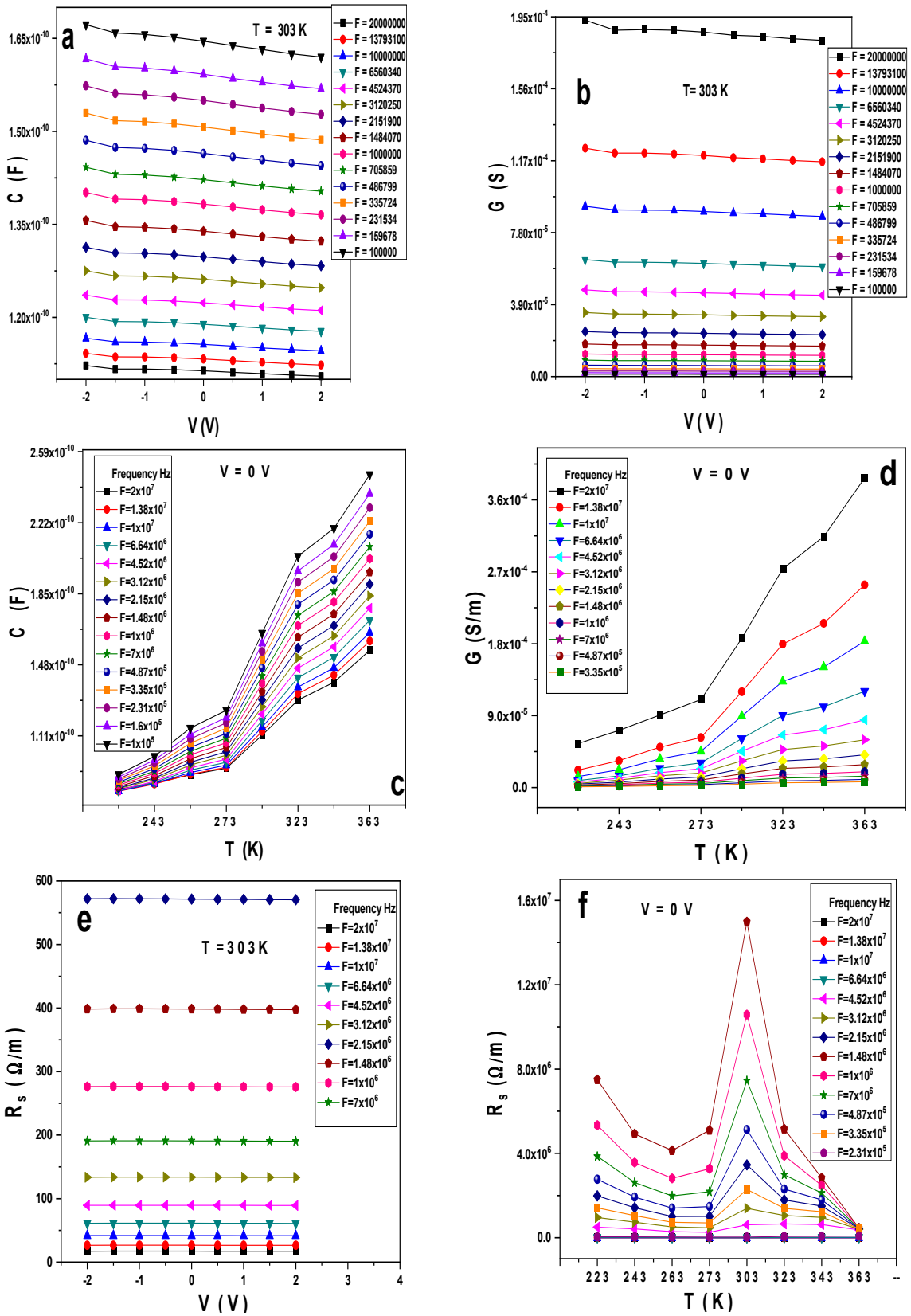


Figure 2. (**a**–**f**) The experimental (**a**) C–V, (**b**) G–V, (**c**) C–T, (**d**) G–T, (**e**) Rs–V, and (**f**) Rs–T for the Au/PVA/SiO_2/p-Si/Al structure.

Additionally, the I–V and C–V characteristics were measured using a Keysight model B2901A and a Novocontrol high-resolution alpha analyzer. These measurements were supported by a Quatro temperature controller, which maintained the temperature stability to within 0.2 K using clean nitrogen as a heating agent.

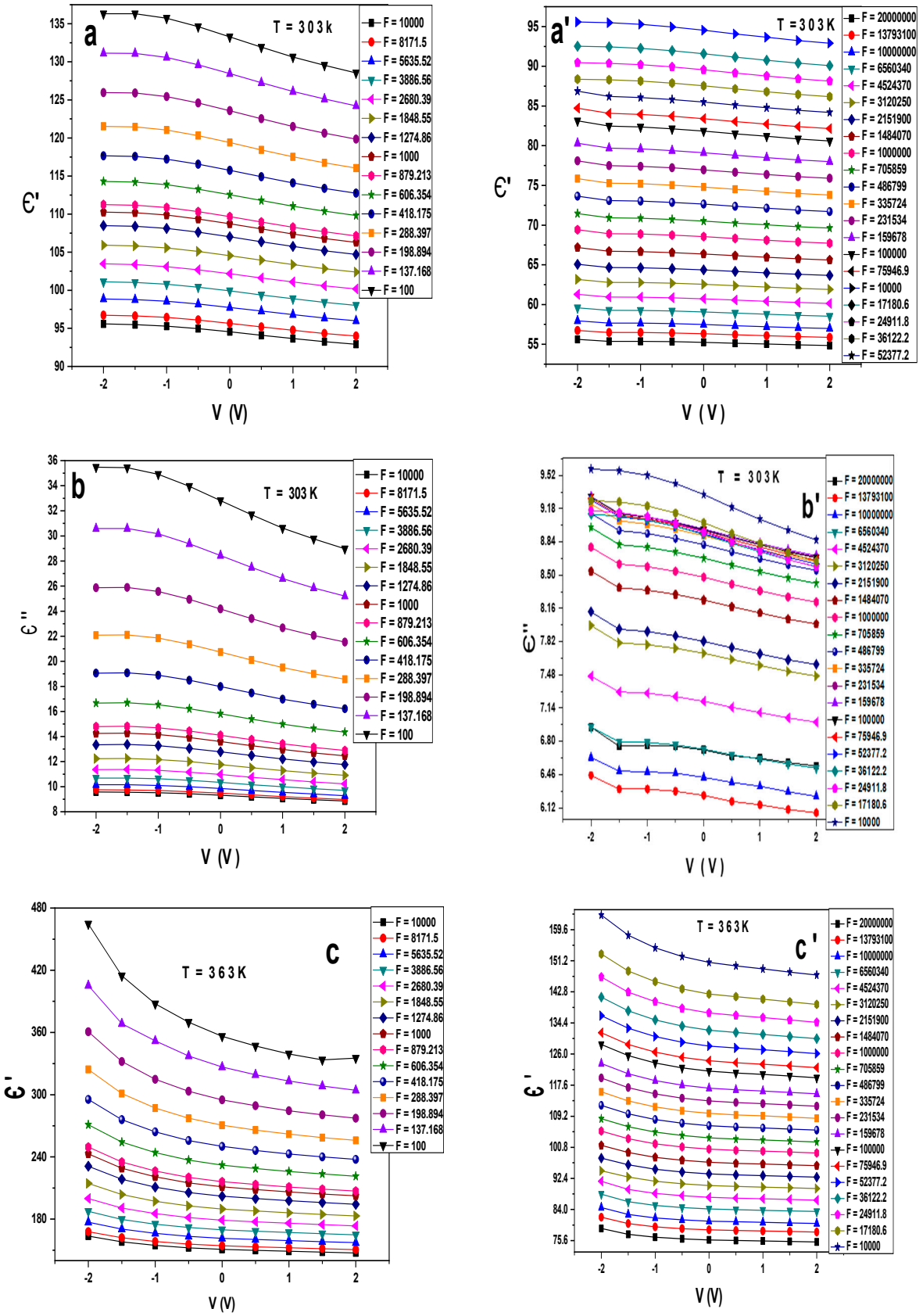
2.2. Dielectric Characterization

Figure 2a,b display the variation of the capacitance (C) and conductance (G) with the voltages and frequencies at a temperature of 303 K for the Au/PVA/SiO_2/p-Si/Al structure. As observed in Figure 2a, the capacitance decreases with the frequency, while the conductance increases. C and G are still independent of the voltage changes. At the same time, the conductance might be attributed to the spreading profile of the interface density of states at the PVA/p-Si and PVA/SiO_2 interface and series resistance (Rs) [18,19]. Figure 2c,d display the variation of C and G with the temperature at different frequencies and a constant voltage V = 0 V; both rise with the temperature. The variation of the series resistance (R_s) with the voltage at different frequencies at room temperature is seen in Figure 2e; it decreases with the frequencies, while Rs shows peaks at room temperature, as displayed in Figure 2f, and then decreases at high temperatures.

Figure 3a–b′ display the variation of the dielectric constant ϵ' and ϵ'' at different frequencies and room temperature for Au/PVA/SiO_2/p-Si/Al. It is seen that ϵ' decreases with the frequencies, and its value ranges from 56 to 135, while the dielectric loss ϵ'' decreases with the frequency, taking values from 6 to 36. Here, we enhanced the values of ϵ' and reduced the values of ϵ'', as shown in Figure 3b,b′. At a temperature of 363 K, ϵ' increases from 75 to 480 while ϵ'' reduces from 13 to 380, as illustrated in Figure 4c,d. On the other hand, working at a low temperature equal to 223 k, the values of ϵ' and ϵ'' range from 41 to 60 and from 1 to 4.4, respectively, as illustrated in Figure 3e–f′. As described above, we can increase the dielectric constant's value and reduce the dielectric loss's value with varying temperatures and frequencies. Still, their values are independent of the change in the voltage. It is stated that the values of ϵ' and ϵ'' depend on several factors related to the interface state density, interfacial layer thickness, series resistance, doping concentration, etc. [17,20].

Figure 4a–h illustrate the variation of ϵ' and ϵ'' with the voltages at different temperatures and constant different frequencies for Au/PVA/SiO_2/p-Si/Al. At the frequency 2×10^7 Hz, ϵ' and ϵ'' increase with the temperatures and their values range from 40 to 80 and 3 to 15, respectively. The dielectric constant and dielectric loss dependence on the voltage is almost low, as shown in Figure 4a,b. At the frequency 10^5 Hz, the values of ϵ' and ϵ'' range from 45 to 120 and 2 to 24, respectively, as displayed in Figure 4c,d, while at the frequencies 10^3 and 10 Hz, ϵ'' increases to large undesirable values, as shown in Figure 4e–h. These variations in the conductance of ϵ' and ϵ'' can also be due to polarization mechanisms such as Maxwell–Wagner [21] and space charge [22,23]. Through the above, it can be concluded that at high frequencies, the value of the dielectric loss is minimal. The industry needs to reduce the value of the heat loss at medium and low frequencies as the value of constant loss rises, which is undesirable.

Figure 5a–f illustrate the variation of ϵ', ϵ'', and tanδ with the frequency at different voltages and fixed temperatures for Au/PVA/SiO_2/p-Si/Al. At a low temperature of 223 k, the behavior is the same for all the ϵ', ϵ'', and tanδ, and the difference is that ϵ'' and tanδ have two peaks at low and high frequencies. The most significant finding here was the enhancement of the value of ϵ' in the range of 40–70 and the decrease in the values of ϵ'' in the range of 0.5–5 and 0.02–0.08, respectively, as seen in Figure 5a–c. At room temperature, ϵ'' and tanδ exhibit the same standard behavior, while ϵ' decreases with all the frequencies. However, the values of ϵ' increase compared to Figure 5a, while ϵ'' and tanδ decrease, as shown in Figure 5d–f. The robust reduction in ϵ' and ϵ'' with the frequency can be described by the Debye relaxation in terms of the polarity alignment and interface effect [8]. Though a great ϵ is significant for high-capacity energy storage dielectrics, the balance between a high dielectric constant and a low dielectric loss is more critical [24].



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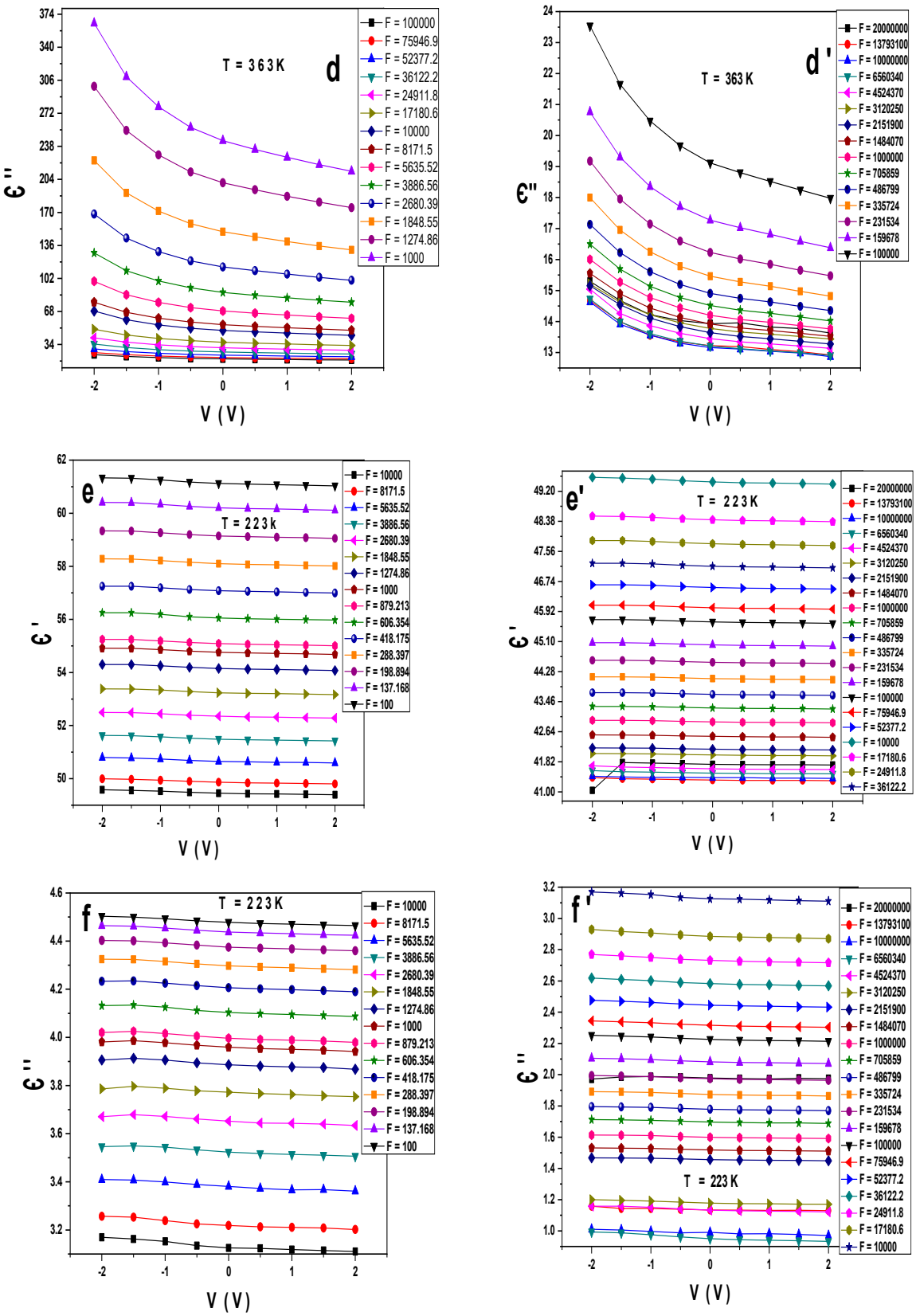
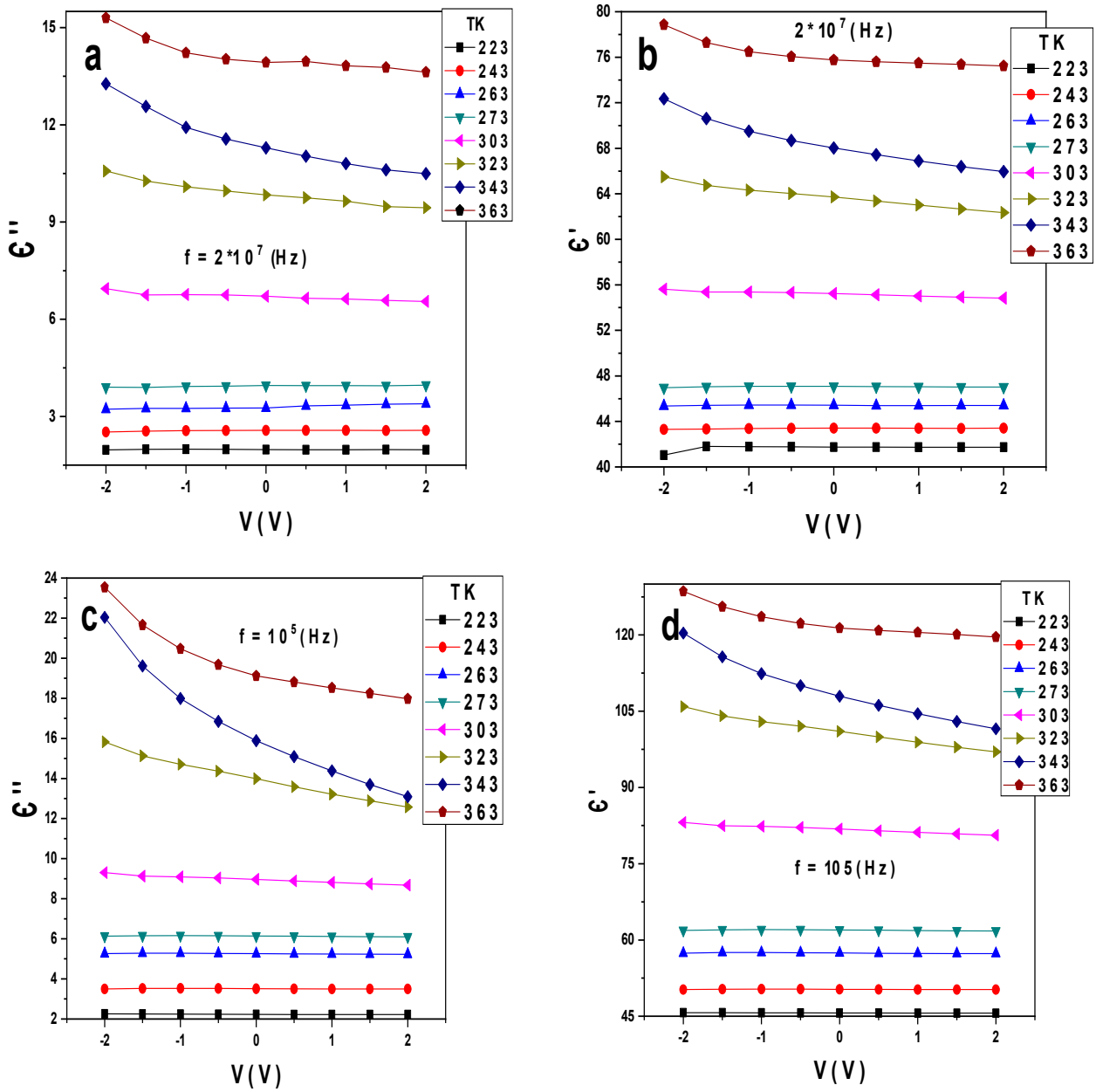


Figure 3. (**a**–**f′**) Є′, Є″ versus V at different frequencies and different constant temperatures for the Au/PVA/SiO_2/p-Si/Al structure.

Figure 6a–f illustrate the variation of Є′, Є″, and tanδ with the temperature at different voltages and frequencies for the Au/PVA/SiO_2/p-Si/Al structure. Є′, Є″, and tanδ increase

with the temperature. All the curves overlap at low temperatures, while at room and high temperatures, the Є′, Є″, and tanδ curves split at each voltage. At the frequency 10^5 Hz, the values of Є′ increase from 40 to 140, while Є″ and tanδ reduce from 0 to 25 and 0.04 to 0.2, respectively, as displayed in Figure 6a–c. As the frequency increases to 2×10^7 Hz, the values of Є′, Є″ and tanδ range from 40 to 80, 0 to 16, and 0.04 to 0.2, respectively, as shown in Figure 6e,f. The impurities, disorders, or additional phases might be clarified in the construction. With an increase in temperature, the joint effect leads to a rise in the values of Є′ and Є″. This may be attributed to the ion jump and space charge effects induced by rising concentrations of the charge carriers. Also, the rising temperature enhances the growth of molecules. It can be supposed that this structure enhanced the dielectric properties Є′, Є″, and tanδ with annealing [25,26]. It is clear that with increasing frequency, Є′ has shown significant improvements, while Є″ and tanδ are decreased, increasing capacitors' ability to store energy and reduce heating loss.



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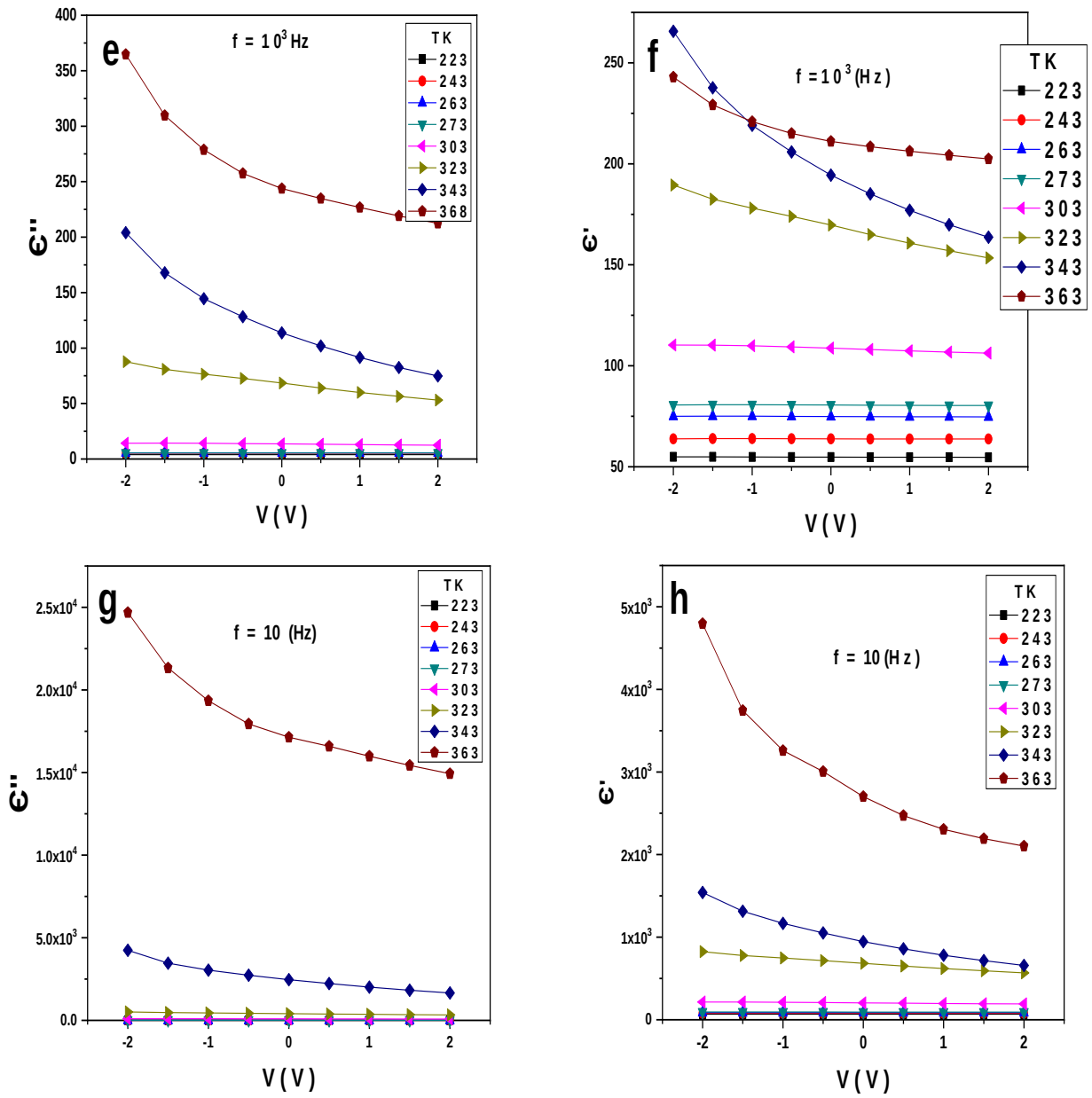

Figure 4. (**a**–**h**) ϵ', ϵ'' versus V at different temperatures and constant frequencies for the Au/PVA/SiO_2/p-Si/Al structure.

Figure 7 displays the variation of the dielectric loss (ϵ'') with a dielectric constant (ϵ') of impedance at different voltages and constant temperatures for Au/PVA/SiO_2/p-Si/Al. Entirely, the figures display a reduction in the radius of the partly shaped semicircles and shrinkage near the origin due to the rising ionic conductivity and declining resistance of the films [27,28].

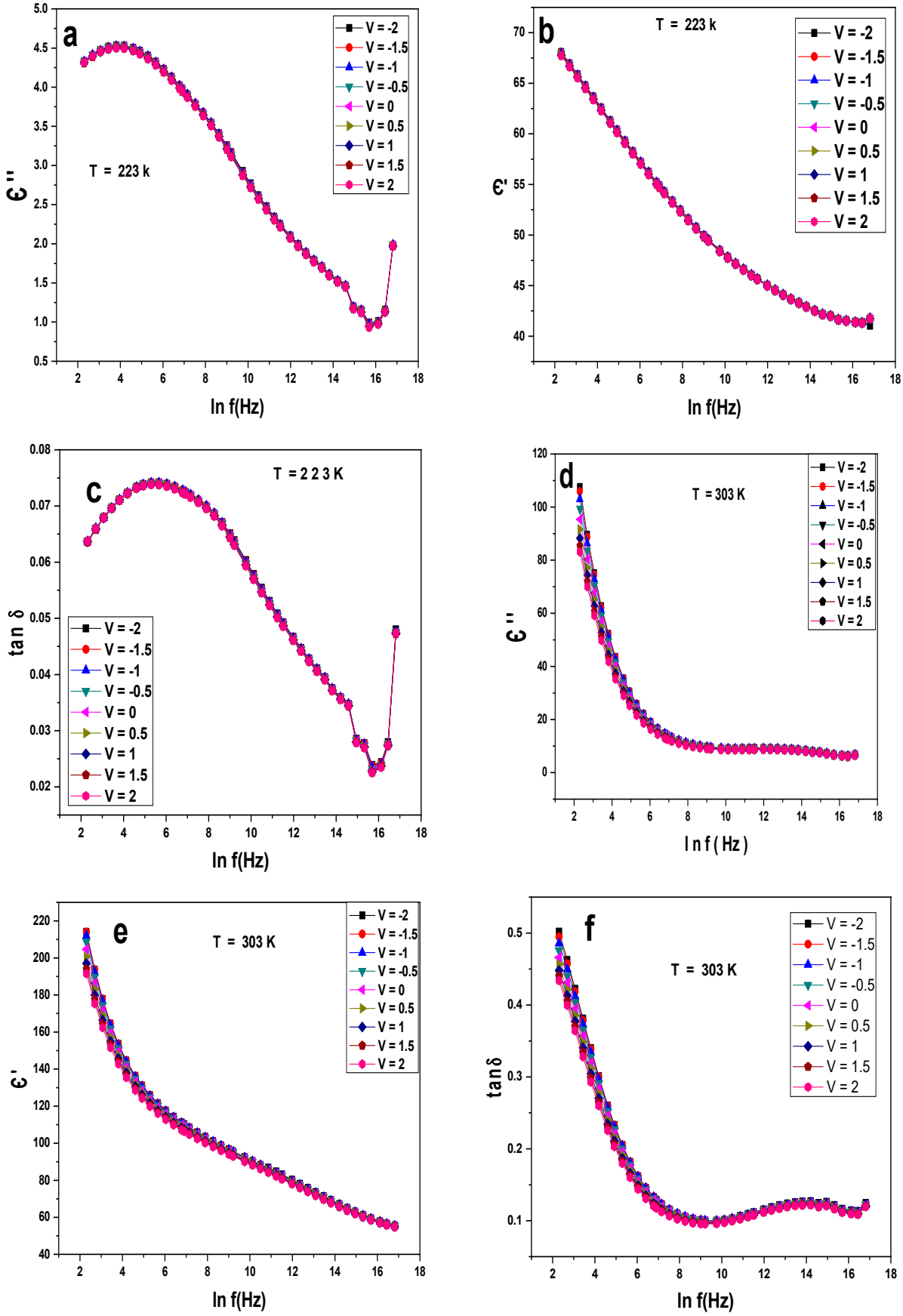

Figure 5. (**a**–**f**) ϵ', ϵ'', tanδ versus lnf at different voltages and constant temperatures for the Au/PVA/SiO_2/p-Si/Al structure.

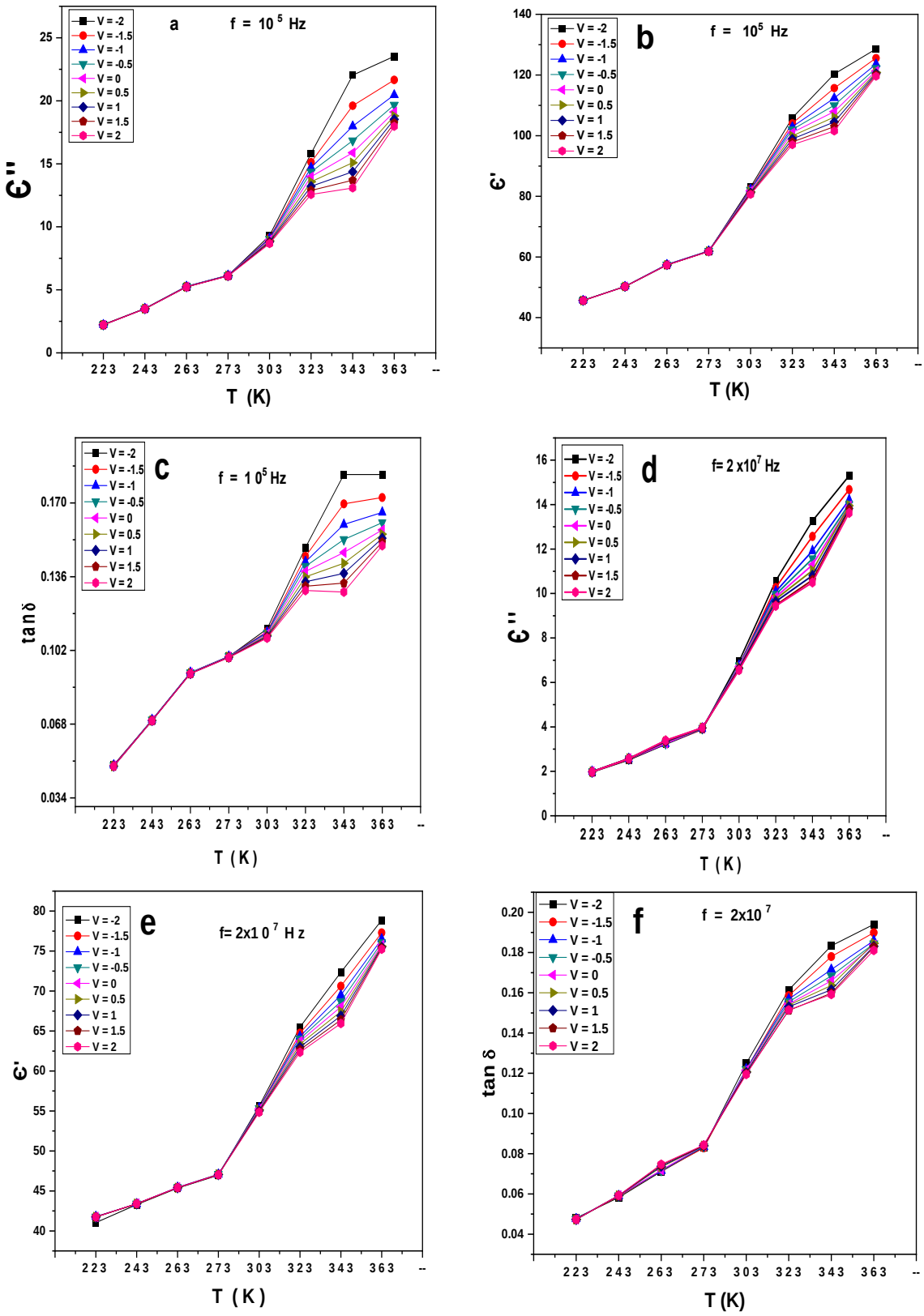

Figure 6. (**a**–**f**) ϵ', ϵ'', tanδ versus Tk at different voltages and constant different frequencies (10^5, 2×10^7 Hz, respectively) for the Au/PVA/SiO_2/p-Si/Al structure.

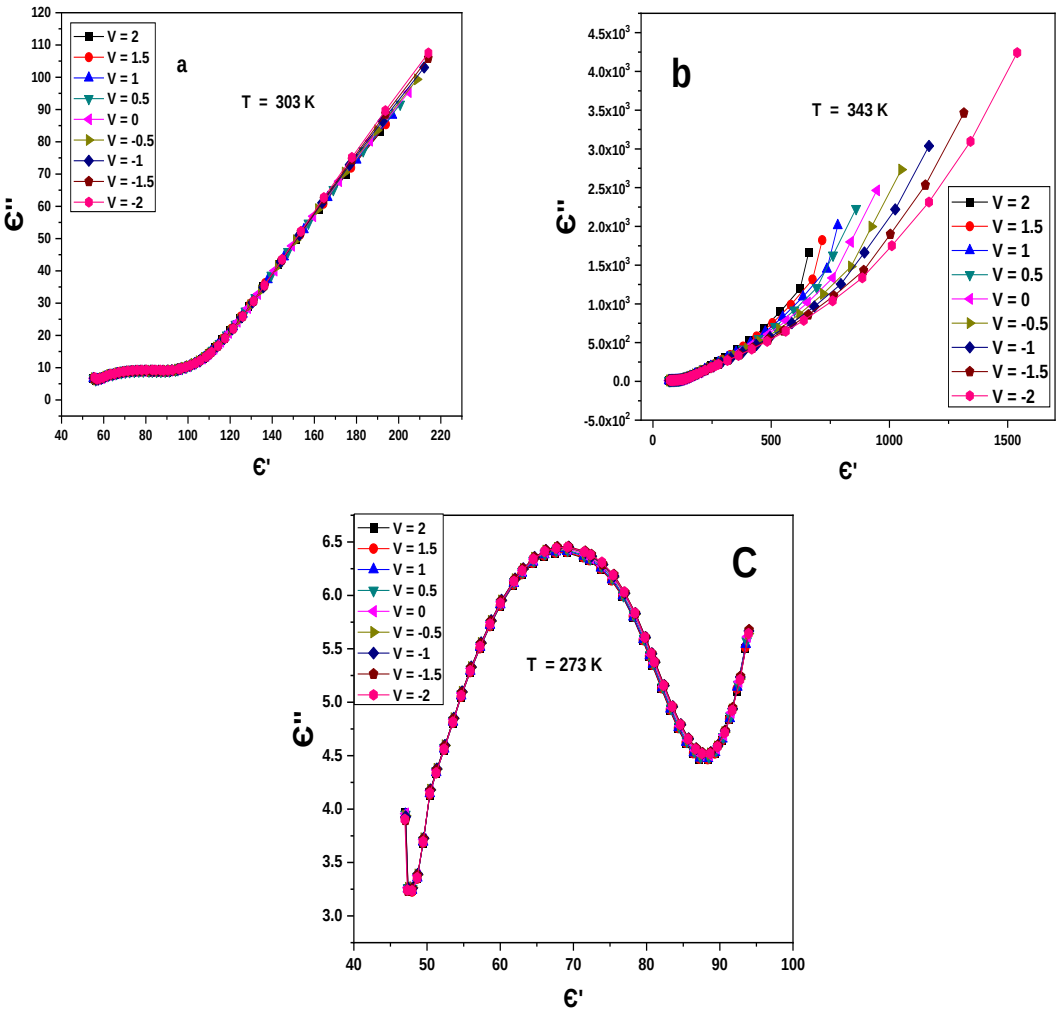

Figure 7. (**a**–**c**) ϵ''-ϵ' at different voltages and constant temperatures for the Au/PVA/SiO_2/p-Si/Al structure.

2.3. The Current–Voltage (I–V) Characteristic

The current–voltage characteristics of the diode were explained according to the thermionic emission model [29–31]:

$$I = I_0\left[\exp\frac{q(V - IR_s)}{nkT}\right] \tag{1}$$

Figure 8a illustrates the I–V characteristic for the Au/PVA/SiO_2/p-Si/Al heterostructure diode at different temperatures, while Figure 8b displays the diode's lnI–V semilogarithmic behavior.

The barrier height can be expressed by [32,33]:

$$\varphi_b = \frac{kT}{q}\mathrm{Ln}\left(\frac{AA^*T^2}{I_0}\right) \tag{2}$$

where I_0 is the saturation current, V is the applied voltage, R_s is the series resistance, n is the ideality factor, T is the temperature in Kelvin, q is the electronic charge, k is the Boltzmann constant, φ_b is the Schottky barrier height, A* is the Richardson constant, and A is the contact area of the diode. The intersection of the inserted straight lines of the linear part with the current axis obtained the I_0. The ideality factor (n) can be determined using Equation (1) as [33,34]:

$$n = \frac{q}{KT}\left(\frac{dV}{dlnI}\right) \quad (3)$$

From Equations (1) and (2), ϕ_b increases with the temperature, while n decreases, as illustrated in Figure 9, and their values are listed in Table 1. Based on Equation (3), the high value of the ideality factor was attributed to the presence of a thin oxide layer and series resistance [23]. Since the non-homogeneous barrier height contributes to the higher value of the ideality factor [35,36], the higher value of n can be explained in terms of secondary mechanisms such as border dips and interfacial imperfections, which are produced by an organic interlayer or a specific border structure [37]. The variation of the barrier height with the ideality factor is illustrated in Figure 10.

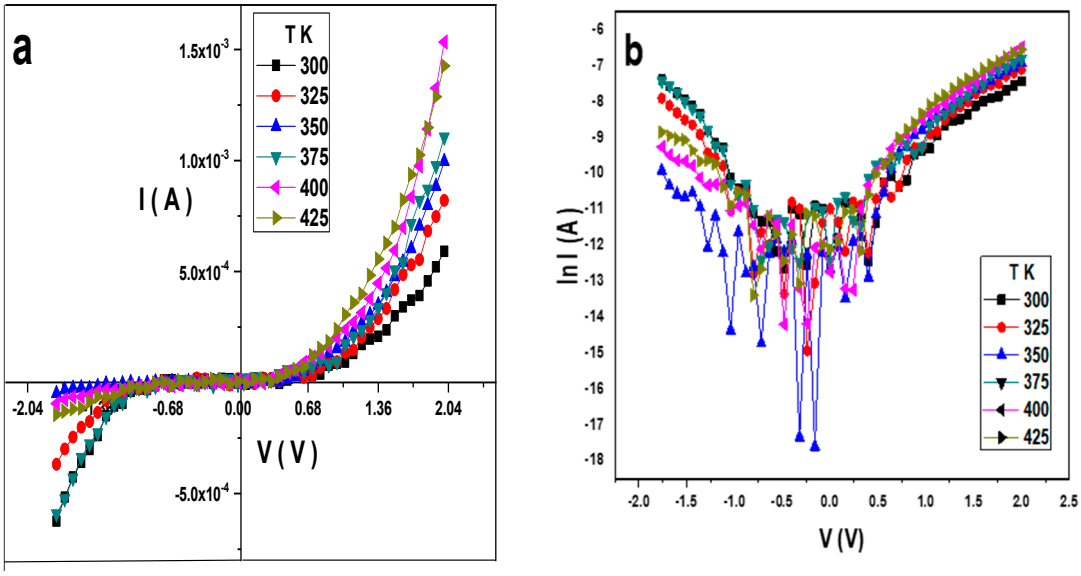

Figure 8. (**a**) I–V, and (**b**) lnI–V at different temperatures for the Au/PVA/SiO_2/p-Si/Al structure.

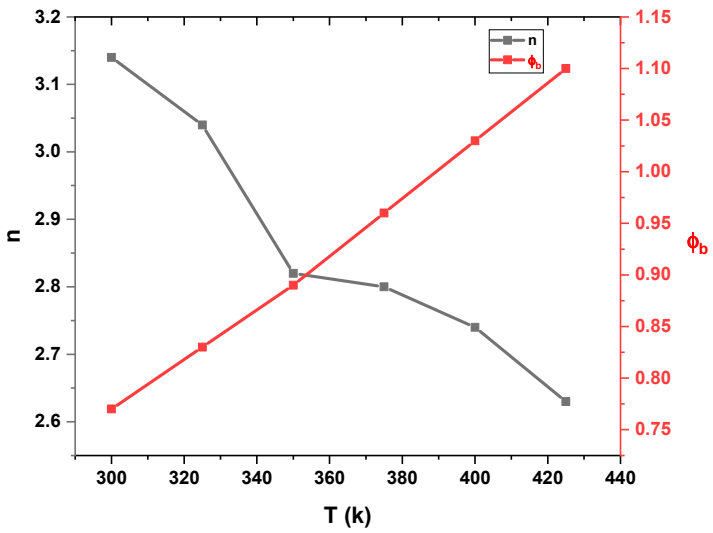

Figure 9. n and ϕ_b versus T for the Au/PVA/SiO_2/p-Si/Al structure.

In addition to that, R_s and R_{sh} decrease with an increasing temperature. As illustrated in Figure 11, R_s and R_{sh} have a significant value due to the thin SiO_2 layer between the PVA and Si layers. The variation of the junction resistance (Rj) with the applied voltage is shown in Figure 12. In contrast, the rectification ratio with a voltage at different temperatures is illustrated in Figure 13. The RR has good values at any temperature, confirming that the diode has a reasonable rectification.

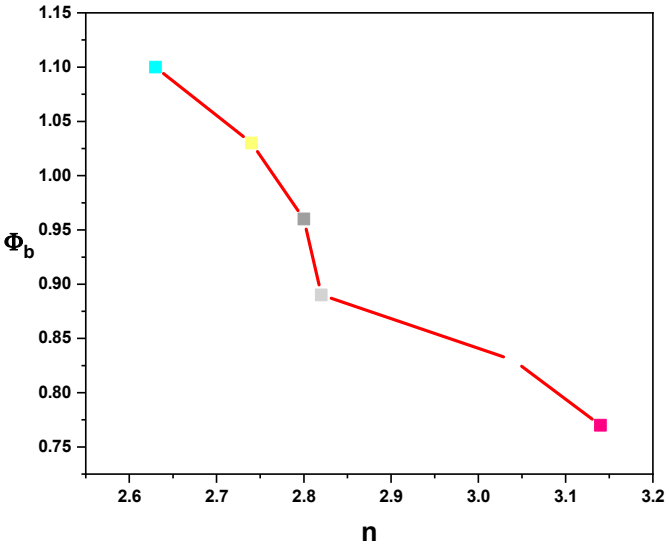

Figure 10. ϕ_b versus n for the Au/PVA/SiO_2/p-Si/Al structure.

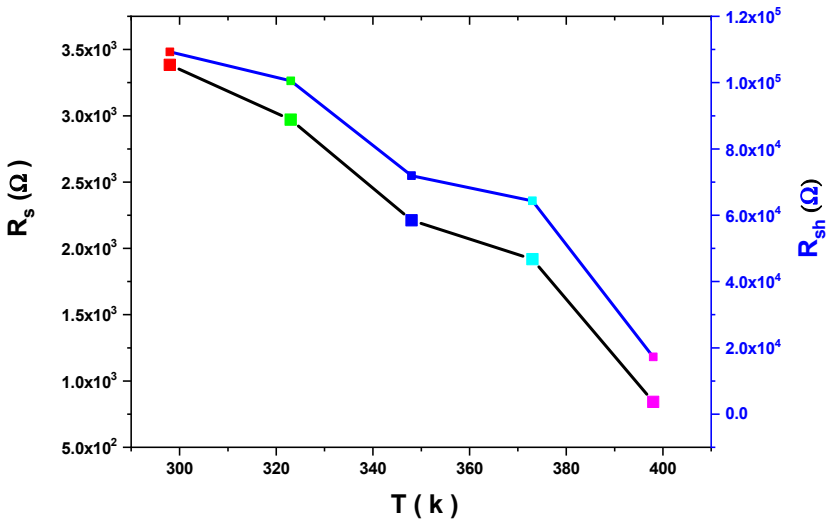

Figure 11. R_s and R_{sh} versus T for the Au/PVA/SiO_2/p-Si/Al structure.

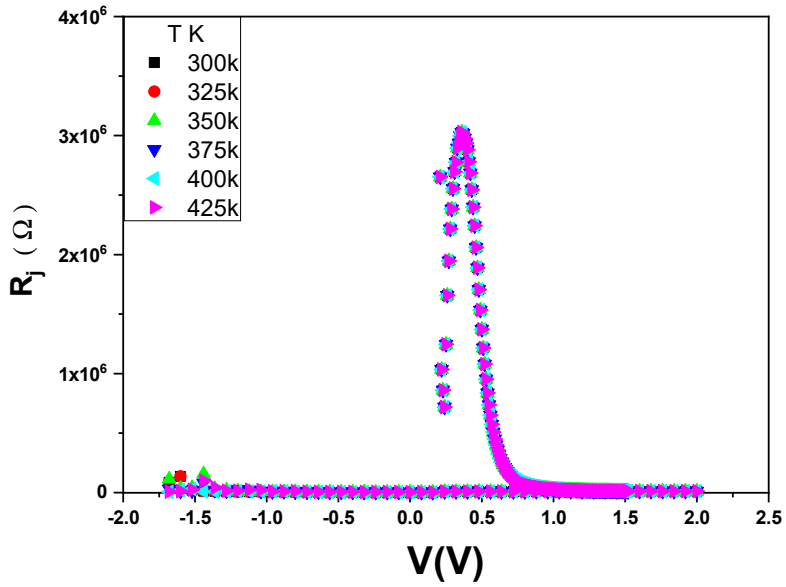

Figure 12. R_j versus V at different temperatures for the Au/PVA/SiO_2/p-Si/Al structure.

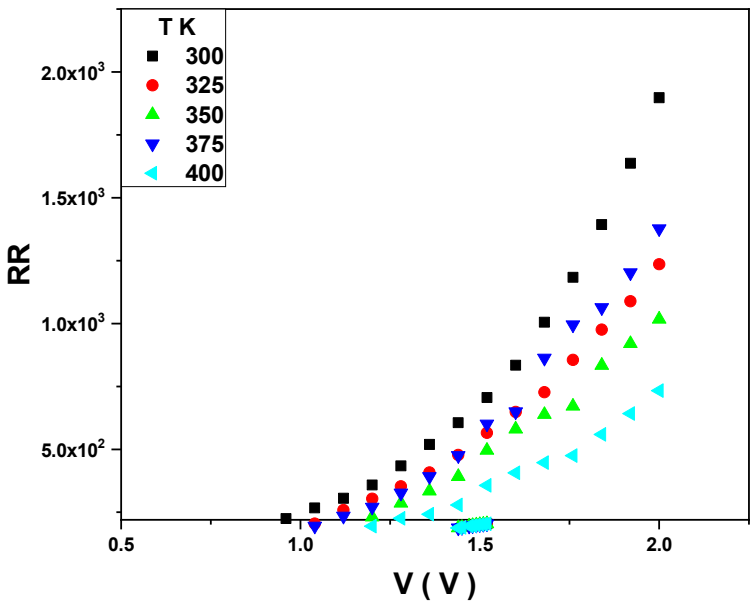

Figure 13. RR versus V at different temperatures for the Au/PVA/SiO_2/p-Si/Al structure.

Table 1. Calculated ideality factor, series resistance, shunt resistance, and Au/PVA/SiO_2/p-Si/Al barrier height at different temperatures.

T (k)	Φ_b eV	R_{sh} Ω	R_s Ω	n
300	0.77	1.09×10^5	3.38×10^3	3.14
325	0.83	1.01×10^5	2.44×10^3	3.04
350	0.89	7.19×10^4	2.01×10^3	2.82
375	0.96	6.43×10^4	1.80×10^3	2.8
400	1.03	1.73×10^4	1.31×10^3	2.74
425	1.1	1.54×10^4	1.40×10^3	2.63

3. Conclusions

In this study, we successfully fabricated an Au/PVA/SiO_2/p-Si/Al structure, which was not previously reported. We investigated the variation of the dielectric constant (ϵ'), dielectric loss (ϵ''), and dielectric tangent (tanδ) across different frequencies, voltages, and temperatures. Our findings demonstrate an increase in the dielectric constant (ϵ') and a reduction in both the dielectric loss (ϵ'') and tangent (tanδ). These results suggest that the Au/PVA/SiO_2/p-Si/Al structure presents new opportunities for advancements in the semiconductor industry, particularly in capacitor manufacturing. Additionally, we systematically analyzed previous studies, examining the undesirable behaviors of ϵ' and ϵ''. Cole–Cole diagrams of ϵ'' and ϵ' under various voltages and temperatures were analyzed. We also performed I–V measurements and assessed electrical parameters such as the ideality factor, series resistance, shunt resistance, rectification ratio, and barrier height at different temperatures.

4. Materials and Methods

The Au/PVA/SiO_2/p-Si/Al was synthesized by cleaning a single crystal wafer of silicon to eliminate all the contamination that exists on the surface. The silicon wafer was left to be oxidized in a furnace at 1170 k for thirty minutes, creating an oxide layer (SiO_2). An aqueous gel solution of PVA was deposited on the surface of the SiO_2/Si using the spin-coating technique. The Au/PVA/SiO_2/p-Si/Al heterostructure was left to dry at a temperature of 223 k, and then a gold electrode was deposited on the top and aluminum as a lower electrode of the structure of the Au/PVA/SiO_2/p-Si/Al using thermal evaporation.

Author Contributions: Conceptualization, A.A. and A.E.H.G.; Validation, A.A., A.E.H.G. and M.A.B.-M.K.; Formal analysis, A.E.H.G.; Investigation, G.M.T. and M.A.B.-M.K.; Resources, G.M.T.; Writing—original draft, A.E.H.G., G.M.T. and M.A.B.-M.K.; Writing—review & editing, A.A. and M.A.B.-M.K.; Visualization, A.A., A.E.H.G., G.M.T. and M.A.B.-M.K. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

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