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Design and Simulation of Linear All-Optical Comparator Based on Square-Lattice Photonic Crystals

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Abstract: An optical comparator is an important logic circuit used in digital designs. Photonic crystals are among the platforms for implementing different kinds of gates and logic circuits, and they are structures with alternating refractive indices. In this paper, an optical comparator is designed and simulated based on a square lattice photonic crystal. In the design of this comparator, a small-sized structure is used. The simulation results show that in the proposed comparator, there is a high difference between logical values “0” and “1”, which are defined based on the optical power level. Due to the small size of this comparator and the adequate difference between logical values “0” and “1”, this structure suits photonic integrated circuits with high accuracy. The proposed structure footprint is 149.04 μm^2 , and the calculated rise time for this circuit is less than 0.4 ps.

Keywords: optical comparator; photonic crystal; defect; photonic bandgap



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1. Introduction

Electrons are considered the charge carriers in electronic circuits. In these circuits, a transistor serves as the base part. In other words, all circuits are designed using transistors. Since the movement of electrons in transistors is determined by the size of this part, the speed of the transistor circuits is limited by the size of the transistors [1–4]. If electronic parts are replaced with optical parts, the photons play the role of charge carriers. Given the high speed of photons, if optical parts are used, their speed will increase drastically. Therefore, it is better to use optical circuits to design high-speed integrated circuits [5–9].

Photonic crystals are among the platforms that suit the design of optical circuits. One of the reasons for paying more attention to this structure is that it is possible to design different types of circuits using photonic crystals. Many logic gates have been designed with photonic crystals [10–17]. Moreover, many logic circuits such as adders, subtractors, decoders, encoders, and de-multiplexers have been designed [18–26]. The two-bit comparator is among the logic circuits. This circuit compares two bits. Very few studies have been conducted on the design of optical comparators with photonic crystals [27–34].

Recently, several papers have been penned on the design of comparators. In 2017, Rathi et al. designed a small-sized structure for an optical comparator based on square-lattice photonic crystals. This paper shows that the structure can act as a comparator using optical power distribution, and the output values are not determined quantitatively [27]. In 2018, Fakouri-Farid et al. used a square-lattice photonic crystal structure to design a comparator. The difference between the high and low logical values was acceptable in this comparator, but the size of the structure was extremely large. Moreover, due to the use of a ring resonator in the structure, the delay time of the circuit is increased [28].

Another comparator was designed by Serajmohammadi et al. in 2019. In this paper, the difference between the high and low logical values was satisfactory, but the circuit

size was large, and a ring resonator was used [29]. Another structure was designed by Surendar et al. in 2019. In this structure, three ring resonators with non-linear rods having several point defects were used. The design of this structure seems difficult due to its large dimensions as well as the use of non-linear rods of different sizes [30].

A comparator was also designed in 2019 by Jalali et al. This structure also consists of four ring resonators, which increase the circuit size and the circuit delay time [31]. In 2020, Seraj et al. designed a comparator based on photonic crystals. Despite the small size of this structure, the difference between the high and low logical values is not appropriate [32].

In 2019, Zhu et al. designed a one-bit comparator by using nonlinear ring resonators [33]. The use of five nonlinear ring resonators has complicated the structure. This photonic crystal structure has a long delay time due to the use of many rings and has a large footprint.

Another photonic crystal structure for digital comparators was proposed by Jile in 2020 [34]. The structure consisted of two ring resonators with several waveguides, which is one of the disadvantages of this structure. Moreover, two control sources were used, which caused high power loss in this structure [34].

In this paper, a photonic crystal structure with a square lattice was used to design an optical comparator. In the design of this structure, we tried to select a small comparator size. Moreover, in this structure, the difference between the logical values "0" and "1" was also considered. Furthermore, we tried to avoid using ring resonators to create a high-speed structure. Therefore, the circuit delay time was reduced, and its speed was increased.

This research's proposed comparator design method is as follows, which is first considered a two-dimensional photonic crystal structure. Then, by creating linear defects as well as the number of point defects, the structure was changed so that it could be used as a comparator. The proposed structure uses two main inputs, a reference input (Ref), and three outputs.

In this research, RSoft software was used to simulate the structure. In the next step, we changed the rods in the path of the waveguides. This change included changing the radius of the rods as well as changing the position of the rods. After the simulation for these modes, we determined the best outputs. The phase difference between the input waves and the Ref source was also used to optimize the results. Then the best structure for the comparator was proposed, the simulations were performed, and the results were obtained.

2. Design of Optical Comparator

We first selected a photonic crystal structure with a square lattice and a small size to design this comparator. Then we created waveguide paths using linear and point defects. That is, some rods in the waveguide paths were considered defective rods. To optimize the structure, we changed the defect rods' radius and position. For the proposed design, simulations were performed for different values of the radius of the rods and their position. Then the obtained optimal state was given as the final structure.

A basic photonic crystal structure consisting of silicon rods with a circular cross-section in the air context was used to design the comparator. There were 24×19 rods that formed a two-dimensional square lattice, and the footprint of this structure was $149.04 \mu\text{m}^2$. The refractive index of the rods is 3.46, which was designed for approximately $1.55 \mu\text{m}$ wavelength. The lattice constant, which is the distance between the centers of the rods, was set to $=0.6 \mu\text{m}$ for this structure. The radius of the silicon rods was also $r = 0.2a$.

This alternating structure led to creating an attribute called the photonic band gap (PBG). Based on this attribute, the propagation of a range of wavelengths in the structure was not allowed. The band structure calculations were also used to calculate this wavelength range. The plane wave expansion (PWE) method was used to calculate the band structure. Figure 1 depicts the results of the band structure calculations.

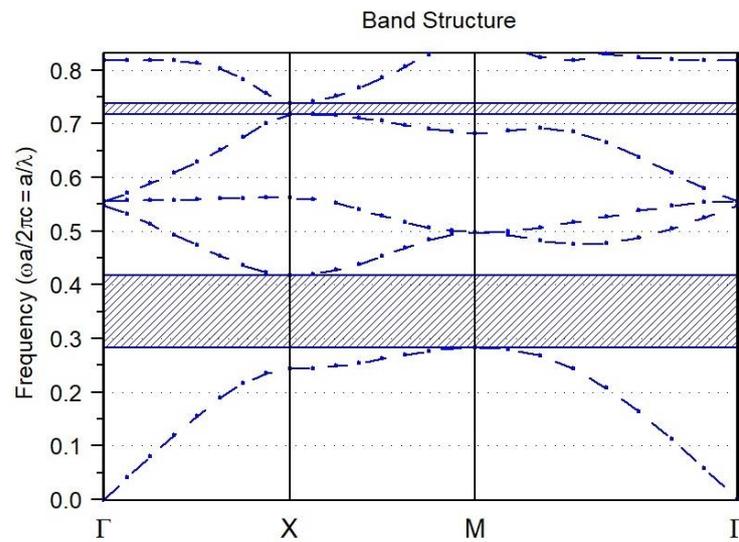


Figure 1. PBG range for the basic structure.

Figure 1 shows that the photonic crystal structure has two ranges of PBG. PBG is the range through which all of the wavelengths of the band cannot cross the crystal structure. In other words, these wavelengths are reflected after colliding with the structure. The light sources used must have a wavelength in the PBG range so that they can be propagated in the waveguide paths and propagated in the same path and not propagated in all parts of the structure.

As seen in Figure 1, no wavelength can enter the structure in the 0.28 to 0.42 normalized range. Since the normalized values are defined as $\frac{a}{\lambda}$, the equivalent wavelength for this range is $1.42 \mu\text{m} < \lambda < 2.14 \mu\text{m}$. Hence, this wavelength has to fall within the PBG range to select a suitable wavelength that can be controlled and directed in the structure. The $1.55 \mu\text{m}$ is selected as the operating wavelength, which is within the aforementioned range.

A combination of linear and point defects was used to obtain the optical comparator. The A and B inputs were placed on the top and bottom of the structure, and a constantly activated input called Ref was also placed on the left side of the structure. When both inputs were off, the output for their equality had to be activated; the Ref input served this purpose. Moreover, to improve the structure performance, reference Ref had a -70° phase shift in relation to the two input references. Three outputs were also selected for three possible states, which included $A < B$, $A = B$, and $A > B$. The outputs of these three states also included F1($A < B$), F2($A = B$), and F3($A > B$). Figure 2 depicts the arrangement of the inputs and outputs and the link between their paths.

As seen in Figure 2, linear defects were used to obtain the comparator and create the input and output paths. These defects were created by omitting all of the rods. Point defects were also used at the intersection of the waveguide paths. The radius of the rods was changed for the point defects. Figure 2 shows the size of the radius of these rods. Some of the rods were also displaced as follows to improve comparator efficiency.

1. Rods with R1 and R2 radii: 0.2a rightward and 0.3a upward.
2. Rods with R3 radii: 0.3a rightward and 0.2a upward.
3. Rods with R4 radii: 0.3a rightward and 0.6a upward.
4. Rods with R5 radii: 0.2a upward.
5. Rods with R6 radii: 0.2a downward.
6. Rods with R7 radii: 0.3a rightward and 0.6a downward.
7. Rods with R8 radii: 0.3a rightward and 0.2a downward.
8. Rods with R9 and R10 radii: 0.2a rightward and 0.3a downward.
9. Rod a: 0.6a rightward and 0.1a upward.
10. Rod b: 0.5a rightward.
11. Rod c: 0.6a rightward and 0.1a downward.

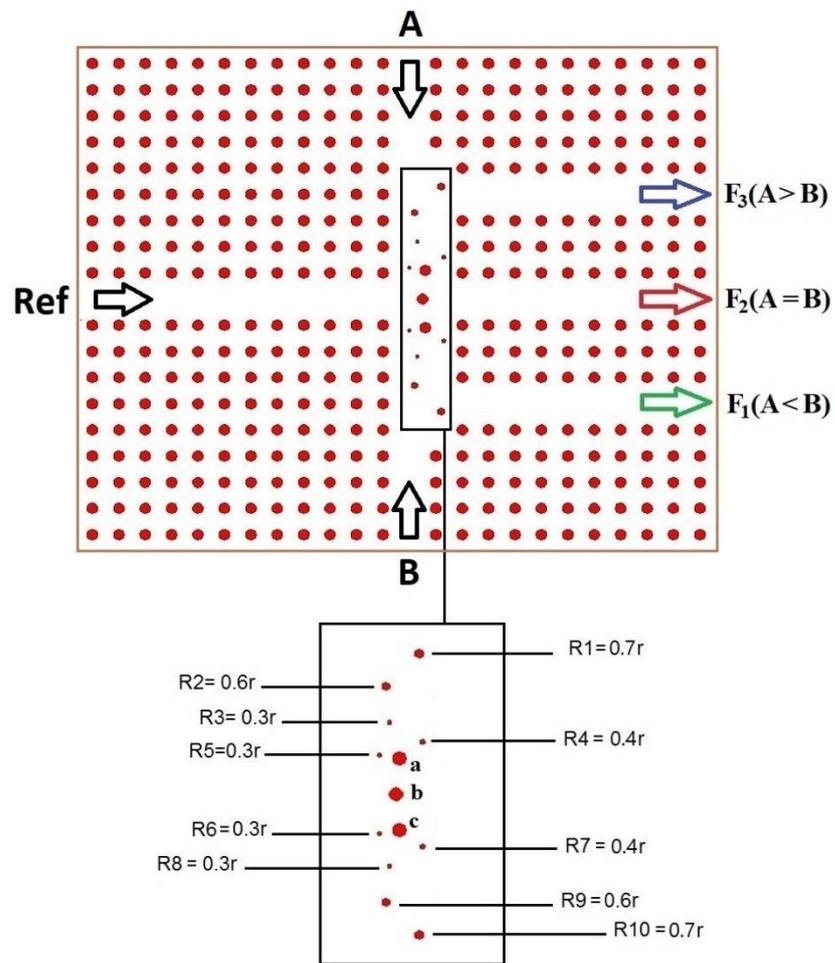


Figure 2. The proposed optical comparator structure.

3. Simulation Results

As mentioned, to achieve the best outputs, the position and size of the defect rods were changed. Phase differences between incoming light waves can also be used to optimize the output response. We used simulations to achieve the best phase difference. Figure 3 shows the results of these simulations.

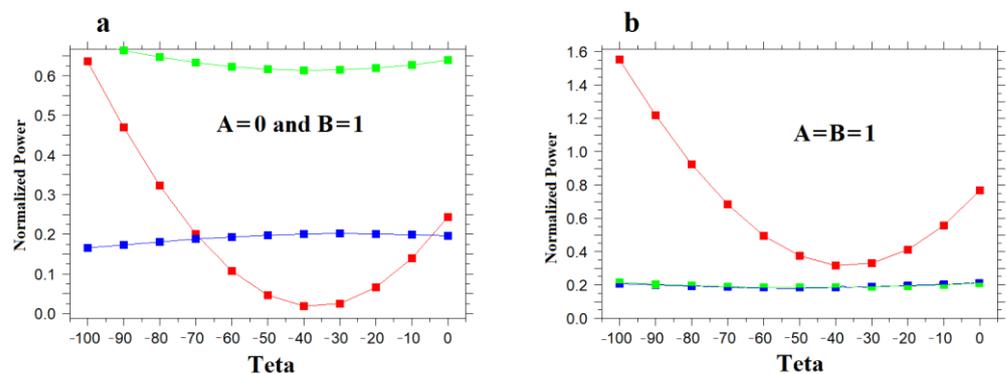


Figure 3. Diagram of output power changes in terms of phase difference changes (a) $A \neq B$ and (b) $A = B = 1$.

Figure 3 shows that if the Ref optical wave has a phase difference of -70 degrees relative to the input sources, the comparator will perform best. Due to the circuit symmetry, the $A = 1$ and $B = 0$ mode is the same as $A = 0$ and $B = 1$.

The comparator was simulated in four input states, and the optical power distribution in the structure was obtained in these states. Figure 4 shows the simulation results. Figure 4a shows power distribution for $A = B = 0$. As seen in this figure, the F2 output had considerable optical power, and it could be considered the equivalent to the logical value “1”. The optical power in the output was supplied by the reference (Ref) input source.

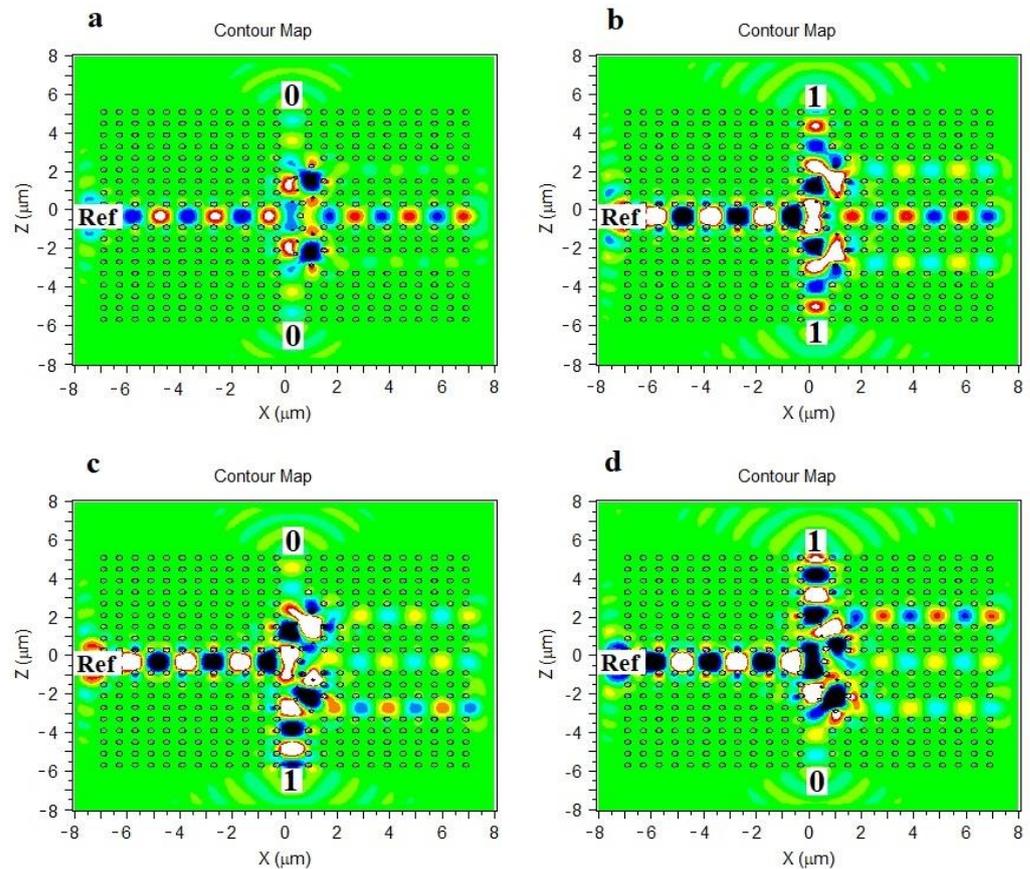


Figure 4. The optical power distribution of the comparator in different input states. (a) $A = B = 0$, (b) $A = B = 1$, (c) $A = 0$ and $B = 1$, (d) $A = 1$ and $B = 0$.

In this state, the decrease in power in the outputs is caused by the interference of the waves emitted from the inputs and Ref input at the intersection, while optimal power is only distributed along path F2 after colliding with the rods and the power level is very low in the other outputs. Figure 4b depicts the optical power distribution for $A = B = 1$. In this case, the output of F2 has a high power, and the other two outputs have a power close to zero.

Figure 4c shows the results when the inputs are $A = 0, B = 1$. Since in this state $A < B$, the F1 output is expected to be in the “1” state, and the other outputs are zero. As seen in this figure, the power distribution in the F1 output is significant and is equal to the logical value “1”.

If the inputs are $A = 1, B = 0$, i.e., $A > B$, the F3 output has to have high optical power, and other outputs have to have very low power due to the symmetry of the circuit. Figure 4d confirms this state. In other words, F3 equals logical value “1”, and the other outputs are in the “0” state.

Figure 5 presents the time curve of the variations of the optical power range in the comparator outputs. As seen in this figure, when $A = B = 0$, the normalized power in the F2 output equals 0.67, and power in the other two outputs equals 0.01. In other words, the F2 output equals the logical value “1”. In addition, when $A = B = 1$, the power in the F2

output equals 0.70, while in other outputs, it is equal to 0.17. In other words, in this state, F2 equals the logical value “1” (see Figure 5a,b).

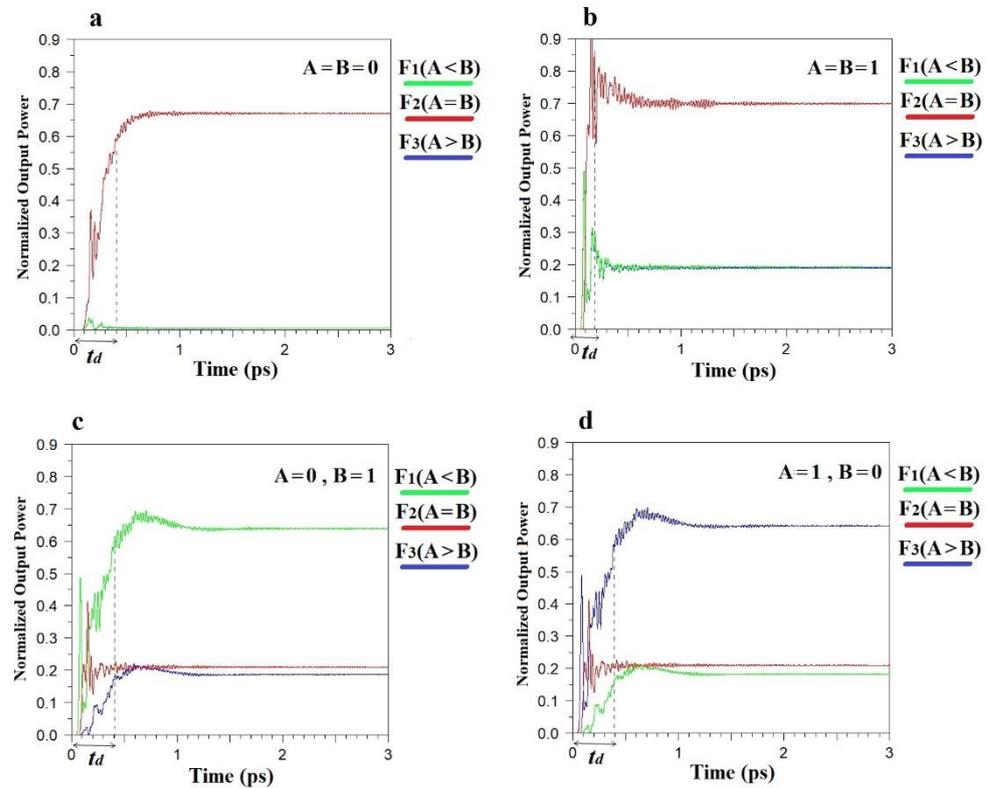


Figure 5. The normalized power diagram in the comparator outputs for different input states. (a) $A = B = 0$, (b) $A = B = 1$, (c) $A = 0$ and $B = 1$, (d) $A = 1$ and $B = 0$.

Figure 5c shows the normalized power diagram in the outputs of the comparator circuit for $A = 0$ and $B = 1$. In this state, the optical power in the F1 output is 0.66, which equals the logical value “1”. In the other two outputs, power equals 0.20, which equals the logical value “0”. The normalized power diagram for $A = 1$, $B = 0$ is also shown in Figure 5d. As seen in this figure, power in the F3 output, which has to be in the logical state “1”, equals 0.66, while in the other outputs, the optical power is low and equals 0.20.

As shown in Figure 5, in the worst case, the time required for the output to reach a steady state is less than 0.4 ps.

One of the important parameters in optical logic circuits is the contrast ratio (CR). This parameter is used to show the power difference in the two logic states, 0 and 1. This parameter is defined as $CR = 10 \log(P_{1,min}/P_{0,max})$ where $P_{1,min}$ is minimum power in logic 1 and $P_{0,max}$ is maximum power in logic 0. In other words, the worst value is considered for all possible modes. According to Figure 5, this value can be calculated for all three outputs. For output F1 this value is equal to $CR = 5.2$ dB. Furthermore, for F2 and F3 outputs, these values are equal to 5.3 dB and 5.2 dB, respectively.

Delay time is another important parameter in digital circuits. If this time is defined as the time required for the output to reach 10% of the steady-state value, the delay times can be calculated for all four states shown in Figure 5. The delay time for $A = B = 0$ is 0.12 ps. This time for mode $A = B = 1$ is approximately equal to 0.1 ps. Moreover, in the case of $A = 0$, $B = 1$ this time is equal to 0.1 ps. Finally, the delay time at $A = 1$, $B = 0$ is approximately equal to 0.1 ps.

Several new articles were reviewed, and their results were compared to compare the proposed structure with previous studies. Table 1 shows the results of this comparison. It is worth noting that very few studies have been conducted on photonic crystal comparators. In Table 1, the size of this structure is compared to other papers. In addition, the worst

value of each output in the “0” and “1” logical value states, i.e., the maximum power for “0” and the lowest power for “1”, are shown in this table and are compared to other structures.

Table 1. Comparison the proposed comparator with other works.

References	Size	F1 “1”Min Power	F1 “0”Max Power	F2 “1”Min Power	F2 “0”Max Power	F3 “1”Min Power	F3 “0”Max Power	Rise Time (ps)
[28]	86 × 49	0.85	0.06	0.85	0.08	0.90	0.05	3.0
[29]	100 × 74	1.4	0.05	0.80	0.00	1	0.05	3.0
[30]	65 × 31	0.91	-	0.90	-	0.83	-	1.5
[31]	121 × 37	0.71	0.10	0.89	0.20	0.75	0.25	2.5
[32]	13 × 13	0.47	-	-	0.11	0.80	0.14	0.31
[33]	80 × 41	0.88	0.08	0.75	0.04	0.78	0.03	1.5
[34]	77 × 111	0.90	0.20	0.90	0.20	0.98	0.02	0.6
This Work	24 × 19	0.66	0.20	0.67	0.2	0.66	0.20	0.4

As seen in Table 1, in references [28–31,33,34], the circuit size is large and does not suit the photonic integrated circuits despite the highly satisfactory “0” value. In reference [30], the values of “0” are not reported and the values of “1” are good logical values, but the circuit size is large. In reference [31], the logical value “0” is high, and the structure is also large. Finally, in reference [32], the structure is small, but two outputs are used simultaneously to compare the inputs. The value “1” in this circuit is also weak.

In these circuits [28–34], the logical values (“0” and “1”) and the structure size are not optimized, but in our proposed comparator, the circuit size is small, while the high difference between the two logical values is also taken into account. It can also be seen that the rise time is very low in the proposed structure and can be used in high-speed optical integrated circuits. Another feature of this structure is the simplicity of designing and using very few waveguides. Furthermore, no nonlinear rods are used in this structure, and all rods are homogeneous. In addition, only one control source has been used in the design of this structure. These features make its design and fabrication easier.

4. Conclusions

In this study, a one-bit comparator is designed and simulated. This circuit can compare two input bits and put one of the three outputs in the logical state “1”. One of the characteristics of the designed structure is its small size, which makes the comparator suitable for photonic integrated circuits. Moreover, the distance between two logical values is considered in designing the comparator to ensure the distance is relatively good. Another characteristic of this circuit is its simple design, which involves simple linear and point defects and does not include resonators that increase the circuit delay time.

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