

Article

A 60 μm -Long Fiber-to-Chip Edge Coupler Assisted by Subwavelength Grating Structure with Ultralow Loss and Large Bandwidth

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Abstract: Efficient fiber-to-chip coupling is a key issue in the field of integrated optics and photonics due to the lack of on-chip silicon light source at present. Here, we propose a silicon-based fiber-to-chip edge coupler by use of subwavelength grating (SWG)-assisted structure. The key conversion region is composed of a trident-shaped SWG in the center and two matched strip waveguides on both sides. To achieve high mode match between fiber mode and silicon waveguide mode and to realize low-loss transmission on-chip, we have divided the conversion region into three parts and determined their optimum dimensions. From results, the total device length is only 60 μm from input fiber to output silicon waveguide, and the insertion loss (IL) is as low as 0.23 dB at the wavelength of 1.55 μm . For the working bandwidth, its value can be enlarged to 240 nm (or 390 nm) by keeping IL < 1 dB (or 1.5 dB), which is quite promising for on-chip broadband devices. Based upon these advantages, we hope such a device could be applied in light coupling between optical fiber and on-chip silicon waveguide.

Keywords: fiber-to-chip coupler; subwavelength grating structure; photonic integrated components



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1. Introduction

Silicon photonics has greatly pushed the development of integrated optics and provided an excellent technique to make on-chip optical circuits available, where the application fields of optical communications, optical interconnects, and data centers are benefited significantly [1–5]. Silicon-on-insulator (SOI), a vital and promising platform for silicon photonics, has attracted tremendous interest to realize compact, high-yield, and energy-efficient photonic integrated circuits (PICs) due to its high refractive-index-contrast and complementary metal-oxide-semiconductor (CMOS) processing [6–9]. Based on such a material platform, the typical size of a single-mode silicon waveguide is only 220 nm \times 450 nm, which poses a huge challenge for efficient light coupling between optical fiber and silicon waveguide since the mode field diameter (MFD) of single-mode fiber (lensed fiber) is about 10 μm (4 μm) [10–12]. Therefore, high-performance fiber-to-chip couplers with features of broad bandwidth, low coupling loss, and compact size are our pursuit goals.

To satisfy these requirements, different coupling structures have been proposed which can be classified as two types, surface grating couplers [13,14] and edge couplers [15,16]. The surface grating coupler is a periodic structure on the waveguide that diffracts the injected waveguide mode according to the phase matching condition, and then the diffracted light wave will be further collected by an aligned optical fiber [13]. We should note that such a process is also reversible, corresponding to fiber-to-chip coupling. Owing to the flexibility in use of the grating coupler, it has been employed as the main input and output couplers for wafer-level device testing at present with advantages of compact size and being able to choose arbitrary design position on the fabrication layout. However, the grating coupler also

has obvious drawbacks, e.g., narrow working bandwidth, low coupling efficiency (or large coupling loss), incident angle dependence, and polarization dependence, all of which are derived from the intrinsic phase matching requirement of the grating coupler [13,14,17]. By contrast, the edge coupler works as a mode evolution method where the injected light from the optical fiber is gradually coupled to the silicon waveguide through inverse tapers [15,16,18]. Thus, the abovementioned drawbacks of grating couplers can be well-addressed since the phase matching condition is no longer required. On the other hand, the mode evolution mechanism also enlarges the conversion length inevitably, making the total length of edge coupler larger than 300 μm [15]. Therefore, new waveguide structures need to be developed in order to efficiently shorten the conversion length of the edge coupler as well as to achieve broad bandwidth and reduced coupling loss.

Compared with conventionally used single-layer silicon inverse tapers for the fiber-to-chip edge coupler [19], multi-layer taper schemes have been proposed. For example, by depositing an extra silicon nitride waveguide layer atop the silicon inverse taper sandwiched by a silicon dioxide spacer layer, the optical fiber mode can be guided through a silicon nitride waveguide and further adiabatically transferred to the bottom silicon waveguide through inverse taper structure. Using standard CMOS compatible fabrication procedures, the coupling loss from lensed fiber (MFD: 4.1 μm) to silicon waveguide (width: 440 nm) was measured to be only 0.25 dB/0.51 dB for TE/TM mode at 1550 nm, and the allowable bandwidth exceeded 60 nm with a coupling loss lower than 0.7 dB for both polarizations [20]. Meanwhile, the key silicon inverse taper length was already 300 μm and the total conversion length would be even longer. To enhance the mode field match between optical fiber and coupler facet, multiple silicon nitride waveguides at different layers have been suggested, but the required multi-stage waveguide tapers make the total device length quite long (e.g., 895 μm [21], 300 μm [22]). Furthermore, the fabrication steps and complexities of such a scheme were obviously increased. These reported multi-layer taper schemes are mainly using silicon nitride waveguides located in the upper cladding region of the silicon waveguide as bridges to efficiently connect optical fiber mode and silicon waveguide mode at different thick levels. If we want to make the light coupling between optical fiber and on-chip silicon waveguide directly without assistance of other intermediate waveguides (e.g., silicon nitride waveguides [20–22]), the mode field mismatch between optical fiber and silicon inverse taper should be reduced as far as possible. Under such conditions, Jia et al. removed the buried oxide (BOX) layer below the silicon inverse taper and formed a suspended silicon inverse taper for the fiber mode coupling, where the measured coupling loss was lower than 1.3 dB for both polarizations [23]. However, the mechanical strength and stability of the suspended structure might pose challenges for on-chip applications. Recently, a subwavelength grating (SWG)-assisted edge coupler was proposed and the total conversion length was reduced to less than 100 μm , which is quite promising for on-chip compact integration [24–28]. However, the obtained fiber-to-chip coupling loss (e.g., 1–2.5 dB [26–28]) and working bandwidth (e.g., less than 150 nm [26–28]) still need to be reduced and increased, respectively, which could help generate the ideal on-chip fiber-to-chip edge coupler.

In this paper, we present an ultralow-loss and large-bandwidth fiber-to-chip edge coupler based on the standard SOI wafer with a 220 nm-thick top silicon layer and a 2 μm -thick BOX layer. The conversion region is formed by a trident-shaped SWG in the center and two matched strip waveguides on both sides along the propagation direction, where different linear taper structures have been employed to reduce the coupling loss. The trident-shaped SWG structure, acting as a homogenous medium, is employed to efficiently match the input fiber mode first and then gradually convert to the silicon waveguide mode, where the coupling interface between optical fiber and proposed edge coupler has been optimized to enhance the coupling efficiency and a tapered SWG structure is employed to reduce the coupling loss. By further adding two matched strip waveguides on both sides of the central SWG waveguide, the coupled mode could be well-confined in the tapered SWG region and further converted to the silicon waveguide via SWG-wire tapered transition waveguide, where the employed matched strip waveguides are beneficial to further reduce

the coupling loss. From results, we have obtained an ultralow insertion loss (IL) of 0.23 dB at 1550 nm and the working bandwidth can be extended to 390 nm (240 nm) by keeping $IL < 1.5$ dB (1 dB), which could well support the broadband operation of on-chip silicon devices. Note that the total conversion length of the proposed edge coupler is only 60 μm , which is quite short compared to some previous reports [20–22,26,28]. Therefore, we believe such a fiber-to-chip edge coupler will be very beneficial for low-loss, broadband, compact light connection between optical fiber and on-chip silicon waveguide, and will also push the development of silicon photonics.

2. Materials and Methods

Compared with some inverse tapers used for the fiber-to-chip edge coupler, their waveguide structures are normally silicon strip waveguides whose mode effective indices and field distributions are determined by the waveguide dimensions. By contrast, the recently reported SWG structures that can suppress diffraction effects and behave as homogeneous media offer a new design degree of freedom for photonic devices, since the mode effective index can be easily engineered by changing the grating duty cycle [24,25]. Here, we will take full advantage of the SWG structure and combine its low-loss and broadband features into the fiber-to-chip edge coupler.

Figure 1 shows the schematic of the proposed fiber-to-chip edge coupler. The key conversion region is composed of one trident-shaped SWG in the center and two matched strip waveguides on both sides along the propagation direction (x -direction). As the light launches into the edge coupler from the lensed fiber, it is firstly coupled and guided by the trident-shaped SWG to reduce the mode size, where the tip widths at the interface side are set as W_1 (=120 nm) and W_2 (=160 nm) with a gap width of g_1 between them and the coupling length is L_1 (part 1), respectively. At the end of coupling length L_1 , the tip widths on both sides are linearly increased to 450 nm, while the tip width in the center remains unchanged ($W_2 = 160$ nm), where the gap width is reduced to 80 nm between them. Secondly, the trident-shaped SWG is gradually turned into the taper SWG in order to further shrink the coupled mode size together with two matched silicon waveguides on both sides, where the coupling length along the x -direction is L_2 (part 2) and the tip width and gap width of the silicon waveguide are W_3 (W_4) and g_2 (g_3) at the left side (right side), respectively. The corresponding width of taper SWG structure is tapered from 1.22 μm to 0.45 μm . Thirdly, the SWG-wire tapered transition structures are employed to couple the optical mode from SWG waveguide to output silicon wire waveguide, and the bilateral matched strip waveguides are linearly tapered from W_4 to W_5 in a conversion length of L_3 (part 3), where the gap widths between bilateral strip waveguides and central SWG-wire tapered waveguide are kept the same ($g_3 = 150$ nm) along the x -direction. Note that, to enhance the mode conversion efficiency, a tapered silicon wire waveguide is used in the central part of the tapered SWG from left side of L_2 to right side of L_3 , corresponding to the waveguide width tapering from 160 nm to 450 nm. Therefore, the total conversion length is a sum of L_1 , L_2 , and L_3 . Through these three key steps, the input fiber mode (lensed fiber, MFD: 3.2 μm [15,26]) can be efficiently converted to on-chip silicon waveguide mode with a typical waveguide size of 220 nm \times 450 nm, which is a commonly used size for the on-chip single-mode silicon waveguide. In addition, the grating period and duty cycle of the employed SWG structure are set as $\Lambda = 300$ nm and $a/\Lambda = 50\%$, respectively, which could alleviate the fabrication requirements.

Based on the abovementioned device scheme, a three-dimensional finite-difference time-domain (3D-FDTD) method is employed to design and optimize the device parameters in detail [29,30]. Figure 2 illustrates the calculated light field evolution through the designed device. We can clearly find that the input fiber mode is indeed converted to the silicon waveguide mode in a total conversion length of 60 μm , and the area difference between input and output modes is quite large (over 100 times) from results of the electric field distributions shown in Figure 2a,c. Utilizing the proposed edge coupler, the input fiber mode size is gradually reduced as well as enhanced mode power density. By adding

two matched strip waveguides on both sides of the central SWG waveguide, the coupled mode could be well-confined in the taper SWG region and further converted to the silicon waveguide via SWG-wire tapered transition waveguide. Finally, we can obtain an efficiently fundamental TE₀ mode of the single-mode silicon waveguide, achieving fiber-to-chip coupling requirements. Within this process, the coupling loss is mainly from the interface between the optical fiber and proposed edge coupler. To reduce such loss, the mode field match should be designed as high as possible at the interface, which is determined by the mode overlap between optical fiber and coupler facet. The mode overlap (MO) is given by [27,28]

$$MO = \frac{|\int E_o E_c dA|^2}{\int |E_o|^2 dA \int |E_c|^2 dA}, \quad (1)$$

where E_o and E_c represent the electric field distributions of optical fiber mode and waveguide mode at the interface, and A is the 2D integral region, respectively. To achieve high coupling efficiency, the mode of the designed waveguide structure at the interface should overlap with the fiber mode to a great extent. After the mode field match, stable and low-loss light transmission and mode conversion should be required to obtain an efficient on-chip fiber-to-chip coupler. Therefore, we will perform detailed structure design and optimization to find the optimum device parameters in the following sections.

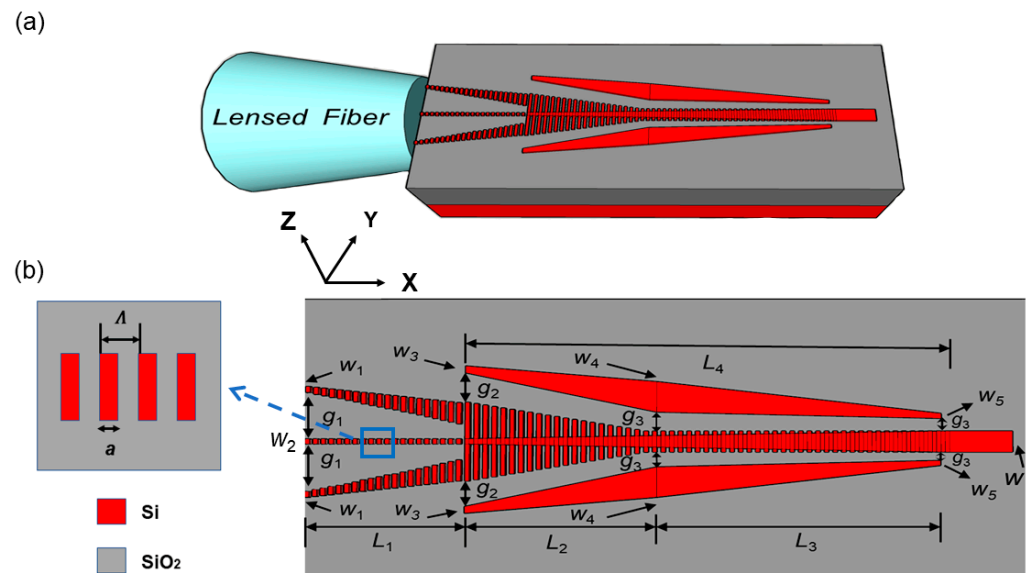


Figure 1. (a) Schematic layout of the proposed fiber-to-chip edge coupler assisted by SWG structure. The upper cladding of SiO₂ is not shown for clarity. (b) Top view of the proposed device and the conversion region is divided into three parts. The structural materials and parameters are also labeled.

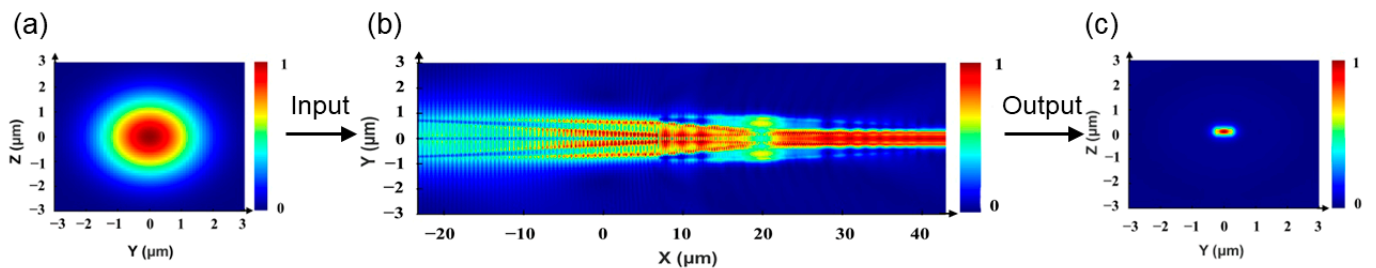


Figure 2. (a) Electric field distribution of the input fiber mode at $\lambda = 1550$ nm, Gaussian source. (b) Electric field evolution through the proposed fiber-to-chip edge coupler. (c) Electric field distribution of the output silicon waveguide mode at $\lambda = 1550$ nm.

3. Results

Before we conduct the structural parameter analyses, the device performance index should be determined first. For the fiber-to-chip edge coupler, loss is a key indicator which includes coupling loss and transmission loss [26–28]. Here, we employ IL coming from input fiber mode to output silicon waveguide mode to characterize the device performance. Figure 3 shows the obtained IL of the proposed edge coupler as functions of the tip widths (W_1 , W_3) at the left side of part 1 and part 2. It is noted that the tip width W_3 of the matched silicon strip waveguide has more influence on the device performance than the tip width W_1 of the trident-shaped SWG, where the optimum value of W_3 is 140 nm within the calculation range. Meanwhile, we can find that the tip width W_1 will almost not affect the device performance (IL) as its value is less than 180 nm, which corresponds to a high mode overlap between optical fiber mode and waveguide mode at the coupling interface. Furthermore, the corresponding electric field distributions can be observed in the insets of Figure 3. Therefore, by consideration of the obtained IL and fabrication linewidth requirement, we set W_1 as 120 nm in the following analyses.

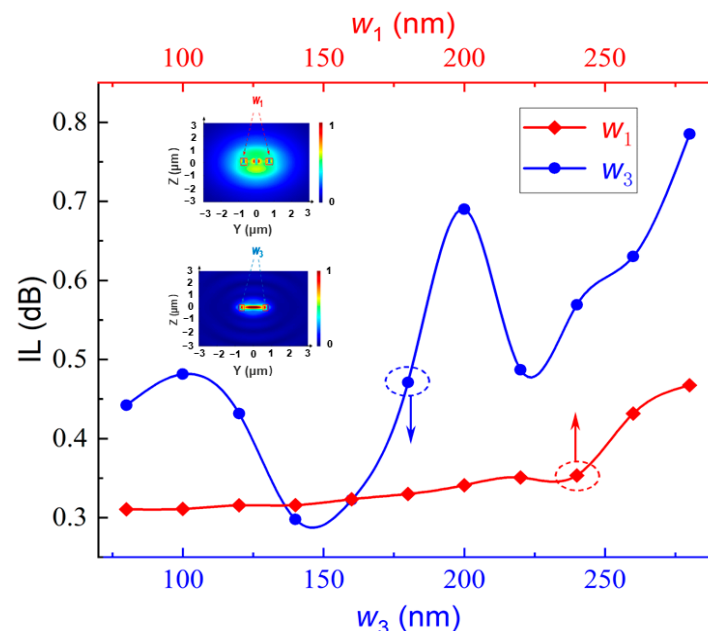


Figure 3. IL of the proposed edge coupler as functions of the tip widths (W_1 , W_3) at the left side of part 1 and part 2 in the device. Insets show the electric field distributions at cross-sections of the two waveguide tip positions.

Apart from tip widths of SWG and silicon waveguide, their gap widths (g_1 , g_2) are also closely related to the device performance. Figure 4 plots the gap widths (g_1 , g_2) variation affecting the IL, where g_1 and g_2 are the gap widths at the left side of part 1 and part 2, respectively. From Figure 4, we can observe that the obtained IL is gradually reducing as g_1 increases from 420 nm to 620 nm, and the IL tends to be stable when g_1 is larger than 550 nm, revealing a high mode overlap with input fiber mode achieved at this gap position. Here, we choose g_1 as 570 nm, which could be easily realized via using current fabrication facilities [28,31]. However, for g_2 , nearly opposite changing behavior can be found, that is, the large gap width will bring large on-chip coupling loss. To reduce IL, a small gap width of g_2 is recommended, and g_2 is set as 120 nm in the present device by consideration of the device fabrication. The corresponding device IL is about 0.3 dB at these chosen optimum positions. Moreover, the required conversion length of every part in the proposed edge coupler should be also determined, which is related to the total fiber-to-chip conversion length. Figure 5 shows the obtained IL dependent on the conversion lengths of part 1 (L_1) and part 2 + part 3 ($L_4 = L_2 + L_3$) in the proposed device. Here, we consider part 2 and

part 3 as a whole during calculation, and more detailed optimizations on their lengths are performed in Figure 6. From Figure 5, we can clearly find a low loss range for the conversion length L_1 , that is, from 18 μm to 30 μm with IL lower than 0.4 dB. Within such a range, the obtained lowest IL is only 0.23 dB at the conversion length $L_1 = 27 \mu\text{m}$, which is quite promising for the low-loss fiber-to-chip coupler. Meanwhile, IL reveals relatively low dependence on the conversion length L_4 and L_4 is a combination of L_2 and L_3 . As L_4 varies from 31.5 μm to 34 μm , the obtained IL is relatively stable and the lowest value is nearly 0.25 dB at the conversion length around $L_4 = 33 \mu\text{m}$. Therefore, the obtained ultralow-loss feature of the proposed edge coupler as well as quite short conversion length offers a good solution for the light coupling between optical fiber and on-chip silicon waveguide compared with previous reports [19–23,26–28].

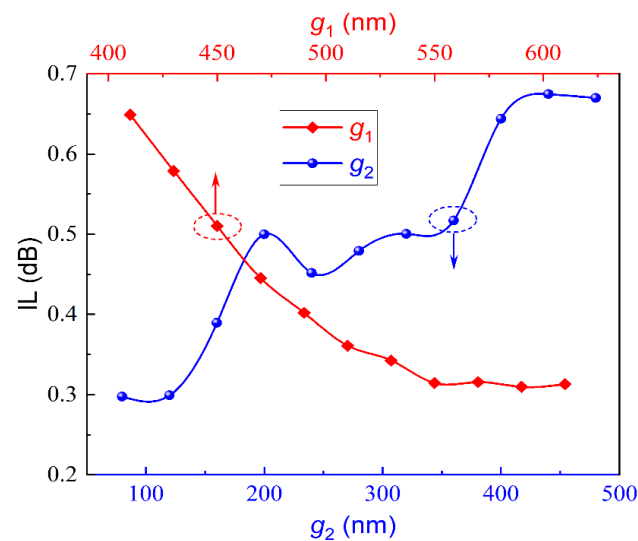


Figure 4. IL of the proposed edge coupler as functions of the gap widths (g_1 , g_2) at the left side of part 1 and part 2 in the device.

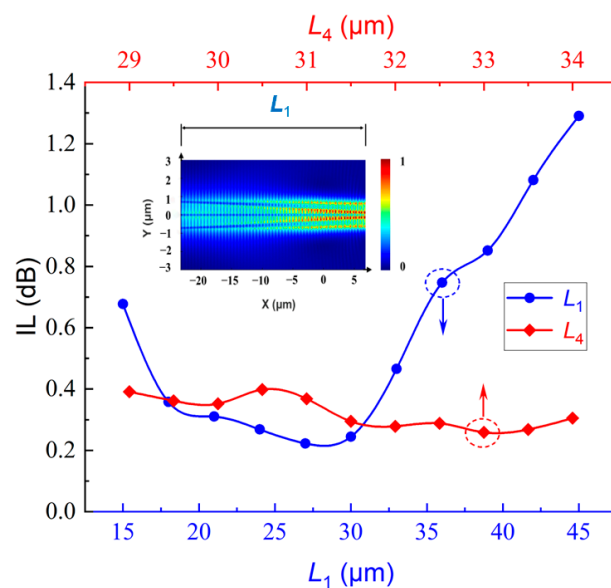


Figure 5. Calculated IL of the proposed device as functions of its conversion lengths L_1 and L_4 of part 1 and part 2 + part 3, respectively. Inset illustrates the electrical field evolution through part 1 in the proposed device.

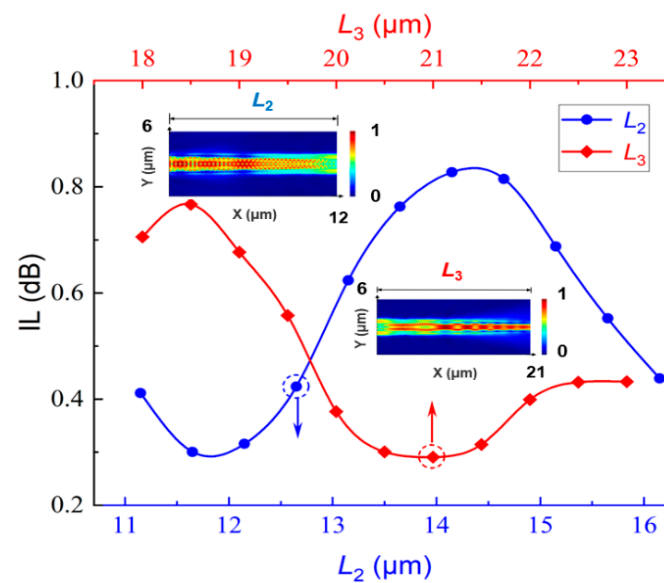


Figure 6. Calculated IL of the designed device as functions of its conversion lengths L_2 and L_3 of part 2 and part 3, respectively. Insets illustrate the electrical field evolutions through these two parts in the proposed device.

Figure 6 gives a more detailed analysis of device performance (IL) dependent on the conversion lengths L_2 and L_3 of part 2 and part 3 in the proposed device. From Figure 6, we can find obvious fluctuations within the calculation ranges and the ranges we chose can cover the lowest value of IL. To obtain such low IL, the optimum conversion lengths are located at $L_2 = 12 \mu\text{m}$ and $L_3 = 21 \mu\text{m}$, respectively. If these conversion lengths shift from their optimum values about $\pm 1 \mu\text{m}$, the obtained IL is still lower than 0.4 dB, revealing relatively large fabrication tolerance. Thus, the total conversion length of the silicon waveguide structure for the edge coupler is $L_1 + L_2 + L_3 = 60 \mu\text{m}$ in the length direction, which can efficiently guide the light mode from input optical fiber to the on-chip silicon waveguide, realizing the compact fiber-to-chip coupling. Moreover, the reflection loss of the proposed device is less than -28 dB , which is quite low for the on-chip devices. Table 1 lists the final determined structural parameters of the proposed fiber-to-chip edge coupler.

Table 1. Optimized structural parameters of the proposed fiber-to-chip edge coupler.

Parameters	W_1 (nm)	W_2 (nm)	W_3 (nm)	W_4 (nm)	W_5 (nm)	g_1 (nm)
Values	120	160	140	450	120	570
Parameters	g_2 (nm)	g_3 (nm)	L_1 (μm)	L_2 (μm)	L_3 (μm)	L_4 (μm)
Values	120	150	27	12	21	33

Based on the optimized structural parameters, we further study the wavelength spectrum of IL for the proposed device shown in Figure 7, where the material dispersions of silicon and silica are also considered [32]. Note that the device reveals better performance working at long wavelength than at the short wavelength within the calculation range from $1.48 \mu\text{m}$ to $1.9 \mu\text{m}$. When the working wavelength is less than $1.5 \mu\text{m}$, the device IL is quickly increased, even larger than 5 dB, which is very large for fiber-to-chip coupling loss. If we want to make IL less than 1.5 dB, the allowable working wavelength range can vary from 1510 nm to 1900 nm, corresponding to a bandwidth of 390 nm. If we further reduce the criterion of IL to 1 dB, the available working bandwidth can still reach 240 nm from 1520 nm to 1760 nm, which is superior to some previous reports [20,22,23,26–28]. Meanwhile, at the nominal wavelength of $1.55 \mu\text{m}$, IL is quite low, only 0.23 dB. Therefore, the proposed

device would be a good candidate to well support the low-loss and broadband operation of on-chip silicon devices.

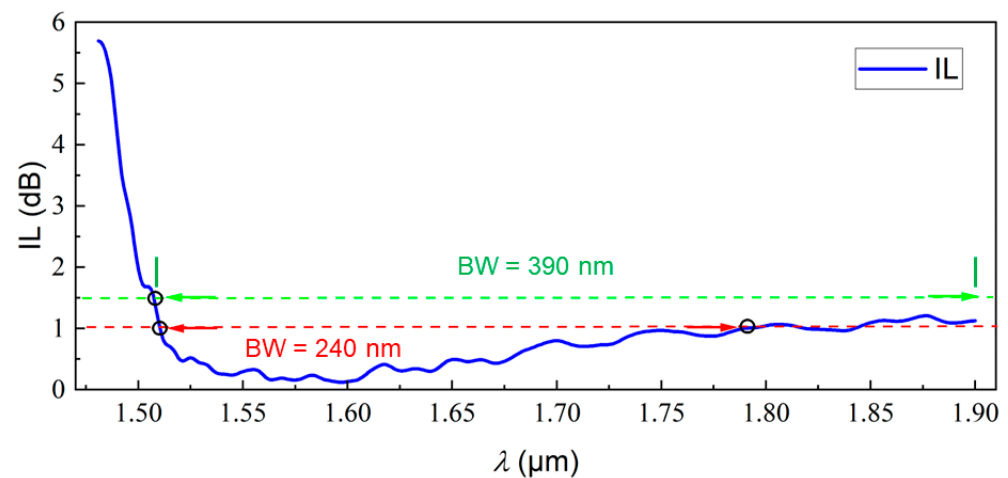


Figure 7. Wavelength spectrum of IL for the proposed edge coupler. The wavelength range changes from 1.48 μm to 1.9 μm and the available working bandwidths are also marked with $\text{IL} < 1.5$ dB and $\text{IL} < 1$ dB, respectively. BW: bandwidth.

To better reveal the function of the two matched strip waveguides on both sides of the central trident-shaped SWG structure, we have made a comparison, that is, the two matched strip waveguides are missing, and the electric field evolution can be found in Figure 8. From this figure, we can find that a slight diffraction effect can be observed at the end of part 2 and the obtained IL of such a device is 0.6 dB at the working wavelength of 1.55 μm . If we further add the designed two matched strip waveguides, such a diffraction effect can be removed as shown in Figure 2b, and the obtained IL is reduced to only 0.23 dB at the working wavelength of 1.55 μm . Therefore, the added two matched strip waveguides can help eliminate the light diffraction effect during the mode coupling process from optical fiber to silicon waveguide through the proposed device. In addition, we also analyze the light field distribution along the waveguide thickness direction for the proposed device, where the device structural parameters are listed in Table 1. Figure 9 plots the x–z view of the electric field evolution through the designed fiber-to-chip edge coupler, where the z-direction stands for the waveguide thickness direction and both the buried oxide layer and upper cladding are silicon dioxide. From Figure 9, we can see that the coupled light from optical fiber can be well-confined in the proposed edge coupler and no energy is leaked into the silicon substrate from our calculations.

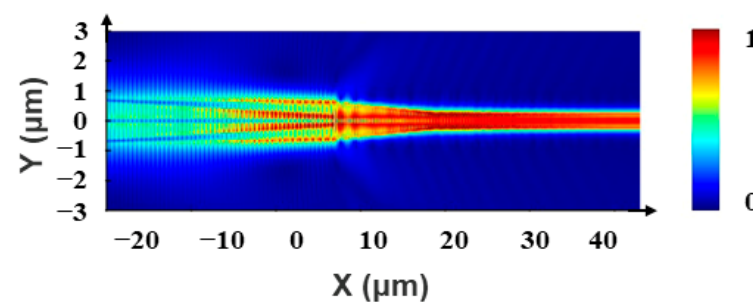


Figure 8. Electric field evolution through the proposed device when the two matched strip waveguides on both sides of the central trident-shaped SWG structure are missing. Working wavelength is $\lambda = 1550$ nm.

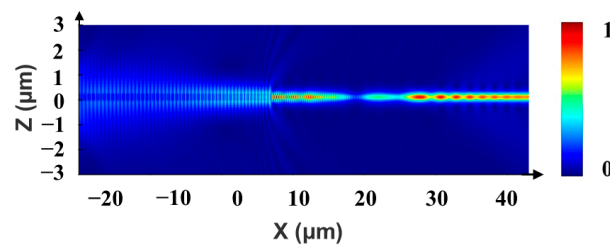


Figure 9. The x–z cross-section view of the electric field evolution through the proposed device. The buried oxide and upper cladding are silicon dioxide.

For the present device fabrication, only one-step E-beam lithography and a one-step etching process will be required since the whole device has a uniform etching depth (220 nm), which could be realized using current fabrication facilities [15,28,31]. Considering fabrication imperfections in practice, we consider the lateral offset between trident-shaped SWG and two matched strip waveguides, because these two sections are separated and their relative positions are more easily affected by fabrication errors. The optimum relative positions shown in Table 1 are derived through structural optimizations. We define Y as the lateral offset of two matched strip waveguides relative to the central trident-shaped SWG. $Y = 0$ stands for the optimum positions, $Y > 0$ stands for the two matched strip waveguides away from the central trident-shaped SWG, and $Y < 0$ stands for the two matched strip waveguides close to the central trident-shaped SWG, respectively, and the obtained results are shown in Figure 10. Note that the device performance reveals significant performance deterioration when the relative positions shift from their optimum positions, particularly for $Y > 0$. If $IL < 0.5$ dB should be kept, the lateral offset range can vary from -40 nm to 200 nm according to our calculation results, which would be very friendly to the device fabrication. In addition, we have also calculated the tolerance ranges of duty cycle, tip width, and gap width of the proposed fiber-to-chip edge coupler, which are shown in Figure 11. From this figure, we can find that the tip width of the proposed device has the smallest tolerance range compared with the duty cycle and gap width. If we set the same criterion of $IL < 0.5$ dB for them, the available tolerance ranges are from 0.483 to 0.540 , from -8 to 24 nm, and from -20 to 25 nm for the duty cycle, tip width shift, and gap width shift, respectively. Therefore, we should carefully control the tip width of the proposed device during the device fabrication process.

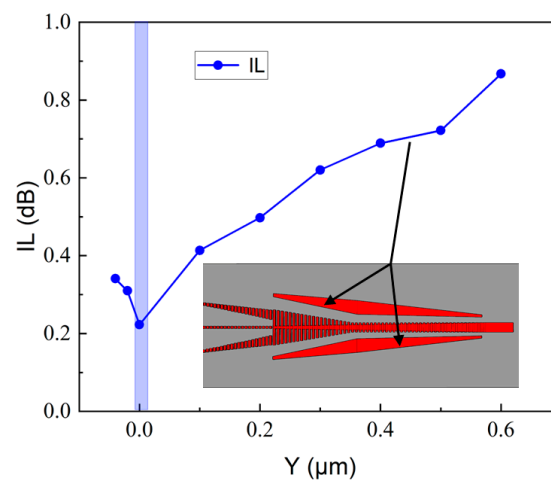


Figure 10. Fabrication tolerance analysis. The obtained IL dependent on the lateral offset of two matched strip waveguides relative to the central trident-shaped SWG. $Y > 0$ and $Y < 0$ stand for the two matched strip waveguides away from and close to the central trident-shaped SWG, respectively. Inset shows the device structure and vertical bold line indicates the optimum position without lateral offset ($Y = 0$).

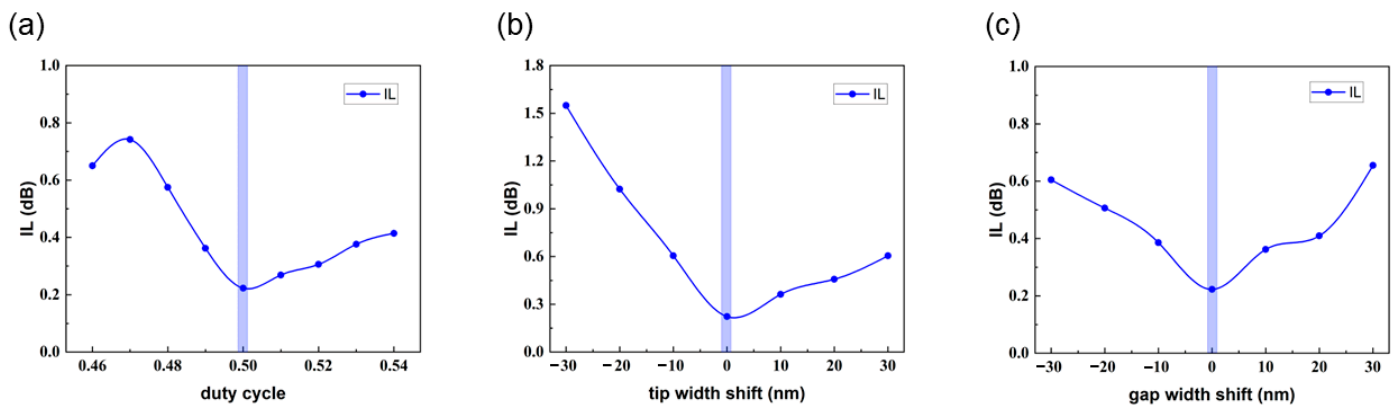


Figure 11. Fabrication tolerance analysis. IL dependent on the variations of (a) duty cycle, (b) tip width shift, and (c) gap width shift of the proposed fiber-to-chip edge coupler.

Finally, we make a comprehensive comparison between previously reported fiber-to-chip edge couplers and the proposed device from total length, IL, bandwidth, and fiber mode size, as listed in Table 2. It is indicated that the working bandwidth and IL of our proposed edge coupler are obviously better than some reported devices. Meanwhile, the total conversion length of 60 μm is also comparable to some reports and only single-step lithography and etching process will be required. With these features, we hope the proposed edge coupler could boost the development of broadband and low-loss fiber-to-chip coupler and further drive PICs towards broadband work and applications.

Table 2. Device Comparisons between Typical Fiber-to-Chip Edge Couplers.

Device Structure	Length (μm)	IL (dB)	Bandwidth (nm)	Fiber MFD (μm)
Single-layer taper [19]	40	6	-	5 [E]
Double-layer taper [20]	>300	0.25/0.51 *	60 (IL < 0.7 dB)	4.1 [E]
Triple-layer and multi-stage taper [21]	895	0.44	-	8.2 [S]
Triple-layer wide ridge taper [22]	300	0.35	95 (IL < 1 dB)	6.5 [E]
Suspended inverse taper [23]	-	1.3	>100 (IL < 1.8 dB)	Cleaved SMF [E]
Fork-shaped SWG coupler [26]	75	1 dB	>100 (IL~1 dB)	3.2 [S]
SWG-assisted inverse taper [27]	45	2.5	150 (IL < 2.5 dB)	3 [S]
Metamaterial-based SWG coupler [28]	90	2.22/2.53 *	120 (IL < 3 dB)	10 [E]
This work	60	0.23	240 (IL < 1 dB)	3.2 [S]

*: 0.25/0.51 and 2.22/2.53 stand for ILs of TE/TM modes, respectively. E: experiment results, S: simulation results; SMF: single-mode fiber. “-”: not mentioned.

4. Conclusions

In summary, by utilizing SWG-assisted structure, we have proposed and analyzed a silicon-based fiber-to-chip edge coupler where the conversion region consist of a trident-shaped SWG in the center and two matched strip waveguides on both sides along the length direction. To enhance the device performance, we have divided the structure into three parts. The first part is employed to efficiently couple the input fiber mode through mode matching design. The second part is used to make the coupled mode convert to the SWG waveguide mode gradually. The third part is intended to convert the SWG waveguide mode to the silicon waveguide mode. From results, the required total conversion length is only 60 μm for the fiber-to-chip coupling, and the accumulated IL is as low as 0.23 dB at the wavelength of 1550 nm. Moreover, the working bandwidth can be extended to 240 nm (390 nm) by keeping IL lower than 1 dB (1.5 dB), which is larger than some previous reports. Therefore, the present device would be a good candidate for the fiber-to-chip coupler with requirements of broadband, low loss, and compact size.

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References

1. Siew, S.Y.; Li, B.; Gao, F.; Zheng, H.Y.; Zhang, W.; Guo, P.; Xie, S.W.; Song, A.; Dong, B.; Luo, L.W.; et al. Review of silicon photonics technology and platform development. *J. Lightwave Technol.* **2021**, *39*, 4374–4389. [\[CrossRef\]](#)
2. Rickman, A. The commercialization of silicon photonics. *Nat. Photonics* **2014**, *8*, 579–582. [\[CrossRef\]](#)
3. Thomson, D.; Zilkie, A.; Bowers, J.E.; Komljenovic, T.; Reed, G.T.; Vivien, L.; Marris-Morini, D.; Cassan, E.; Viro, L.; Fedeli, J.M.; et al. Roadmap on silicon photonics. *J. Opt.* **2016**, *18*, 073003. [\[CrossRef\]](#)
4. Rahim, A.; Spuesens, T.; Baets, R.; Bogaerts, W. Open-access silicon photonics: Current status and emerging initiatives. *Proc. IEEE* **2018**, *106*, 2313–2330. [\[CrossRef\]](#)
5. Margalit, N.; Xiang, C.; Bowers, S.M.; Bjorlin, A.; Blum, R.; Bowers, J.E. Perspective on the future of silicon photonics and electronics. *Appl. Phys. Lett.* **2021**, *118*, 220501. [\[CrossRef\]](#)
6. Yang, H.; Kuan, Y.; Xiang, T.; Zhu, Y.; Cai, X.; Liu, L. Broadband polarization-insensitive optical switch on silicon-on-insulator platform. *Opt. Express* **2018**, *26*, 14340–14345. [\[CrossRef\]](#)
7. Falconi, F.; Melo, S.; Scotti, F.; Malik, M.N.; Scaffardi, M.; Porzi, C.; Ansalone, L.; Ghelfi, P.; Bogoni, A. A combined radar & lidar system based on integrated photonics in silicon-on-insulator. *J. Lightwave Technol.* **2021**, *39*, 17–23. [\[CrossRef\]](#)
8. Pinguet, T.; Denton, S.; Gloeckner, S.; Mack, M.; Masini, G.; Mekis, A.; Pang, S.; Peterson, M.; Sahni, S.; Dobbelaere, P.D. High-volume manufacturing platform for silicon photonics. *Proc. IEEE* **2018**, *106*, 2281–2290. [\[CrossRef\]](#)
9. Witzens, J. High-speed silicon photonics modulators. *Proc. IEEE* **2018**, *106*, 2158–2182. [\[CrossRef\]](#)
10. Marchetti, R.; Lacava, C.; Carroll, L.; Gradkowski, K.; Minzioni, P. Coupling strategies for silicon photonics integrated chips. *Photonics Res.* **2019**, *7*, 201–239. [\[CrossRef\]](#)
11. Son, G.; Han, S.; Park, J.; Kwon, K.; Yu, K. High-efficiency broadband light coupling between optical fibers and photonic integrated circuits. *Nanophotonics* **2018**, *7*, 1845–1864. [\[CrossRef\]](#)
12. Wang, X.; Yu, H.; Huang, Q.; Zhang, Z.; Zhou, Z.; Fu, Z.; Xia, P.; Wang, Y.; Jiang, X.; Yang, J. Polarization-independent fiber-chip grating couplers optimized by the adaptive genetic algorithm. *Opt. Lett.* **2021**, *46*, 314–317. [\[CrossRef\]](#) [\[PubMed\]](#)
13. Cheng, L.; Mao, S.; Li, Z.; Han, Y.; Fu, H.Y. Grating couplers on silicon photonics: Design principles, emerging trends and practical issues. *Macromachines* **2020**, *11*, 666. [\[CrossRef\]](#) [\[PubMed\]](#)
14. Su, L.; Trivedi, R.; Sapra, N.V.; Piggott, A.Y.; Vercruyse, D.; Vučković, J. Fully-automated optimization of grating couplers. *Opt. Express* **2018**, *26*, 4023–4034. [\[CrossRef\]](#) [\[PubMed\]](#)
15. Mu, X.; Wu, S.; Cheng, L.; Fu, H.Y. Edge couplers in silicon photonics integrated circuits: A review. *Appl. Sci.* **2020**, *10*, 1538. [\[CrossRef\]](#)
16. Liu, W.; Zhang, J.; Liu, L.; Dai, D.; Shi, Y. High efficiency silicon edge coupler based on uniform arrayed waveguides with un-patterned cladding. *IEEE Photonics Technol. Lett.* **2020**, *32*, 1077–1080. [\[CrossRef\]](#)
17. Zhang, Z.; Shan, X.; Huang, B.; Zhang, Z.; Cheng, C.; Bai, B.; Gao, T.; Xu, X.; Zhang, L.; Chen, H. Efficiency enhanced grating coupler for perfectly vertical fiber-to-chip coupling. *Materials* **2020**, *13*, 2681. [\[CrossRef\]](#)
18. Larrea, R.; Gutierrez, A.M.; Griol, A.; Brimont, A.; Sanchis, P. Fiber-to-chip spot-size converter for coupling to silicon waveguides in the O-band. *IEEE Photonics Technol. Lett.* **2019**, *31*, 31–34. [\[CrossRef\]](#)
19. Almeida, V.R.; Panepucci, R.R.; Lipson, M. Nanotaper for compact mode conversion. *Opt. Lett.* **2003**, *28*, 1302–1304. [\[CrossRef\]](#)
20. Maegami, Y.; Okano, M.; Cong, G.; Suzuki, K.; Ohno, M.; Narushima, T.; Yokoyama, N.; Seki, M.; Ohtsuka, M.; Namiki, S.; et al. Simple and fully CMOS-compatible low-loss fiber coupling structure for a silicon photonics platform. *Opt. Lett.* **2020**, *45*, 2095–2098. [\[CrossRef\]](#)
21. Sun, S.; Chen, Y.; Sun, Y.; Liu, F.; Cao, L. Novel low-loss fiber-chip edge coupler for coupling standard single mode fibers to silicon photonic wire waveguides. *Photonics* **2021**, *8*, 79. [\[CrossRef\]](#)

22. Wang, X.; Quan, X.; Liu, M.; Cheng, X. Silicon-nitride-assisted edge coupler interfacing with high numerical aperture fiber. *IEEE Photonics Technol. Lett.* **2019**, *31*, 349–351. [[CrossRef](#)]
23. Jia, L.; Li, C.; Liow, T.-Y.; Lo, G.-Q. Efficient suspended coupler with loss less than -1.4 dB between Si-photonic waveguide and cleaved single mode fiber. *J. Lightwave Technol.* **2018**, *36*, 239–244. [[CrossRef](#)]
24. Halir, R.; Ortega-Monux, A.; Benedikovic, D.; Mashanovich, G.Z.; Wanguemert-Perez, J.G.; Schmid, J.H.; Molina-Fernandez, I.; Cheben, P. Subwavelength-grating metamaterial structures for silicon photonic devices. *Proc. IEEE* **2018**, *106*, 2144–2157. [[CrossRef](#)]
25. Li, C.; Zhang, M.; Xu, H.; Tan, Y.; Shi, Y.; Dai, D. Subwavelength silicon photonics for on-chip mode-manipulation. *PhotonIX* **2021**, *2*, 11. [[CrossRef](#)]
26. Mu, X.; Chen, Z.M.; Cheng, L.R.; Wu, S.L.; Pepe, A.; Tu, X.; Fu, H.Y. Effects of fabrication deviations and fiber misalignments on a fork-shape edge coupler based on subwavelength gratings. *Opt. Commun.* **2021**, *482*, 126562. [[CrossRef](#)]
27. Sun, Y.; Li, T.; Zhou, P.; Zou, Y. Subwavelength-structured high-efficiency nanophotonic coupler for air top-cladded silicon waveguide. *IEEE Photonics J.* **2021**, *13*, 6600705. [[CrossRef](#)]
28. He, A.; Guo, X.; Wang, T.; Su, Y. Ultracompact fiber-to-chip metamaterial edge coupler. *ACS Photonics* **2021**, *8*, 3226–3233. [[CrossRef](#)]
29. Sullivan, D.M. *Electromagnetic Simulation Using the FDTD Method*; IEEE Press: Piscataway Township, NJ, USA, 2000.
30. Lumerical FDTD Solutions. Available online: <https://www.lumerical.com/products/fdtd/> (accessed on 12 April 2022).
31. Giewont, K.; Nummy, K.; Anderson, F.A.; Ayala, J.; Barwicz, T.; Bian, Y.; Dezfulian, K.K.; Gill, D.M.; Houghton, T.; Hu, S.; et al. 300-mm monolithic silicon photonics foundry technology. *IEEE J. Sel. Top. Quantum Electron.* **2019**, *25*, 8200611. [[CrossRef](#)]
32. Palik, E.D. *Handbook of Optical Constants of Solids*; American Academic Press: Salt Lake City, UT, USA, 1998.