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Microstrip Array Ring FETs with 2D p-Ga_2O_3 Channels Grown by MOCVD

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Abstract: Gallium oxide (Ga_2O_3) thin films of various thicknesses were grown on sapphire (0001) substrates by metal organic chemical vapor deposition (MOCVD) using trimethylgallium (TMGa), high purity deionized water, and silane (SiH_4) as gallium, oxygen, and silicon precursors, respectively. N_2 was used as carrier gas. Hall measurements revealed that films grown with a lower VI/III ratio had a dominant p-type conduction with room temperature mobilities up to 7 cm^2/Vs and carrier concentrations up to ~10^{20} cm^{-3} for thinner layers. High resolution transmission electron microscopy suggested that the layers were mainly κ phase. Microstrip field-effect transistors (FETs) were fabricated using 2D p-type Ga_2O_3:Si, channels. They achieved a maximum drain current of 2.19 mA and an on/off ratio as high as ~10^8. A phenomenological model for the p-type conduction was also presented. As the first demonstration of a p-type Ga_2O_3, this work represents a significant advance which is state of the art, which would allow the fabrication of p-n junction based devices which could be smaller/thinner and bring both cost (more devices/wafer and less growth time) and operating speed (due to miniaturization) advantages. Moreover, the first scaling down to 2D device channels opens the prospect of faster devices and improved heat evacuation.

Keywords: MOCVD; p-type; Ga_2O_3; thin films

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1. Introduction

Recently, gallium oxide (Ga_2O_3) with an ultra-wide bandgap (UWBG) of ~4.9 eV has emerged as a next generation semiconductor material for high power electronic devices. This is in great part due to its high breakdown electric field (~8 MV/cm), which largely surpasses that of competing materials systems such as SiC or GaN. Furthermore, the emergence of n-type doping capacity and single crystal Ga_2O_3 substrates has allowed the development of various unipolar electronic devices including metal oxide semiconductor field effect transistors (MOSFETs), Schottky diodes, and metal semiconductor field effect transistors (MESFET), which have been demonstrated based on high quality homo-epitaxial growth [1–3]. The vast majority of this work has focused on homoepitaxial growth of monoclinic β-Ga_2O_3, which is the most stable of five common polytypes α-, β-, γ-, ε-,

and κ). A major drawback of β-Ga_2O_3 until recently, however, has been lack of a method to obtain p-type conduction; this is a key limitation for its adoption in a whole range of semiconductor device applications. Moreover, the relatively low thermal conductivity of Ga_2O_3 and the problem of Ga_2O_3 substrate cost being two orders of magnitude higher than sapphire are both currently hindering the fuller development of Ga_2O_3-based powered electronics. In previous studies, we showed that κ-Ga_2O_3 (an orthorhombic polymorph which is normally considered to be transient) could be stabilized in heteroepitaxial growth on sapphire (0001) substrates by MOCVD [4–12]. In this work, we found that high levels of shallow acceptor p-type conduction could be achieved in such layers using silicon impurity doping under Ga rich growth conditions. We then processed 2D layers of such p-type Ga_2O_3:Si into microstrip array ring FETs using conventional photolithography. The operational characteristics of the FETs proved to be consistent with p-type conduction. This is the first demonstration of both shallow acceptors doping of Ga_2O_3 and a p-type Ga_2O_3 channel FET. A phenomenological model that is coherent with a p-type channel is also presented.

2. Materials and Methods

A commercial MOCVD reactor (AIXTRON 200/4 RF) was used to grow Ga_2O_3 on sapphire (0001) substrates at growth temperatures ranging from 730 °C to 1000 °C. Trimethylgallium (TMGa), high purity deionized water and SiH_4 were adopted as the Ga, O and Si precursors, respectively. N_2 was used as the carrier gas. The total pressure was 50 mbar. The VI/III ratio was either 100 (Ga-rich) or 150 (O-rich). The SiH4 flow rate was fixed at 15 sccm [4–12].

3. Results

XRD analysis was performed (Figure 1) to analyze the phases of the grown ~150 nm thick Ga_2O_3:Si with different VI/III ratio 100 and 150. The XRD results showed three peaks for each Ga_2O_3:Si layer. The three peaks that were observed were similar to the results of the β-Ga_2O_3 substrate (Figure 1). However, the TEM analysis in Figure 1d showed the result of κ-phase with the space group of $Pna2_1$ [4,5,10]. This metastable and transient κ-Ga_2O_3 was also identified by Playford et al. [13]. The κ-phase Ga_2O_3:Si was grown in the (002) direction and the six rotated domains were observed in the ~150 nm thick Ga_2O_3:Si.

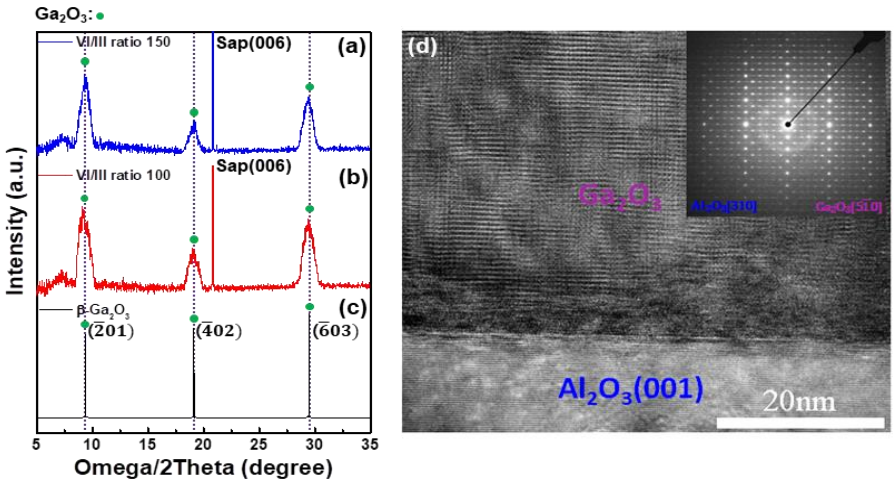
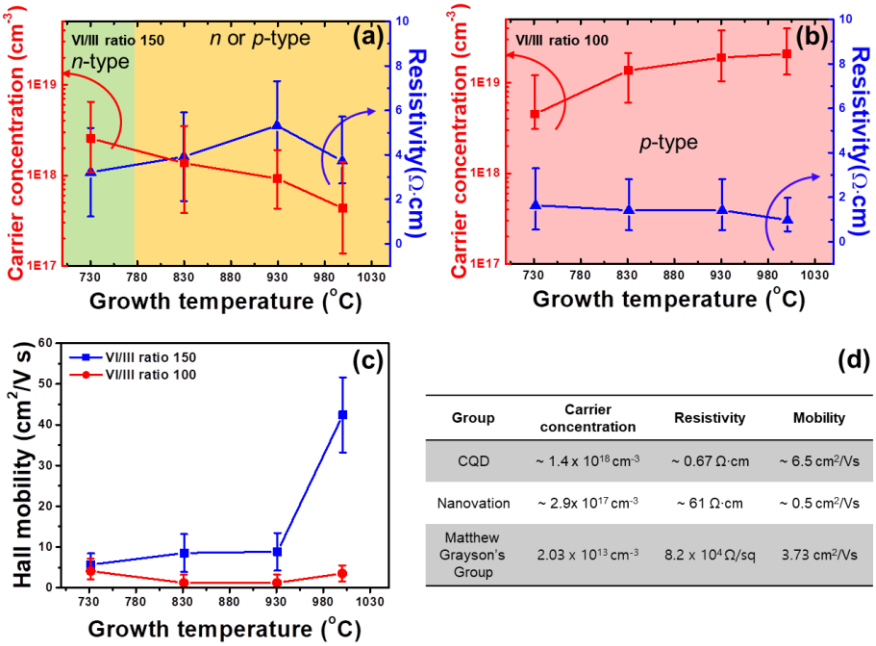


Figure 1. XRD omega/2theta scan of ~150 nm thick Ga_2O_3:Si with VI/III ratio (**a**) 150 and (**b**) 100; (**c**) XRD omega/2theta scan of β-Ga_2O_3 (TAMURA Corp); (**d**) TEM image of typical morphology of the ~150 nm thick Ga_2O_3:Si on sapphire, and an inset of the SAED patterns that were obtained along the (510) zone axis at the Ga_2O_3/Al_2O_3 interface. Ga_2O_3:Si with the space group $Pna2_1$ is identified.

Electrical properties were measured using Van der Pauw Hall measurements. Ohmic contacts were obtained using a Ga/In eutectic. Figure 2a,b show the results as a function of growth temperature for both VI/III ratios. At a VI/III ratio of 150, Ga_2O_3:Si that was grown at 730 °C shows n-type characteristics and the carrier concentration is ~2.6 × 10^{18} cm^{-3}. The average resistivity is measured as ~4.3 Ω·cm. As the growth temperature was increased from 730 °C to 1000 °C, the carrier concentration decreased linearly to ~4.4 × 10^{17} cm^{-3}. Such a tendency is reminiscent of the amphoteric doping of GaAs with Si [14,15]. In the case of GaAs, p-type Si doping behavior was obtained for a relatively low V/III ratio and growth temperature [16–18]. Assuming that the Si dopant acts as a shallow acceptor by substituting on the O-site of the Ga_2O_3, the VI/III ratio of 100 growth condition could be expected to a generate higher density of oxygen vacancies (V_O) by virtue of the Ga-rich nature of the growth which lets the Si substitute more readily at the O-sites. This assumption is coherent with Figure 2c which shows the Hall mobility of the Ga_2O_3:Si as a function of growth temperature for VI/III ratios of 150 and 100. For a VI/III ratio of 150, an n-type mobility near 50 cm^2/Vs was observed for a growth temperature of 1000 °C. For a VI/III ratio of 100, a p-type mobility of ~3.3 cm^2/Vs was observed. This demonstrates Si being an amphoteric dopant in κ-Ga_2O_3. Si impurity doping is generally incorporated to substitute for Ga where it acts as a shallow donor to create heavily doped n-type Ga_2O_3. But as the density of V_O increases under Ga-rich growth conditions, the above results suggest that Si can act as a shallow acceptor by substituting on the O-sites in κ-Ga_2O_3, and thus promote a transformation to predominantly p-type conduction. These p-type results were confirmed via theoretical and experimental measurements by multiple groups [19–21].



Group	Carrier concentration	Resistivity	Mobility
CQD	~ 1.4 x 10^{18} cm^{-3}	~ 0.67 Ω·cm	~ 6.5 cm^2/Vs
Nanovation	~ 2.9x 10^{17} cm^{-3}	~ 61 Ω·cm	~ 0.5 cm^2/Vs
Matthew Grayson's Group	2.03 x 10^{13} cm^{-3}	8.2 x 10^4 Ω/sq	3.73 cm^2/Vs

Figure 2. (**a**) Carrier concentration and resistivity of Ga_2O_3:Si on sapphire (0001) as a function of growth temperature at VI/III ratio 150; (**b**) carrier concentration and resistivity of Ga_2O_3:Si on sapphire (0001) as a function of growth temperature at VI/III ratio 100; (**c**) Hall mobility of Ga_2O_3:Si on sapphire (0001) as a function of growth temperature at VI/III ratio 100 and 150; (**d**) Table of ~150 nm thick hall measurement data measured in different groups.

Ring type FETs were fabricated and evaluated for the characteristics of the FET device of ~150 nm thick p-type Ga_2O_3:Si with VI/III ratio of 100. Figure 3 shows the I-V curves; it was observed that the drain current decreased with increasing gate voltage. However, it was not possible to achieve pinch-off due to the gate electrode burning at gate voltages higher than 50 V. To avoid this issue, the channel thickness was reduced to ~1.2

nm and the ring pattern FETs were patterned with microstrips. Ga_2O_3:Si channel layers were grown at 1000 °C with a VI/III ratio of 100. The channel thickness was estimated to be ~1.2 ± 0.5 nm based on the interferometric growth rate calibration and AFM step-edge profilometry. Hall measurements confirmed the p-type nature of the layers with a resistivity of ~0.007 Ω·cm, a carrier concentration of ~1.7 × 10^{20} cm^{-3}, and a mobility of ~5.7 cm^2/Vs.

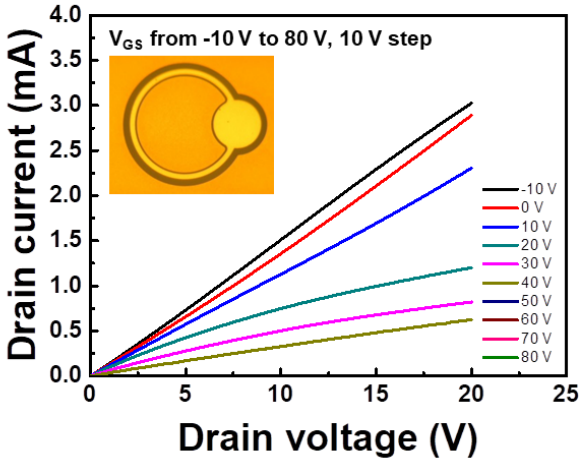


Figure 3. I-V curves of ~150 nm thick p-type Ga_2O_3:Si on sapphire (0001) from V_{GS} = −10 V to 80 V and inset is an optical microscope image of the fabricated device.

Standard photolithography and lift-off were employed to deposit source and drain metal contacts. Before their deposition, 3 μm × 3 μm microstrip patterns were formed by electron cyclotron resonance-reactive ion etching (ECR-RIE) with CF_4 for 5 min. The metal contacts were Ti (20 nm)/Au (150 nm) deposited by e-beam evaporation. SiO_2 of 100 nm thick gate dielectric material was formed by plasma-enhanced chemical vapor deposition (PECVD). After dielectric and passivation film deposition, the gate metal contact was formed with Pt (20 nm)/Ti (20 nm)/Au (150 nm) on the SiO_2 film. The gate length, and the spacing between the source/drain and the inside source circular pad were 15, 20, and 100 μm, respectively. Figure 4a shows schematic illustrations of the device with top- and cross-sectional views illustrating the device scale. Figure 4b shows an optical microscope image of the fabricated devices.

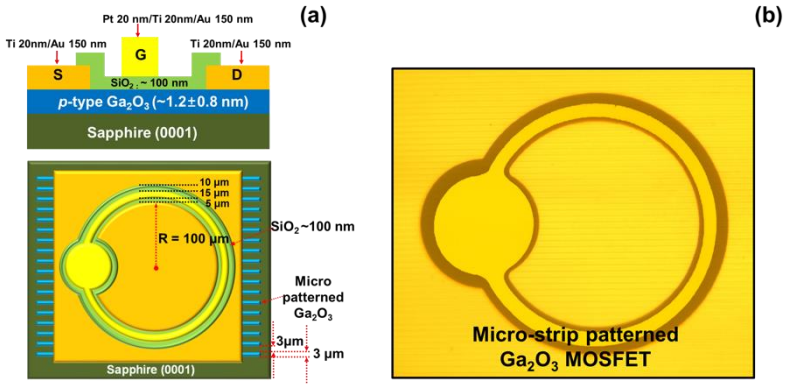


Figure 4. (**a**) Cross view and top view schematic illustration of 2D Ga_2O_3:Si channel microstrip array FETs with details of device scale; (**b**) Optical microscope image of the fabricated device.

The FETs were then fabricated and tested using a semiconductor parameter analyzer and probe station. Figure 5a shows the DC source-drain current versus source-drain voltage (I_{DS}–V_{DS}) output characteristics for the depletion-mode FETs that were measured by increasing the gate-source voltage (V_{GS}) stepwise from −50 to 100 V. The maximum I_{DS} was 2.19 mA and it was effectively modulated by V_{GS} from −50 to 100 V, which is coherent with a p-type channel. Because of the heavy p-doping, the 2D microstrip channel is normally-on, and the channel off-state was observed for a gate bias of 50 V (I_{DS} = 0.1 pA at V_{DS} of 40 V). In addition, because of the high sheet resistance, even with a drain voltage as high as 40 V, the voltage drop in the FET channel was still lower than $|V_G\text{-}V_T|$, which was the condition for current saturation in long channel FETs. As such, the I_{DS}-V_{DS} characteristics remained linear. Figure 5b displays a similar set of curves that were obtained from the simulation. It can be seen that the theoretical model is consistent with the experimental data in showing an output resistance increase with positive gate voltage and I_{DS} bunching with little variation of the output resistance for $V_{GS} < 0$. This is also consistent with a p-type channel. Figure 5c shows the transfer characteristics at V_{DS} of 10 to 40 V in a logarithmic scale. The device achieved an on/off ratio of ~10^8 by minimizing the thickness and width of the channel. Figure 5d shows that IG increases above a V_{GS} of 50 V because of a gate leakage current. It is expected that the on/off ratio can be further improved through the optimization of the dielectric layer.

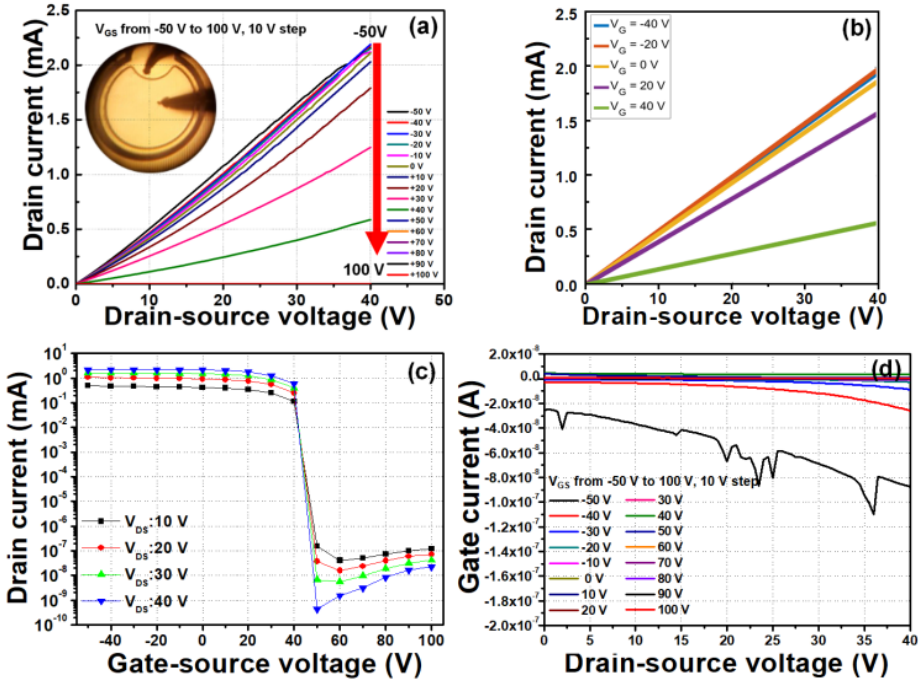


Figure 5. (**a**) I-V curves from V_{GS} = −50 V to 100 V and the inset is an optical microscope image of the device during measurement using a probe station; (**b**) Simulation data of I-V curves from V_{GS} = −40 V to 40 V; (**c**) transfer characteristics at V_{DS} = 10 V to 40 V; (**d**) Gate current-drain source voltage characteristics with V_{GS} increased stepwise from −50 V to 100 V.

A phenomenological model was developed that was based on the device configuration that is displayed in Figure 4. Figure 6 shows the schematic of the model device that consists of a linear array of δ = 3 μm wide micro-strips that were separated from each other by δ = 3 μm. They are covered by a disk-shaped source contact of 200 μm in diameter and separated from a square shaped drain by a 30 μm wide circular channel. As such, in each quadrant, the channel length, Li, varies between a minimum value when it is perpendicular to the disk and a maximum value when it is tangential to the disk. The position of the ith microstrip is identified by its distance, di, from the center of the source disk.

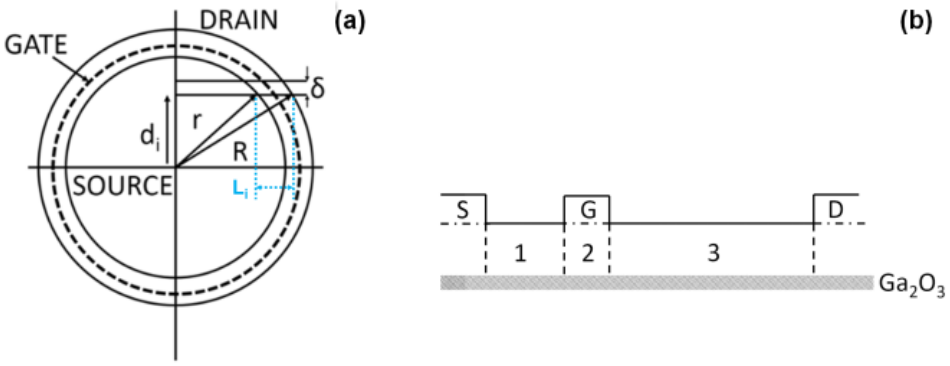


Figure 6. (**a**) Schematic illustration of the 2D Ga_2O_3:Si channel microstrip array FETs. (**b**) Schematic illustration of three portions of the Ga_2O_3 channel.

At $V_G = 0$ V, the channel is uniform and the current between source and drain in the i^{th} micro-strip channel is given by

$$I_i = ep_s\delta v_i \tag{1}$$

where e is the electron charge (C), p_s is the 2D hole concentration (carriers/cm^2), δ the wire width (cm), and v_i is the hole velocity in the ith channel (cm/s). In the absence of saturation velocity (long channel-low mobility),

$$v_i = \frac{\mu V_{DS}}{L_i} \tag{2}$$

where μ is the hole mobility (cm^2/Vs) and L_i is the channel length (cm).

If $d_i = 2i\delta \; with \; 0 \le i \le N$, Equation (1) becomes for top and bottom right quadrants

$$I_{right} = 2\sum_{i=0}^{N} I_i = ep_S\mu V_{DS}\sum_{i=0}^{N} 1/\left[\sqrt{(N+5)^2 - i^2} - \sqrt{N^2 - i^2}\right] = 2.84ep_S\mu V_{DS} \tag{3}$$

Due to the relatively big gate pad on the left side of the source, the channel lengths are longer for a sizeable portion of the FIN-microstrips, so we estimate the total current should be multiplied by a factor η ~ 1.8–1.9 < 2. Finally,

$$I = I_{Right} + I_{Left} = \eta I_{Right} \tag{4}$$

At $V_G \neq 0$, the channel is made of three portions with different conductances (Figure 6b). By neglecting the contact resistance, we get for each channel,

$$I_i(V_G) = \frac{V_{DS}}{\frac{1}{G_1^i} + \frac{1}{G_2^i} + \frac{1}{G_3^i}} \; with \; G_{1,3}^i = \frac{ep_s(V_G = 0)\delta\mu}{L_{1,3}^i} \;\; G_2^i = \frac{ep_s(V_G \neq 0)\delta\mu}{L_2^i} \tag{5}$$

If $P_s(V_G \neq 0) = P_s(V_G = 0)exp(-\frac{eV_C}{KT})$, where $V_c(V_G)$ s the channel potential that is induced by the gate bias, the expression for the current reads

$$I_i(V_G) = ep_s(V_G = 0)\delta\mu V_{DS}/(L_1^i + L_2^i exp(eV_C/kT) + L_3^i) \tag{6}$$

or after summation over all channels,

$$(V_G) = \frac{2I(V_G = 0)}{1 + exp(\frac{eV_C}{kT})} \tag{7}$$

This equation shows that for $V_C < 0$ ($V_G < 0$) the drain current decreases, whereas for $V_C > 0$ ($V_G > 0$) the drain current increases in agreement with the experimental data. This is coherent with the channel being a p-type. In quantitative terms, it shows that current de-

creases by several orders of magnitude under a positive V_G compared to a limiting increase by a factor 2 under a negative V_G. This asymmetry in the variation of the I-V characteristics for $V_G < 0$ and $V_G > 0$ is also consistent with the experimental data.

From the Poisson equation, one can derive an expression of V_C for intermediate gate bias:

$$V_C(y) = \frac{V_G \lambda_D exp(-\frac{y-D}{\lambda_D})}{D + \lambda_D} \quad (8)$$

where D is the thickness of the SiO_2 barrier, y is the vertical coordinate inside the Ga_2O_3 layer, and λ_D is the Debye length in the Ga_2O_3 layer that is fitted to reproduce the experimental I-V characteristics. Figure 5b displays the simulation data of I-V curves from V_{GS} = −40 to 40 V, for which we used a channel mobility μ = 23 cm^2/Vs and hole concentration $p_s = 2.35 \times 10^{12}/cm^2$.

4. Conclusions

In conclusion, κ-Ga_2O_3:Si layers that were grown on sapphire (0001) substrates by MOCVD showed consistent p-type Hall signal for layers that were grown with lower III/VI ratios during growth. The room temperature mobilities were up to 7 cm^2/Vs, resistivities were as low as 0.007 Ω.cm, and the carrier concentrations were up to ~10^{20} cm^{-3} for thinner layers. The ring mesa FETs were fabricated based on ~1.2 nm thick p-Ga_2O_3:Si channels that were formed into a number of 3 μm wide microstrips. The devices achieved a maximum drain current density of 2.19 mA and an on/off ratio of ~10^8 and showed characteristics that were consistent with a p-type conduction in the channel. The p-type Ga_2O_3 that was demonstrated in this work represents a significant advance and is state of the art, which may herald the fabrication of a range of p-n junction-based devices. These could be smaller/thinner and bring both cost (more devices/wafer and less growth time) and operating speed (due to miniaturization) advantages than current isotype FETs. Moreover, the demonstration of the first functioning devices based on scaling down to 2D device channels in Ga_2O_3 based FETs opens the prospect of faster devices and improved heat evacuation.

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