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High-Speed Waveguide InP/InGaAs UTC-PDs for over 200 Gb/s/λ Optical Transmission

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Abstract

Scaling of artificial intelligence data centers is pushing the aggregate speed of photonic transceivers over 1.6 Tb/s and even 3.2 Tb/s, which in the multi-channel configuration accounts for a 200 Gb/s data transmission speed for each wavelength. Uni-traveling carrier photodetectors have proved high bandwidth performance utilizing ultra-fast carrier transit and ultra-small junction capacitance, while few reports discuss the effect of the coplanar lines on bandwidth. In this work, the parasitic effect of coplanar lines is studied, and a modified structure is designed for an InP-based waveguide uni-traveling carrier photodetector. Simulation results reveal a promotion rather than deterioration effect in PD frequency response from the coplanar lines after optimization, and the circuit analysis predicts a parasitic capacitance decrease over 40 fF, which is larger than the 23 fF junction capacitance itself. The fabricated photodetector verifies a 69% increase in bandwidth up to 120 GHz for the same active area at an external responsivity of 0.476 A/W. The eye-diagrams of 100 GBd and 140 GBd under PAM4 format also indicate huge potential for over 200 Gb/s/λ photodetection.

Keywords: waveguide photodetector; uni-traveling carrier; coplanar lines; indium-phosphide; optical transceiver; parasitic

1. Introduction

Driven by the urgent need for massive data transmission from artificial intelligence (AI) and cloud computing applications, the speed of optical transceivers in optical networks is upgrading rapidly through the mainstream 800 Gb/s to potential 1.6 Tb/s and even predictably 3.2 Tb/s in the near future, accelerating the transformation of conventional data centers (DCs) to AIDCs [1–3]. Under such circumstances, the scale-up and scale-out of data centers requires fast response from transceivers and an aggregate data rate over 200 Gb/s per lane or wavelength. The establishment of Ethernet standards concerning 200 Gb/s to 1.6 Tb/s operation (IEEE P802.3dj) and 200 Gb/s per wavelength operation in multimode fibers (IEEE P802.3ds) is already ongoing, and they are expected to be released within this year [4]. For photoreceivers, high-bandwidth photodetectors (PDs) over 67 GHz are fundamental to support such high rate with the assistance of at least 4-level Pulse Amplitude Modulation (PAM4). Waveguide PDs based on Ge/Si materials are welcome for data centers and have achieved high bandwidth to 80 GHz recently [5,6], whereas high cost and delicate sub-micro fabrication techniques are necessary for ultra-high

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bandwidth beyond 100 GHz using lateral junction PD structures [7,8]. The high overall expectation of both ultra-high speed and high responsivity at low dark current demands extremely advantageous material properties, device design and fabrication methods. Uni-traveling carrier photodetectors (UTC PDs) in III-V materials, with inherent high absorption coefficient, large bandgap range, and distinct carrier mobility, could be a competitive candidate for such high-speed scenarios.

The UTC structure utilizes deviated transportation paths for carriers, where electrons travel through the longer junction area (or collector) to ensure small junction capacitance and holes crowd to the P-contact layer by relaxation immediately after generation in the P-doped absorption layer (or absorber) [9]. Enabled by the higher mobility and velocity, the transit time of electrons could balance well with that of the holes, amounting to a reduced total transit time. Multiple bandgap and doping designs are also beneficial for shortening this transit time, such as the modified absorber, graded-doping absorber, pre-doped collector, double cliff-layer collector, and near-ballistic collector structures [10–14]. To date, there have been many reports on improving UTC-PD performance such as ultra-high bandwidth over 200 GHz [15,16], high power handling over −2.4 dBm@165 GHz [14], and bias-insensitive working [17,18]. Despite the highlighted device performance, few reports concern the coplanar lines (CPLs) of the PDs which could also play an important role in high-frequency photodetection and radio-frequency (RF) power transmission. As part of the PD chip, coplanar lines are used to collect photocurrent from the junction, and also act as an electrical network in parallel with the junction, hence determining the total impedance seen by the readout circuit or testing probes.

In our previous work [19], we integrated a multimode waveguide and an impedance line to a uni-traveling carrier mesa to achieve a bandwidth of 140 GHz, but at the cost of a high RF loss (over 6 dB) and a low responsivity, which always holds true to any PDs with matching resistors. In this work, we choose to optimize the coplanar line size to reduce the induced parasitic capacitances and inductances, and the deduced lumped circuit parameters are analyzed to explain the effect on frequency response. RF transmission simulations indicate an opposite trend in the frequency response evolution of the CPL itself, where the optimized CPL enables an uplift in S_{21} curve even with a reduced inductance. The suppressed parasitic effect results in an elevated bandwidth up to 120 GHz for the same PD size. Section 2 will introduce the PD structure with the design details of the CPLs. Section 3 will exhibit the fabrication process and the measurement results of the fabricated device, and the bandwidth improvement will be explained and discussed in Section 4. Finally, Section 5 will conclude the work.

2. Device Design

The UTC photodetector is integrated on a 3.85 μm thick coupling waveguide through a single epitaxy growth consisting of a stack of InP/InGaAsP(Q1.06) layer pairs (diluted waveguide) and two planar waveguide layers on top. Each InP layer has a constant thickness of 80 nm, whereas the thickness of InGaAsP(Q1.06) layers increases from 100 nm to 300 nm from bottom to top. The planar waveguide layers are N-doped for N contact and electron collection. Consecutively on the coupling waveguide is a 160 nm collector lightly doped to 1×10^{16} cm^{-3}, a 20 nm cliff layer moderately doped to 1×10^{17} cm^{-3}, a 110 nm absorber of three graded P-doped InGaAs layers, a 310 nm InGaAsP(Q1.1) electron barrier layer, and a P contact InGaAs layer. Two extra InGaAsP bandgap-grading layers of 20 nm and 30 nm are also inserted on the top and bottom of the absorber, respectively. Details of the epi-layers are summarized in Figure 1 below.

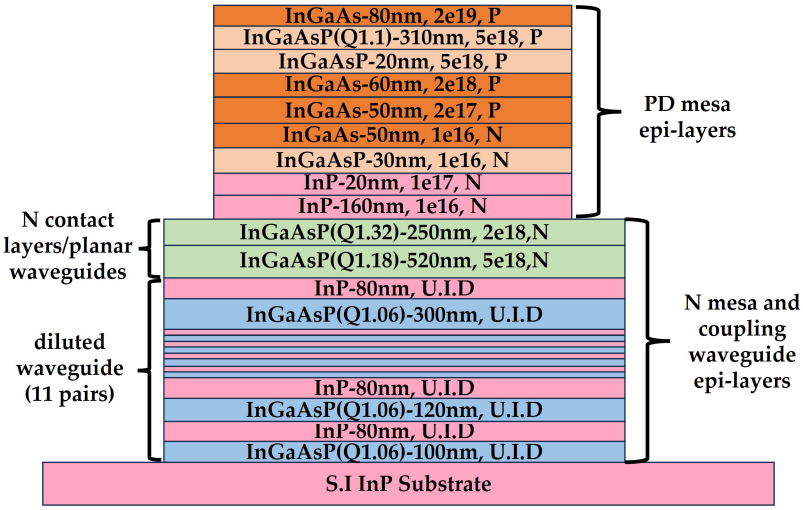


Figure 1. Epi-layer structure of the uni-traveling carrier photodetector.

Ground–signal–ground (GSG) on-chip coplanar lines are used to collect photocurrent from the junction, and the parasitic capacitance and inductance of the CPLs will also add to the total impedance seen by the probes or readout circuits. Depicted in Figure 2 are two GSG designs from our previous work and this work. For the signal lines, only a rectangle-shape line with a length of L_s and a width of W_s was used for both signal transmission and pad contact previously. In this work, the signal line is optimized to a transmission region with a length of L_s' and a width of W_s', and a region pad of 40 μm × 40 μm, both connected by a width grading region 10 μm long. Another width grading region is designed for signal feed from Port 1 to the signal line, which is 3.5 μm long in this work but 70.5 μm in the previous structure. Ground lines are also narrowed from 98 μm to 60 μm and aligned to the signal line at Port 2. The center-to-center distance of the ground–signal (GS) lines is also reduced to 100 μm from 150 μm to mitigate the RF wave transmission loss and device–probe coupling loss. The dielectric substrate under the gold GSG lines consists of a 3 μm polyimide layer, a 120 μm InP substrate layer, and a 1 μm indium layer on a 1.5 mm AlN_x substrate as is the case in reality after chip fabrication.

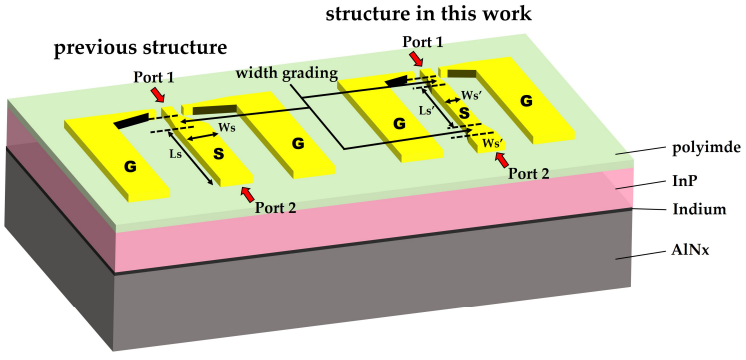


Figure 2. Schematic of GSG CPLs.

Both GSG CPL structures were simulated for transmission up to 300 GHz by the Finite Element Method, with the maximum mesh size of 1 μm and at least 10 mesh grids at the narrowest line for the highest frequency. Both ports were terminated with 50 Ω impedances. The S21 results are shown in Figure 3. Starting from the CPL size in the previous design as pointed out in Figure 3a, L_s was the first parameter to be swept and simulated. With the reduction in L_s, the normalized S21 curve lifts gradually at high frequency beyond 50 GHz, with a −3 dB bandwidth rising from 150 GHz to 200 GHz. Then, an extreme narrow-down

of W_S = 5 μm was introduced for three short L_S situations in Figure 3a, and an uplift in response between 50 GHz and 150 GHz could be achieved in Figure 3b, which is attributed to the inductance of the signal line. With W_S′ also fixed to 5 μm, L_S′ was swept for the new CPL design in Figure 3c. For L_S′ not exceeding 120 μm, the normalized S21 varies little during the whole band, but decreases fast for longer L_S′. This may indicate that the CPL capacitance has overruled the inductance, for the response curves no longer show any uplifts. Also confirmed in Figure 3d is the inductance reliance on the signal width, where only small W_S′ values lead to the uplift of response curves, and nearly no uplift is observed for W_S′ = 20 μm. In comparison, the optimized GSG pattern enables a −3 dB decline at a very high frequency of 280 GHz, whereas the previous GSG introduced loss over 3 dB beyond just 150 GHz. The response enhancement between 50 GHz and 150 GHz will surely help to improve the total PD bandwidth when taking the PD junction into consideration.

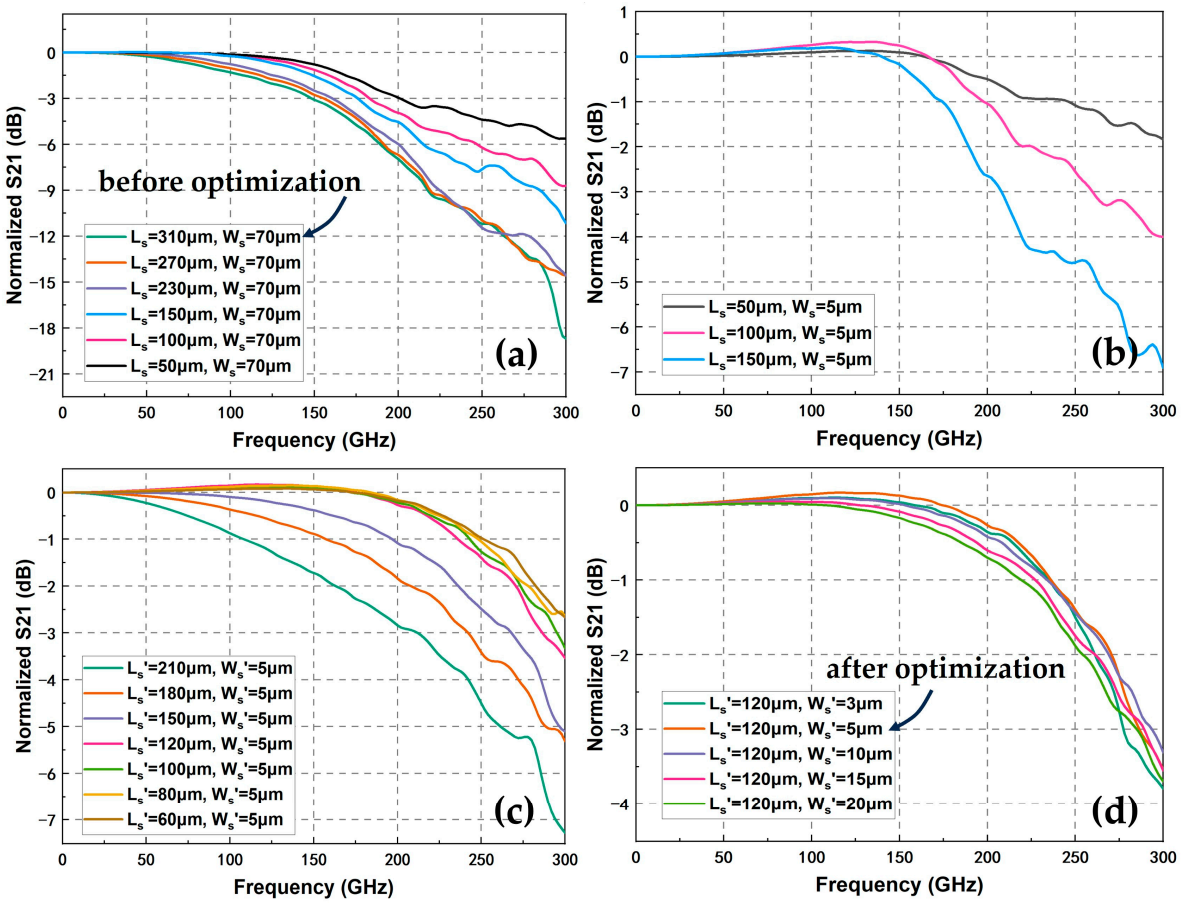


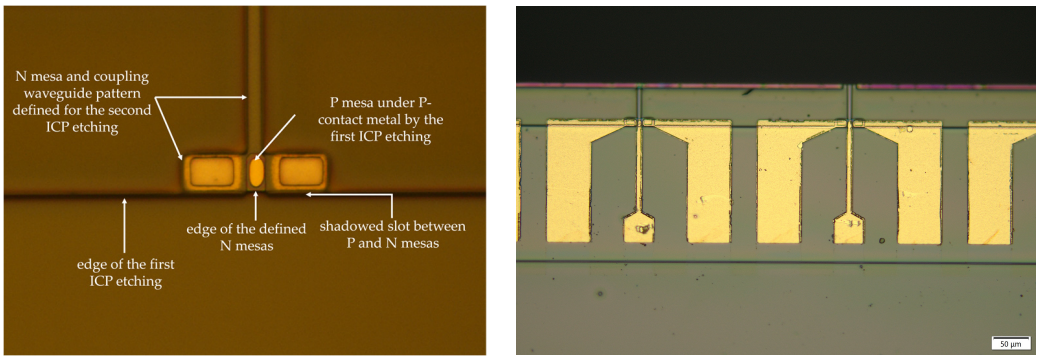
Figure 3. S21 simulation results for both GSG CPLs: (**a**) previous design with different L_S values, (**b**) previous design with narrowed signal line and different L_S values, (**c**) new design with different L_S′ values, and (**d**) new design with reduced signal line length and different W_S′.

3. Device Fabrication and Measurement

Device fabrication started with the deposition of Pt-Ti-Pt-Au P-contact metal by e-beam evaporation, which was followed by inductively coupled plasma (ICP) etching to define the P mesa position. In this work, we adopted a two-step etching process to form the rectangle P mesa, N mesa, and the coupling waveguide simultaneously, instead of three individual etchings for each region in our previous work. In the first step, only three sidewalls of the P mesa were etched down to the N-contact layer surface, leaving the remaining sidewall intact—otherwise a down-step to the N mesa would have been formed beneath the passivation layer. In the second step, both the N mesa and the coupling

waveguide were deeply etched to the substrate, during which the last sidewall of the P mesa was also etched. Consequently, on the side of the P mesa where the signal line transitions from the P mesa top down to the substrate, both the P and N mesas share a common sidewall, thereby avoiding the step that would otherwise be introduced by the overlaying N mesa.

The N-contact metal was sputtered and lifted off between the two etching steps, and a photolithographic polyimide layer was spun and solidified after the deep etching for passivation, leaving P and N contact windows open for CPL deposition. The CPLs were electroplated to 1.8 μm on a 300 nm Ti-Au seed layer by sputtering and lift-off too. The substrate was chemically thinned to 120 μm by hydrochloric acid and phosphoric acid solutions for convenient cleaving. Deep trenches perpendicular to coupling waveguides were formed during deep etching to help locate the cleaving point. After cleaving, the bar chips were deposited with SiO_2-Ta_2O_5 anti-reflection films on the input facets. Pictures of devices in and after fabrication are provided in Figure 4. The actual coupling waveguide length after cleaving is measured to be 43.8 μm.



(**a**) (**b**)

Figure 4. Microscope photographs of the fabrication process: (**a**) after the photolithography of the second ICP etching pattern, and (**b**) device bar ready for measurement.

The cleaved bars are mounted on Al_3N_4 heat sink substrates by fused indium, with the device input facets slightly protruding at substrate edges for the convenience of fiber coupling. Photo currents and dark currents were collected using on-chip probes, and the fiber-to-device-facet alignment was ensured by monitoring photocurrents during precise fiber position adjustment.

Dark current and photocurrent were measured using a parameter analyzer, where an optical illumination power of 4.33 mW at 1550 nm was measured for the coupling tapered fiber, and the I–V curves are plotted in Figure 5. The dark current remains low under 8.0 nA till −3.0 V, and reads 3.84 nA at −1.5 V where the photodetector was further measured for bandwidth and eye-diagrams. A photocurrent of 2.06 mA was observed at −1.5 V and 2.09 mA at −3.0 V, which amounts to a photoresponsivity of at least 0.476 A/W.

The bandwidth of the photodetectors was measured by the combination of a vector network analyzer (VNA) setup and a heterodyne setup where two lasers with identical polarizations were interfered for a high-speed magnitude-modulated optical source. Below 40 GHz, the VNA setup was used with a coaxial GSG probe for photocurrent collection. For frequency over 40 GHz, the RF power meters were used to measure PD output power as the frequency difference between the two lasers swept from 40 GHz to 170 GHz. Three GGB waveguide probes were used to cover the entire bands of 40~50 GHz, 75~110 GHz, and 110~170 GHz, whose insertion losses were carefully assessed from data sheets and de-embedded. All coaxial and waveguide probes feature the same 100 μm GSG pitch.

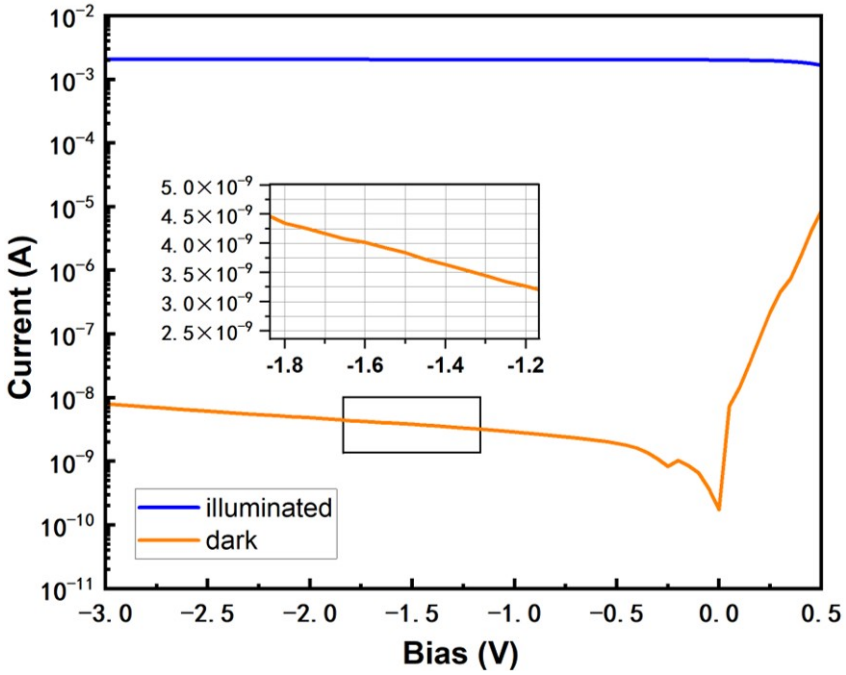


Figure 5. Dark current and photocurrent measurement results.

Figure 6 exhibits the measured and fitted results of PD bandwidth for both CPL designs with and without (w/o) optimization (opt.) After CPL optimization, the device achieves a bandwidth of 120 GHz. Under the same active area of 50μm^2, this value represents a 69% improvement compared with our previous one that only reaches 71 GHz. For the optimized CPL, the scattered data denoted by red circles manifest some irregular fluctuation beyond 40 GHz, which is also observed in the whole band of scattered data for CPL without optimization denoted by the blue diamonds. The reason should originate from the unstable composite wave magnitude coming from two individual lasers, for the data below 40 GHz of the PD without CPL optimization was also acquired from the heterodyne setup, instead of the VNA setup.

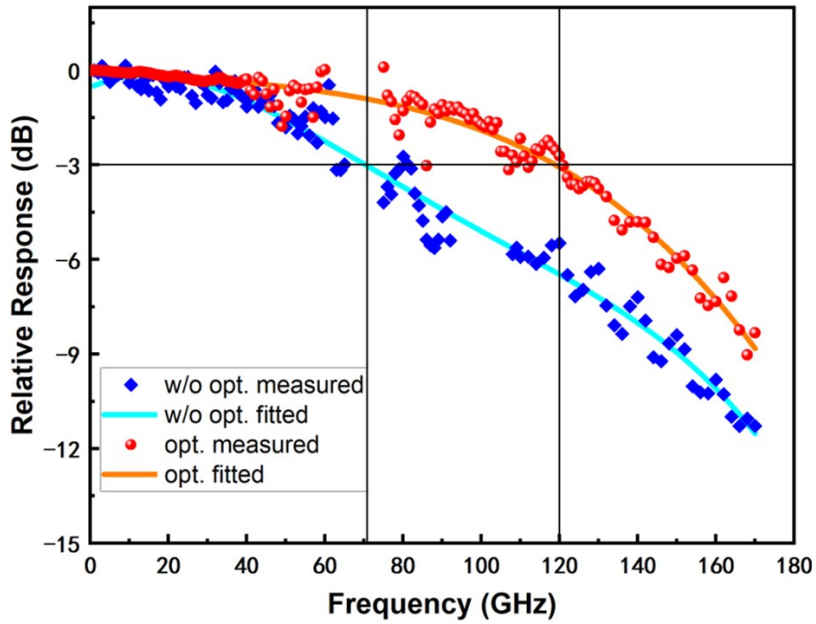
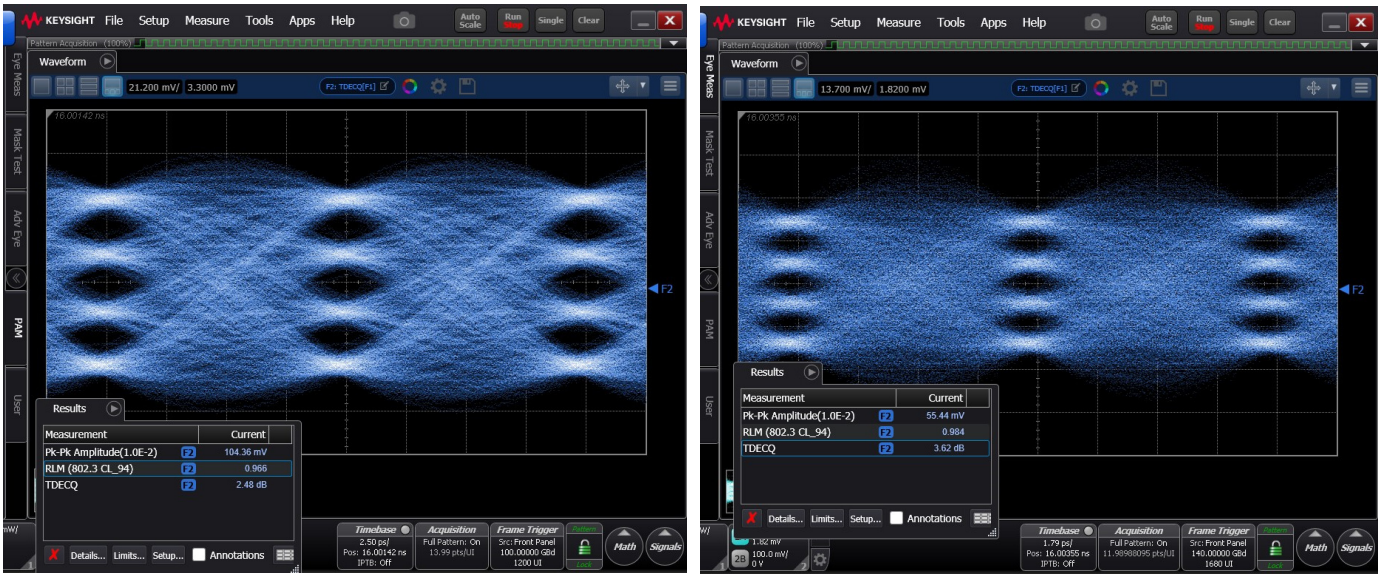


Figure 6. Bandwidth results at −1.5 V bias centered at 1550 nm and 5.0 mA average photocurrent.

Eye-diagrams were also measured to examine systematic transmission under PAM4 format. Both 100 Gbaud and 140 Gbaud rates were examined with on-chip probes, and the results are shown in Figure 7. The four energy levels are distinct with clear open eye patterns. Though the bit-error-rate (BER) is higher than standards during measurement, the high RMS Level Mismatch (RLM) over 0.96 and low Transmitter and Dispersion Eye Closure Quaternary (TDECQ) less than 3.62 dB still reflect a competitive performance for over 280 Gb/s for PAM4 signals. We believe that the performance could still remain excellent for better BER if higher photocurrents are biased. It should be noted that the frequency response of the 145 GHz bandwidth modulator was also included in the measurement results, and measurement beyond 140 Gbaud was therefore limited and unavailable due to higher response loss.



(**a**) (**b**)

Figure 7. PAM4 eye-diagram measurement results: (**a**) at 100 Gbaud and 4 mA average photocurrent; (**b**) at 140 Gbaud and 3 mA average photocurrent.

4. Discussion

The measurement results demonstrate an obvious improvement in both photoresponsivity and bandwidth performance. On one hand, the coupling waveguide length adopted in this design is longer, avoiding the situation in our previous work where the minimum optical power was evanescently coupled to the PD absorber due to the varied optical field distribution within the multimode waveguide. On the other hand, the additional anti-reflection film on the end facet also contributes to a reduced coupling loss.

As for the bandwidth improvement, we further conducted circuit simulations to clarify the influence of different CPL designs. The equivalent circuit is shown in Figure 8a to emulate the PD junction (red dashed line region) in series with the CPLs (green dashed line region) seen from the calibrated 50 Ω probe. Parameters were fitted to the measured S_{22} data in Figure 8b.

The deduced circuit parameters could be used to estimate the PD characteristics. Limited by the VNA capability, only parameters at the relatively low frequency band were fitted out. At high frequencies, the parallel junction resistances R_{j1} and R_{j2} should gradually increase and be reckoned as an open circuit; therefore, the whole junction capacitance is approximated as:

$$C_j \approx (1/C_{j1} + 1/C_{j2})^{-1}. \quad (1)$$

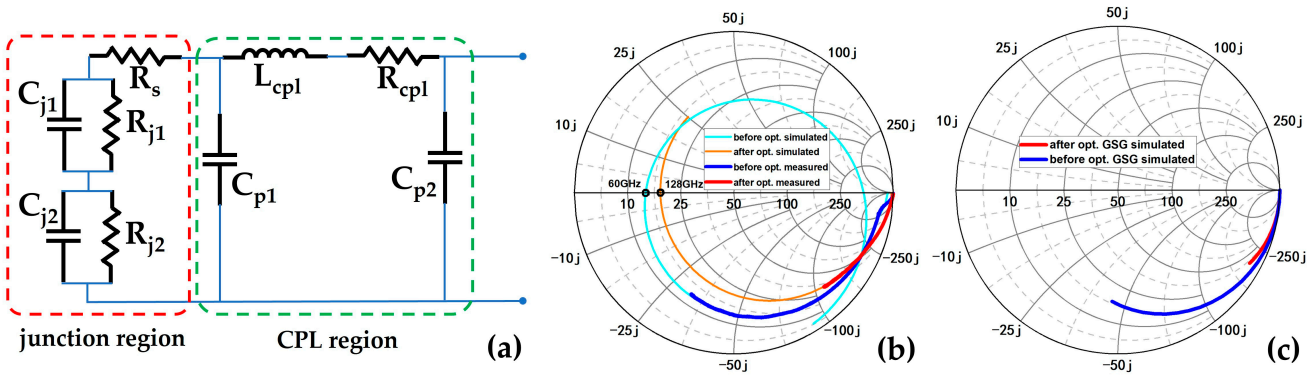


Figure 8. S_{22} parameter analysis results: (**a**) the equivalent circuit model; (**b**) measured (from 1 MHz to 40 GHz) and simulated (from 1 GHz to 170 GHz) S_{22} results of the PD; (**c**) simulated S_{22} results of the CPLs (from 1 MHz to 40 GHz).

In addition, the whole parallel capacitance of the CPLs could be estimated by the sum of C_{p1} and C_{p2} at high frequency as will be denoted by C_p. Key parameters are summarized in Table 1 below.

Table 1. Fitting results for the PD.

Fitted Circuit	C_{j1} [fF]	C_{j2} [fF]	C_j [fF]	C_{p1} [fF]	C_{p2} [fF]	C_p [fF]	L_{cpl} [pH]	R_{cpl} [Ω]
Before Optimization (bo)	32.97	129.51	26.28	34.90	18.29	53.19	130.94	2.93
After Optimization (ao)	35.92	63.91	23.00	6.20	1.09	7.29	53.09	14.84

The equivalent junction capacitances (C_j) deviate less due to the same PD mesa designs for both trials. The smaller value can be attributed to the reduced actual mesa size resulting from the overlaid photolithography and two ICP etchings mentioned in Section 2. The capacitance (C_p), inductance (L_{cpl}) and resistance (R_{cpl}) of the CPLs differ remarkably, which reflects the effect of the optimized size. The narrower signal line and the two-step etching process have decreased the capacitances simultaneously as the deduced C_p comprises 34.90 fF for C_{p1} and 18.29 fF for C_{p2} before optimization and 6.20 fF for C_{p1} and 1.09 fF for C_{p2} after optimization. For R_{cpl}, the signal line size variation dominates the resistance change, as calculated by:

$$R = \rho L / A, \tag{2}$$

where ρ, L, and A represent the resistivity, length and cross-section area of the transmission line respectively. Taking the rectangular portions in both CPLs for a rough estimation where the signal line is in series with two parallel ground lines, the ratios of the total L_{ao}/A_{ao} and L_{bo}/A_{bo} amount to 14.46 μm^{-1} and 3.21 μm^{-1}, respectively. This implies a resistance at least 4.5 times higher after optimization, in general agreement with the fitting result.

The inductance is complex considering both self- and mutual parts for CPLs, with the theoretical equations as follows [20]:

$$\begin{cases} L = \dfrac{\mu_0}{2\pi} l \left[\ln, \left(\dfrac{2l}{W+H} \right), +, 0.2235, \left(\dfrac{W+H}{l} \right), +, 0.5 \right] \\ M = \dfrac{\mu_0}{2\pi} \left[l \cdot arsinh\left(\dfrac{l}{D} \right) - \sqrt{l^2 + D^2} + D \right] \end{cases}, \tag{3}$$

where L is the self-inductance of a transmission line with a rectangle cross-section, M is the mutual inductance of two lines with the same length l. W and H are the width and

thickness of the line, and D is the distance between the two lines. Intuitively as in our work, line length l is bigger than the sum of W and H, and therefore L should increase with l monotonally. Similarly, M follows the same trend as L for l is over 1.5 times higher than D, and the inverse hyperbolic sine item also takes dominance. In total, the inductance is still higher for the CPLs before optimization.

For comparison, the S_{22} simulation results of the CPLs are also plotted in Figure 8c by the FEM described in Section 2. Both curves evolve in similar tendency as in Figure 8b and show less capacitive reactance meanwhile due to the absence of the PD junctions. The fitted circuit parameters for the simulated CPLs alone were also deduced by the "CPL region" circuit in Figure 8a, and the results are shown in Table 2. All capacitances and inductances achieve the same level as Table 1 presents, especially for results before optimization. This could also justify the reduced capacitance and inductance of the optimized CPL structure.

Table 2. Fitting results for the CPLs alone.

Fitted Circuit	C_{p1} [fF]	C_{p2} [fF]	C_p [fF]	L_{cpl} [pH]	R_{cpl} [Ω]
Before Optimization	45.98	12.95	58.93	121.19	23.22
After Optimization	16.98	1.02	18.00	60.00	29.65

The effect of the reduced CPL capacitance and inductance on frequency response tendency is also reflected in the Smith chart, for a faster conversion from capacitive to inductive impedance could be observed for the previous CPL design, which reveals an early electric resonance at lower frequency and the bandwidth is therefore limited. Over the same frequency range of 40 GHz, the impedance evolves slower for the optimized CPL, and the resonance frequency is predicted to be 128 GHz instead of 60 GHz. Consequently, the frequency response curve in Figure 6 rolls down faster after 128 GHz.

5. Conclusions

In this work, an optimized coplanar waveguide GSG line is designed and proved to induce little parasitic effect on the bandwidth performance of an evanescently coupled waveguide uni-traveling carrier photodetector. Measurement and simulation results compared with our previous work show a significantly reduced parallel capacitance to the PD junction for the optimized CPL, and a remarkable rise in bandwidth up to 120 GHz. The CPL parasitic capacitance weighs much less than the junction, and the bandwidth of the CPL itself amounts to 280 GHz, which means a predictable higher PD bandwidth if the junction capacitance could be further reduced. For the device in this work, the active area is 50 μm^2, which is twice or even three times those with bandwidths over 200 GHz. If the area is shrunk to the same size, the shrunk junction capacitance may be controlled within 10 fF, in almost equal weight with the optimized CPL, and the PD bandwidth could be raised again. Theoretically, the PD bandwidth is determined by both carrier transit time and resistance–capacitance (RC) circuit response time, where the transit-time limited bandwidth for the epi-structure in our work is estimated to be 310 GHz. For most UTC-PDs designed for high-speed applications and mentioned above, the transit time is usually a less limiting factor, while RC response time takes dominance. Through the simulation results on our previous CPL design, it is found that the CPL itself could achieve high RF loss as the frequency increases, concealing the merit of the small junction area. Therefore, the CPL frequency response should also be taken into consideration alongside the junction itself during device design.

The high bandwidth of the fabricated device also enables clear eye opening in the PAM4 100/140 Gbaud transmission test, indicating a high bitrate at 280 Gb/s. The photoresponsivity of the device achieves 0.476 A/W, with a low dark current of 3.84 nA at the

working condition, which reaches the same level as another very recent report from us featuring a 0.49 A/W high responsivity edge-illuminated UTC-PD with only 90 GHz bandwidth [21]. Additionally, considering the habitual practice of pre-emphasis and electrical amplification techniques used in actual optical transceivers, the fabricated device is quite promising for high-speed photodetection over 200 Gb/s/λ, or even higher for 400 Gb/s/λ.

Author Contributions: Device design, simulation and data analysis were performed by H.Y. (Han Ye). Chip fabrication and process design were performed by Q.H., L.G., and H.Y. (Han Ye). The first draft of the manuscript was written by H.Y. (Han Ye). Supervision and manuscript revision were performed by H.Y. (Hua Yang) and H.Y. (Han Ye). All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The datasets generated during the current study are available from the corresponding authors upon reasonable request.

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Conflicts of Interest: The authors declare no conflicts of interest.

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