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A Low-Power Comparator-Based Automatic Power and Modulation Control Circuit for VCSEL Drivers

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Abstract

This paper proposes an automatic power and modulation control (APMC) circuit that can directly detect the degradation of vertical cavity surface emitting laser (VCSEL) diodes by utilizing a novel voltage sensing mechanism, thereby eliminating the need for costly external monitoring photodiodes. Notably, the proposed APMC architecture facilely observes the performance degradation by sampling the voltage values at the upper node of the VCSEL diode during both modulation on and off states. The APC loop can perceive a 25 mV voltage drop that corresponds to a 0.5 mA increase in the threshold current, providing a 4-bit digital switch signal. Thereafter, it is delivered to the VCSEL diode driver to initiate compensation of the bias current. In the AMC loop, a 50 mV voltage drop equivalent to a 1 mA reduction in the modulation current is similarly detected to produce another 4-bit digital code. The proposed APMC IC is designed by using a 180 nm CMOS process and consumes a total power of 18.2 mW from a single 3.3 V supply.

Keywords: APC; AMC; LiDAR; optoelectronic; transmitter; VCSEL

1. Introduction

Light detection and ranging (LiDAR) systems have gained significant attraction in diverse applications, including autonomous driving, agriculture, archaeology, and smart home monitoring, due to their ability to acquire precise three-dimensional spatial information [1–4]. A typical direct time-of-flight (dToF) LiDAR sensor consists of a transmitter (Tx) that emits pulsed laser signals and a receiver (Rx) that detects the reflected light. The Tx plays a critical role because the quality and stability of the emitted pulses directly influence the measurement accuracy and the overall system reliability. Therefore, the development of a compact, energy-efficient, and high-performance Tx circuit has become a key focus in modern LiDAR sensor systems. In particular, VCSEL diodes are widely used due to their low cost, fast modulation capability, and ease of integration characteristics. However, VCSEL diodes suffer from performance degradation during operations, such as the increase in threshold current and the decrease in optical output efficiency with rising temperature, as shown in Figure 1 [5]. Specifically, a temperature increase of 50 °C typically leads to a threshold current increase of ~0.25 mA and a reduction in optical output power by approximately 1.2 mW [6], and this degradation is also accompanied by a voltage drop at the output node. This degradation often cannot be externally monitored in real time. Also, partial replacement is not feasible because VCSEL diodes are typically co-packaged with their driver chips, and therefore, an entire module must be replaced with a new one, resulting in considerable time and overhead costs.

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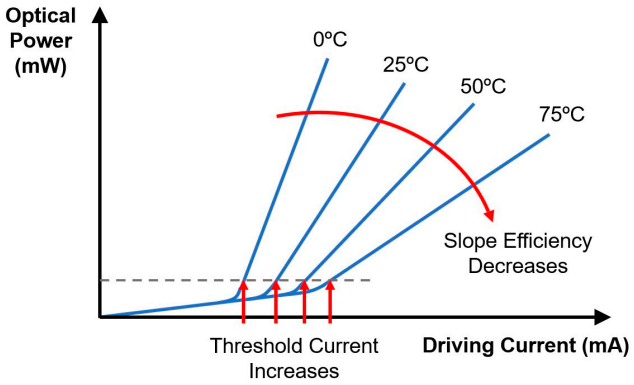


Figure 1. Conceptual output power–current characteristics of VCSEL diodes under varying temperature conditions.

Well-known mechanisms—namely, automatic power control (APC) and automatic modulation control (AMC) paths—have been frequently incorporated to internally detect and compensate for the performance degradation of VCSEL diodes, leading to the mitigation of this critical issue. Figure 2a illustrates the block diagram of a conventional implementation that typically employs a monitoring photodiode (MPD) alongside the VCSEL diode to detect its degradation directly [7–9]. However, this architecture requires additional components, including a narrow-bandwidth transimpedance amplifier (TIA) that results in large chip area and power consumption characteristics.

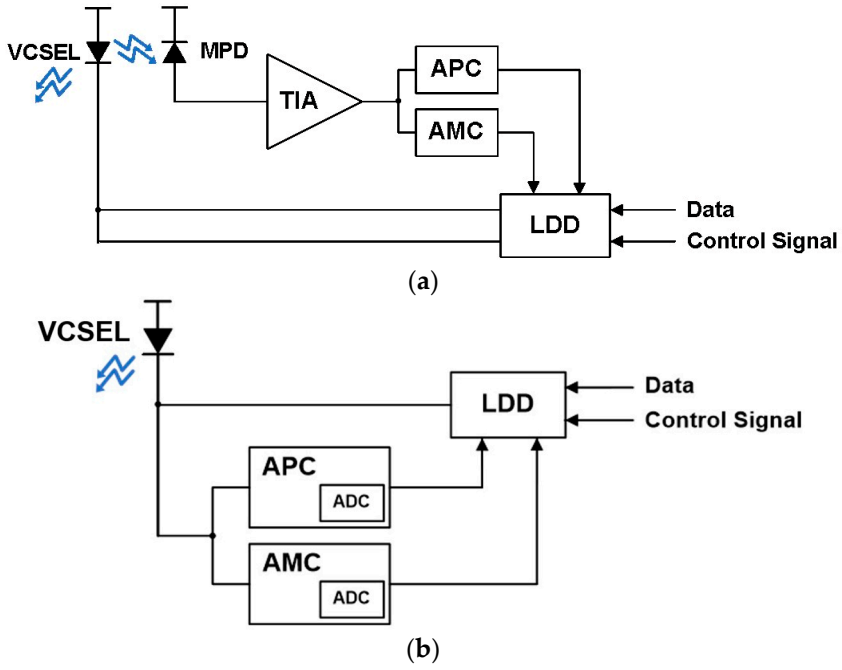


Figure 2. Block diagrams of VCSEL drivers with APC and AMC loops: (**a**) a conventional architecture with an MPD; (**b**) a conventional structure with no MPD.

It is also well known that VCSEL diodes are inherently unidirectional. Therefore, they cannot emit light signals toward both the output (i.e., targets in LiDAR systems) and the MPD simultaneously. For this purpose, either an optical splitter or an additional VCSEL dedicated for monitoring is often employed, consequently increasing the power consumption and the circuit complexity further. Recently, various structures have been proposed to improve integration [10]. As an example, Figure 2b shows another architecture in which the DC voltage drop in the VCSEL node is directly sensed without an MPD [11].

Nonetheless, this structure relies on the internal analog-to-digital converter (ADC) within the APC and AMC blocks, inevitably increasing the circuit complexity and resource usage. In addition, a prior APC-specific approach employing low-pass filters (LPFs) for voltage averaging mandates the use of capacitors, which are generally large in physical size. The inclusion of such components leads to an enlarged chip area, which is undesirable particularly for applications targeting high integration and low power consumption characteristics. Therefore, this paper proposes a comparator-and-counter-based automatic power and modulation control (APMC) circuit that can eliminate the requirements of MPDs, ADCs, or large passive components, thereby achieving improved compactness and system efficiency.

VCSEL degradation is detected by monitoring the voltage drop at the anode of the utilized VCSEL diode. When the sensed voltage falls below a predefined reference level, a logic '1' is generated by the comparator. Then, the logic-high outputs are counted using a digital counter, therefore resulting in a 4-bit digital code that represents the degree of degradation. All digital circuits are implemented by using full-custom design methodology.

2. Circuit Description

Figure 3 depicts the proposed architecture of this work in which the VCSEL diode's internal node voltage is sensed on-chip without the need of an MPD and a complicated ADC. Instead, a compact structure based upon comparators and counters is suggested, consequently producing digital control codes. Hence, this architecture can achieve significant reductions in both chip area and power consumption when compared to prior designs.

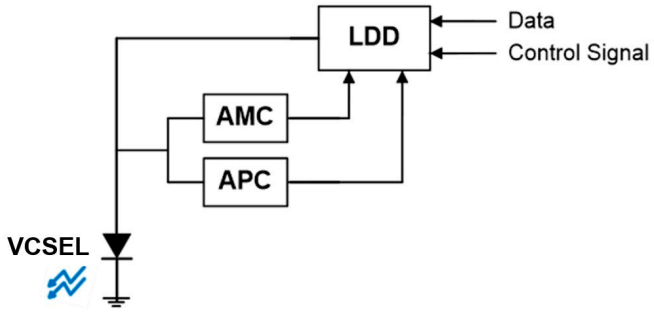


Figure 3. Block diagram of the proposed VCSEL driver with the APMC loop.

Figure 4 shows the overall block diagram of the proposed automatic power and modulation control (APMC) circuit that operates with an asynchronous clock generator. The voltage of the upper node (V_{LD}) of the VCSEL diode is detected through a buffer and used to determine how much the performance of the implemented VCSEL diode has been degraded. The following peak-detect-and-hold (PDH) circuit samples and holds the voltage (V_H) when the modulation is turned on, such that it can be processed later along with the voltage V_L that is defined as the value of V_{LD} when the modulation is turned off. Namely, V_H represents the peak voltage sampled by the PDH with the modulation on, while V_L corresponds to the buffer output V_{LD} observed with the modulation off.

Thereafter, these signals are processed through the APC and AMC paths. The operation of the APC is as follows: V_H (obtained from the PDH circuit) and V_{LD} (acquired from the initial buffer) are divided through two resistors (R) to generate an average voltage (V_C). Then, this V_C is sampled and held as V_{CS} by a sample-and-hold (S/H) circuit at the time when V_{LD} equals V_L, hence ensuring stable signal processing without being affected by the variations from the previous sampling stage. The following comparator takes V_{CS} as its input signal. Since the comparator has a threshold voltage, also known as the reference voltage at which compensation is required, its output (the penultimate APC signal) becomes a logical '1' when V_{CS} is below the threshold. Finally, this APC signal is fed into

a counter, which generates a 4-bit digital code, i.e., APC [3:0] that increments with each incoming '1'.

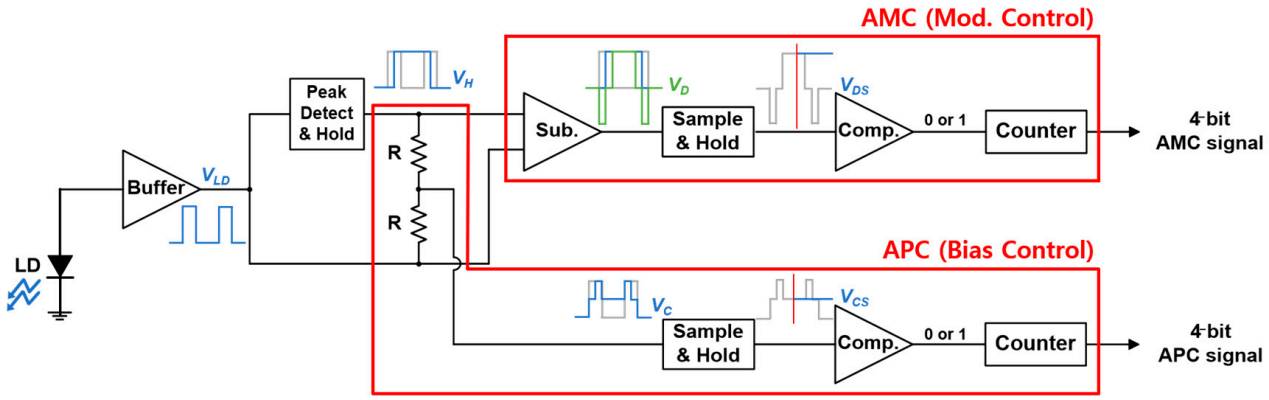


Figure 4. Block diagram of the proposed APMC circuit.

The operation of the AMC is as follows: V_H and V_L enter the subtractor circuit to extract the voltage component corresponding to the modulation current, generating the output V_D (= $V_H - V_L$). Then, this V_D is sampled and held as V_{DS} by the S/H circuit at the time when V_{LD} equals V_L, ensuring that it is processed stably regardless of the previous sampling. Similar to the APC path, the comparator takes V_{DS} to produce either a logical '1' or a logical '0' as the AMC signal. Finally, it is processed by a counter to generate a 4-bit digital code, i.e., AMC [3:0]. The timing diagram of data processing is shown in Figure 5.

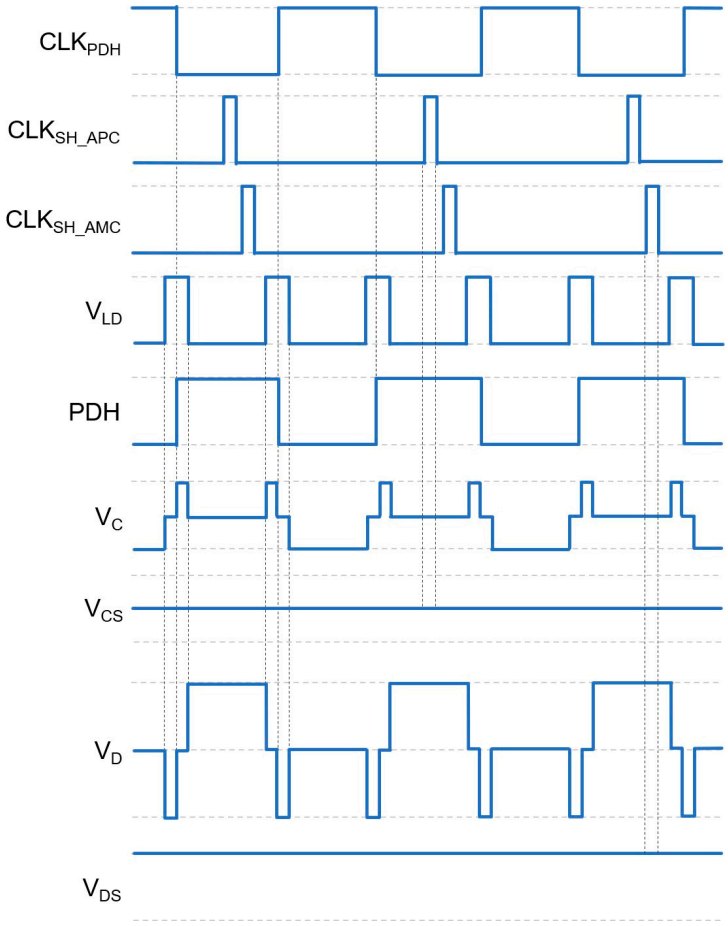


Figure 5. Timing diagrams of data processing in the APMC circuit.

Figure 6a shows the schematic diagram of the PDH circuit that shares the structure of a basic two-stage operational amplifier (OP-AMP) and is designed to detect and hold the peak of the output voltage. At the output of the OP-AMP, a capacitor (C) and a parallel NMOS switch (M6) are exploited for peak detection and reset. When the RESET signal is '1', M6 is turned on and rapidly discharges the stored charges in the capacitor, thus resetting the PDH circuit. When the RESET signal is '0', M6 is turned off and the capacitor is charged as the OP-AMP output increases due to the input signal, then holds at the peak voltage. Even when the OP-AMP output drops, the voltage stored in the capacitor can remain, allowing the PDH circuit to reliably hold the maximum input voltage. However, the reference current generated by R1 and diode-connected M8 in this circuit is sensitive to PVT variations. To alleviate this issue, a positive temperature-coefficient current generator and a negative temperature-coefficient current generator can be exploited to generate a more robust and stable reference current, which is then less affected by the PVT variations [12].

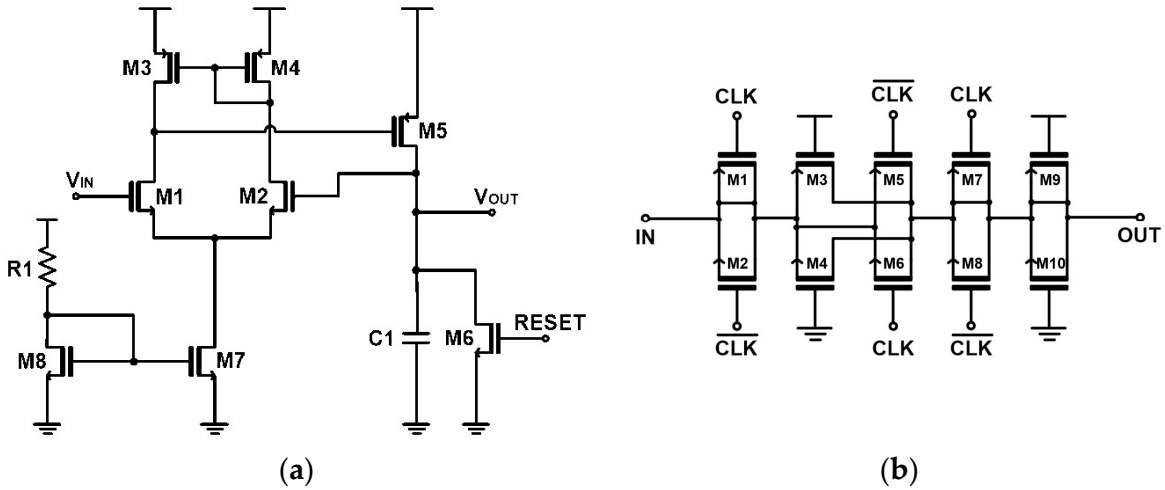


Figure 6. Schematic diagrams of the (**a**) PDH and (**b**) S/H circuits.

Figure 6b illustrates the schematic diagram of the S/H circuit, which uses a chain of MOSFET transmission gates (TG) to control the connection between the IN and OUT nodes depending on the clock signal (CLK), thereby enabling sampling and holding operations. Here, a TG chain structure including dummy switches is employed to suppress any voltage disturbance caused by the charge injection from the channel to adjacent nodes and to minimize inevitable mismatches. When the CLK is low ('0'), the IN and OUT nodes are disconnected. This allows the IN node to sample the voltage from the previous stage. As the CLK transitions to high ('1'), M5 and M6 are turned ON, thus forming a conductive channel that transfers the sampled voltage to the OUT node. When the CLK returns to low ('0'), M5 and M6 are turned OFF, disconnecting the IN and OUT and allowing the output node to hold the sampled voltage. Although this structure is simple, it provides stable operations and precise sampling control based only on the clock timing. The same S/H circuits are utilized for both the APC and AMC paths in this work, thereby allowing the sampled voltages during the modulation on and off states to be processed within the designated timing.

Figure 7 illustrates the schematic diagram of the clock-less asynchronous comparator that switches the output to high ('1') or low ('0') based on the MOSFET threshold voltage. When the input voltage is lower than the internally defined reference level, the PMOS-based pull-up path (M1, M2) conducts and drives the output to high ('1'). Conversely, if the input exceeds the reference, the NMOS-based pull-down path (M3, M4) is turned on, therefore

pulling the output to low ('0'). In addition, two more inverter buffers (M7~10) are included at the output to ensure clean and stable logic levels.

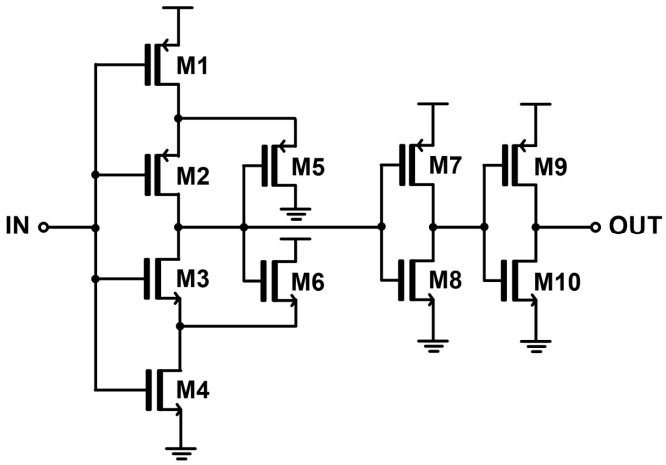


Figure 7. Schematic diagram of the comparator.

Figure 8 shows the block diagram of the subtractor and the detailed circuit schematic diagram of the fully differential amplifier (FDA) that is utilized to remove the common-mode DC voltages. Thereafter, a difference amplifier with a two-stage op-amp is used for the AC differential subtracting. It is noted that there exist alternative solutions utilizing op-amps, such as [13].

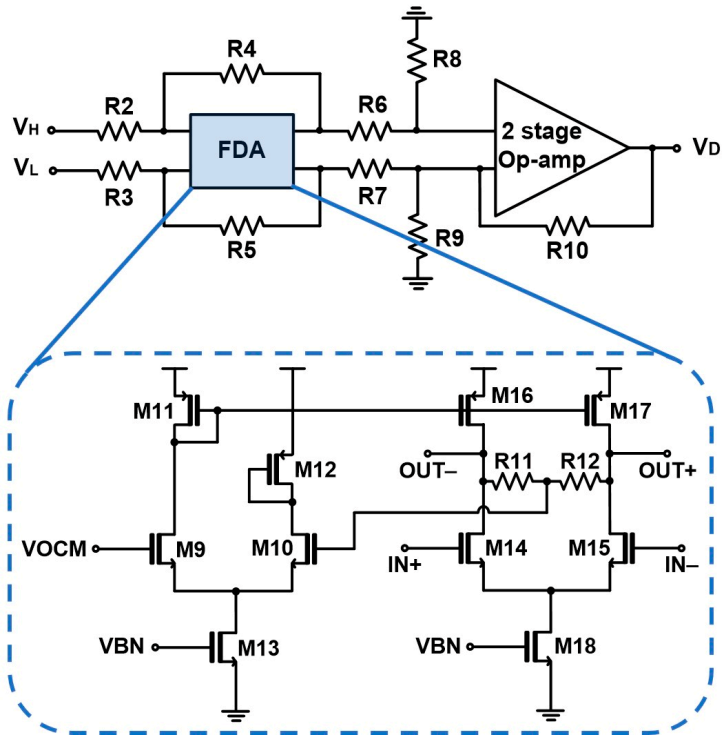


Figure 8. Block diagram of the subtractor with the schematic diagram of the FDA.

The FDA consists of two consecutive differential amplifiers, where the first stage (M9–M13) takes an external output DC voltage (V_{OCM}) at the gate of M9 so that M10 can define the common-mode level of the differential output via the output resistors R11 and R12. Members of the second differential pair (M14 and M15) receive V_H and V_L at the IN– and IN+ terminals, respectively, and generate an AC differential output. Then, the

FDA output is passed to the difference amplifier, thereby generating the final output (V_D) representing $V_H - V_L$.

Figure 9 shows the logic-level diagram of the counter that consists of four D flip-flops (D-FFs), generating a 4-bit digital code. The D input of the first D-FF is connected to VDD, and each Q output is connected to the D of the next D-FF. The clock is driven by either the APC or AMC signal. Therefore, each time the signal becomes logic high ('1'), one bit is sequentially transferred to the next Q. Consequently, the outputs from the APC [3:0] (or AMC [3:0]) sequentially transition through 0000, 0001, 0011, 0111, and 1111, generating a final 4-bit digital code with an increasing number of logic highs. The generated 4-bit signal is delivered to the current compensation circuit of the VCSEL diode driver, where it is used to gradually increase the compensation current.

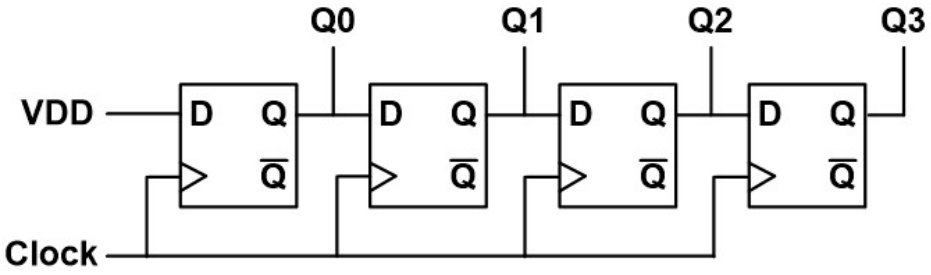


Figure 9. Logic-level diagram of the counter.

Figure 10 shows the logic-level diagram of the asynchronous clock generator that controls the sampling and holding timing of the PDH, S/H(APC), and S/H(AMC) circuits. With a single clock input (CLK_{IN}), three asynchronous clock signals, i.e., CLK_{PDH}, CLK_{SH_APC}, and CLK_{SH_AMC}, can be produced. All digital blocks implemented in the circuit are fully custom-designed.

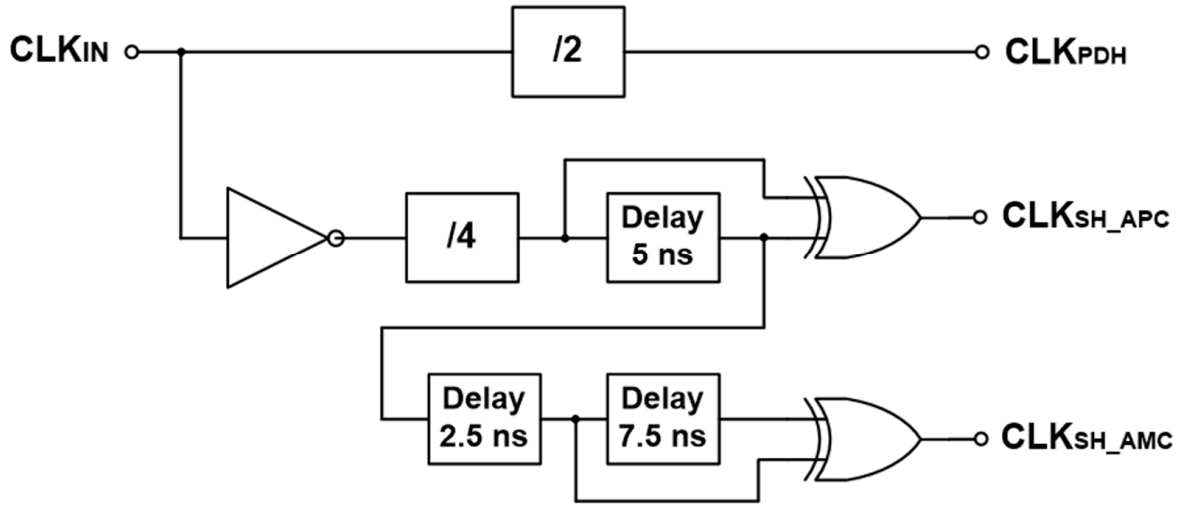


Figure 10. Logic-level diagram of the asynchronous clock generator.

3. Layout and Simulation Results

3.1. Layout

Figure 11 shows the layout of the proposed APMC circuit that is designed by using the model parameters of a standard 180 nm CMOS process with a total chip area of 1.5×2 mm^2 and a core circuit area of 484×234 μm^2. According to the post-layout simulation results, the DC power consumption is 18.2 mW from a single 1.8 V supply.

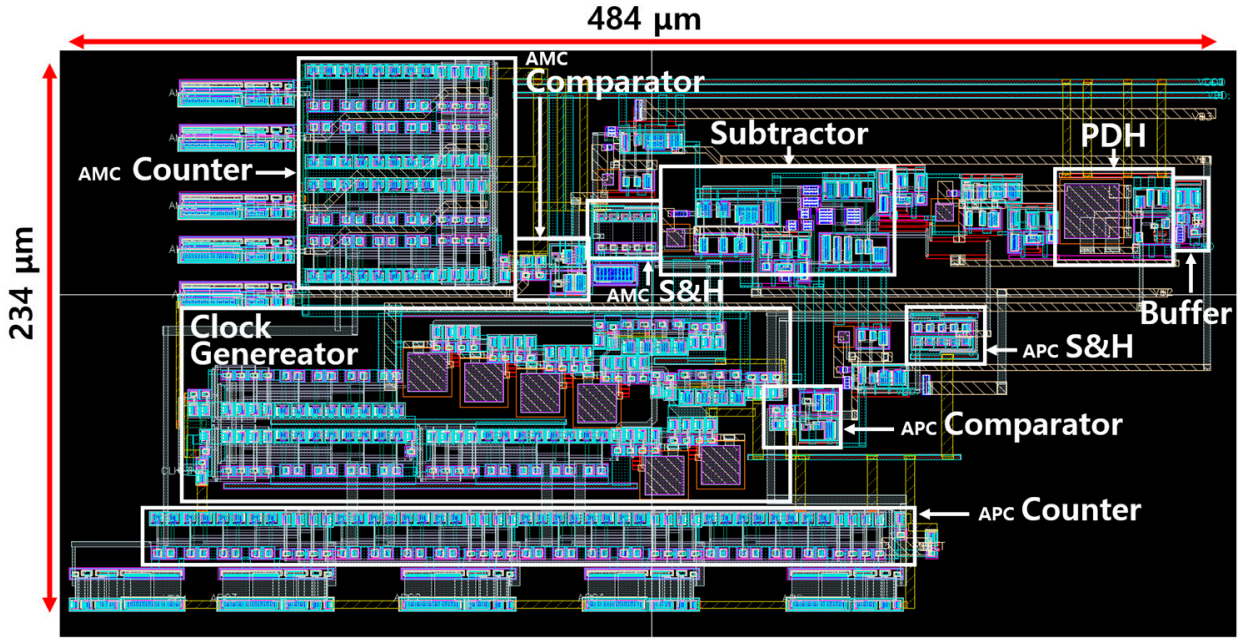


Figure 11. Layout of the APMC circuit.

3.2. Post-Layout Simulation Results

Figure 12 shows the simulation results of the asynchronous clock generator used in the proposed APMC circuit. Starting from a single input clock, three output clocks with different timings—labeled a, b, and c—are precisely generated.

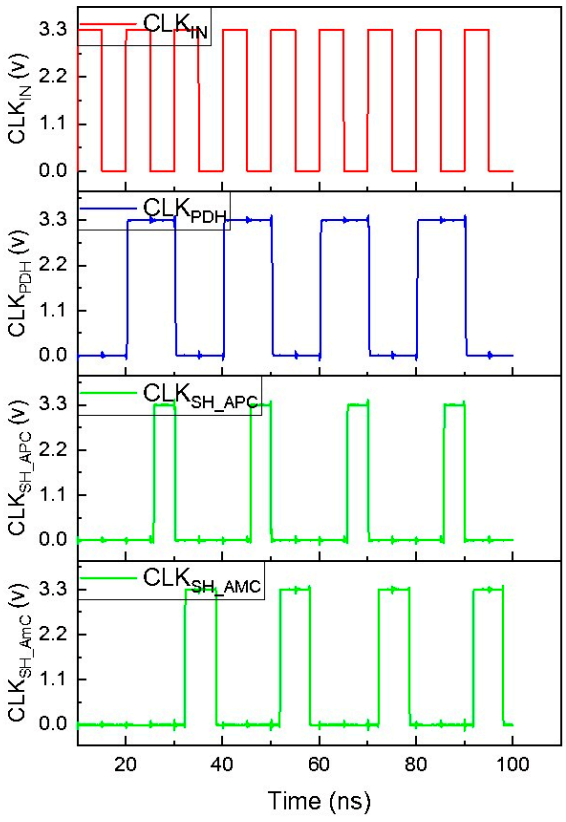


Figure 12. Simulation results of the asynchronous clock generator that generates CLK_{PDH}, CLK_{SH_APC}, and CLK_{SH_AMC} from a single input clock, CLK_{IN}.

Figure 13 presents the simulation results of the APC compensation path, where the condition for the APC compensation is defined as a 0.5 mA increase in the VCSEL threshold current. This appears as a 0.5 mA decrease in the average DC current and then a 25 mV decrease in the control voltage (V_C). The amplitude of each AMC pulse is held constant during this operation.

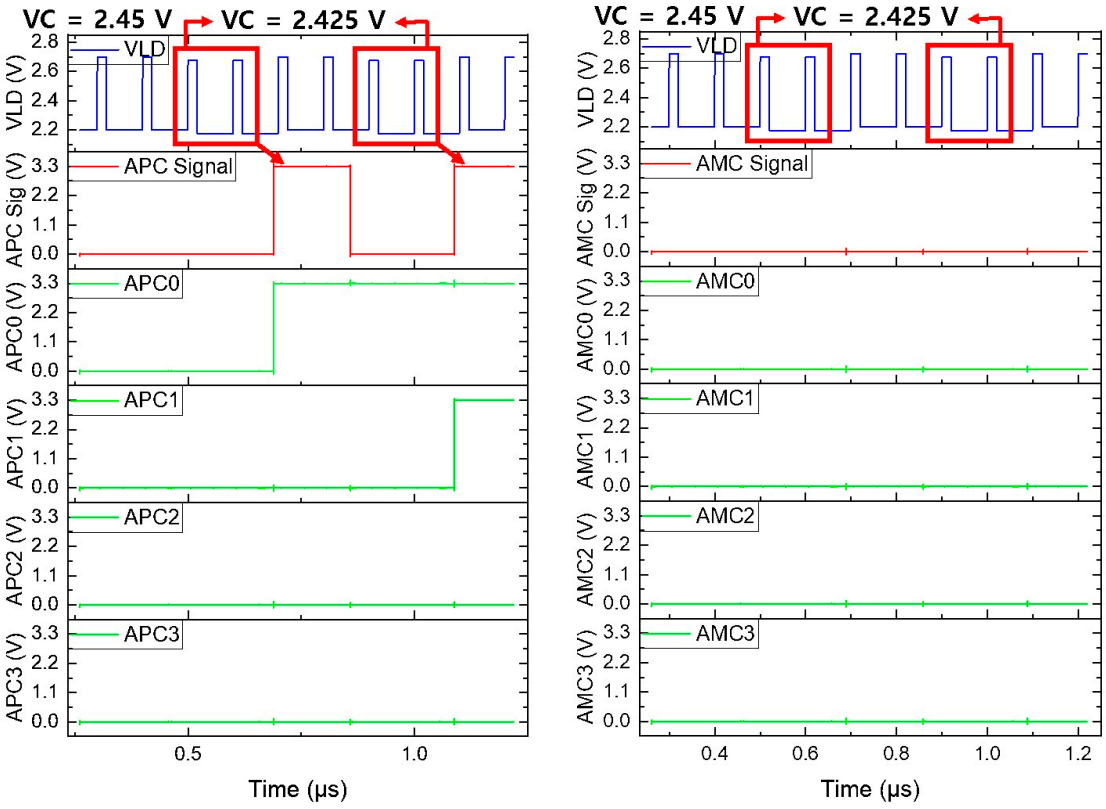


Figure 13. Simulation results of the APC and AMC paths under a condition that only requires APC compensation (V_C decreases 25 mV): (**a**) APC path and (**b**) AMC path. APC (AMC) [3:0] represents the number of APC (AMC) pulses counted.

When V_C decreases by 25 mV, the APC signal becomes a logic high ('1'). Then, both APC0 and APC1 are sequentially set to '1' with each occurrence. In contrast, the AMC signal remains at a logic low ('0').

Figure 14 shows the simulation results of the APMC circuit, where the AMC compensation condition is modeled as a 50 mV decrease in V_H while the V_L of each pulse remains constant. The 50 mV decrease in V_H corresponds to a 1 mA reduction in the modulation current, while the V_L of each pulse remains constant. When V_H decreases by 50 mV, the AMC signal becomes a logic high ('1'). Then, both AMC0 and AMC1 are sequentially set to '1' with each occurrence. As V_H decreases by 50 mV, the V_C also decreases by 25 mV, causing the APC path to operate in the same manner as the AMC path.

Figure 15 shows the simulation results of the counter circuit. Each time the input clock goes high, a logic '1' is sequentially transferred through Q0, Q1, Q2, and Q3, demonstrating the proper operations. In this circuit, the input clock corresponds to the APC (or AMC) signal, and its output Q [3:0] corresponds to the APC [3:0] (or AMC [3:0]). These results confirm the signal transitions at the third and fourth bits.

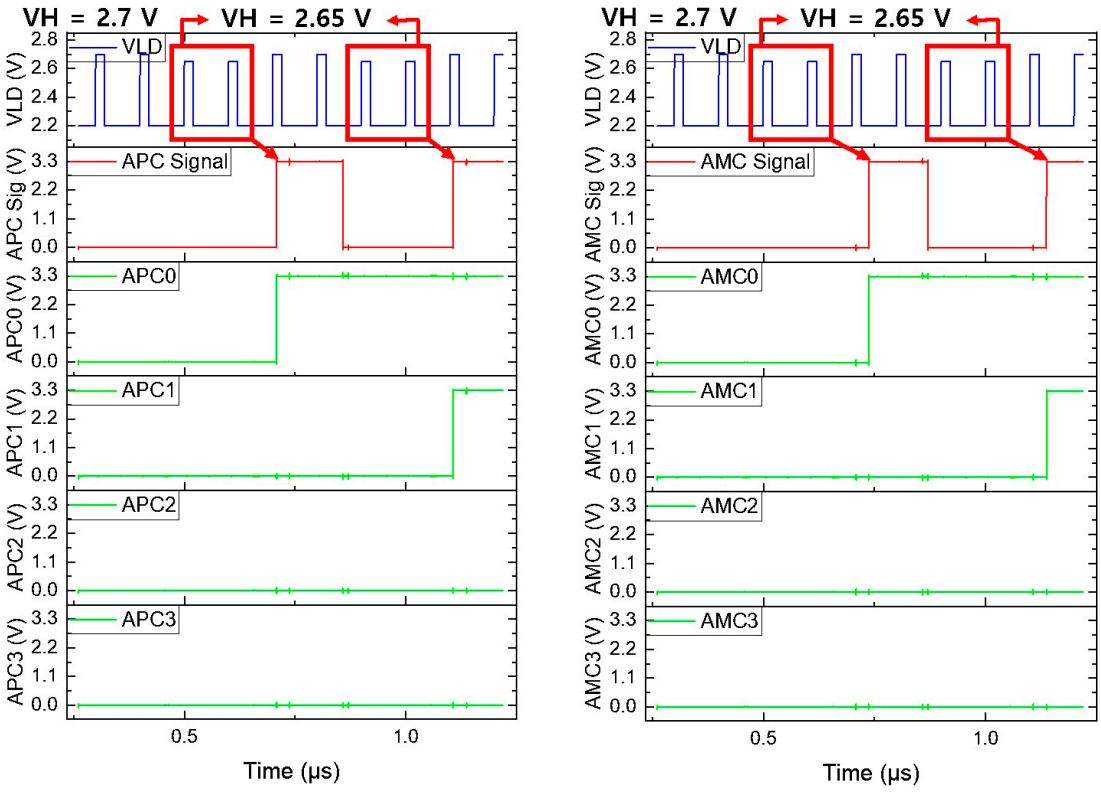


Figure 14. Simulation results of the APC and AMC paths under a condition that only requires AMC compensation (V_H decreases 50 mV): (**a**) APC path and (**b**) AMC path. APC (AMC) [3:0] represents the number of APC (AMC) pulses counted.

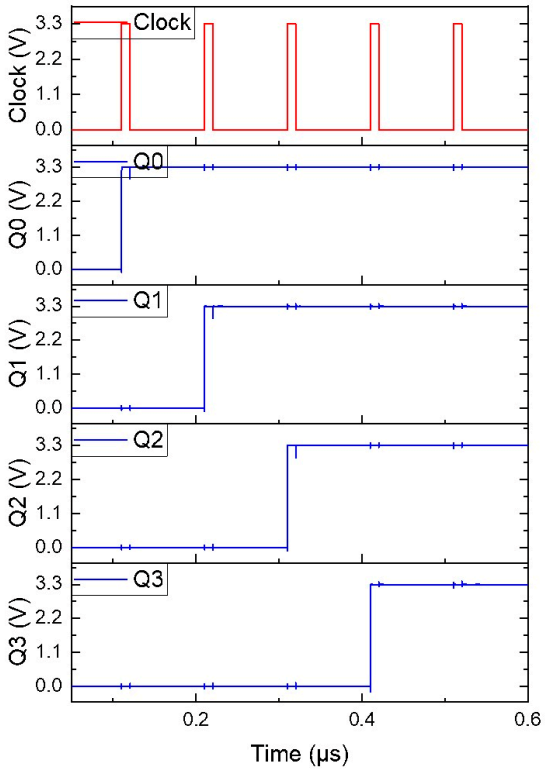


Figure 15. Simulation results of the counter which counts the number of times the clock signal is high (Clock: APC or AMC signal, Q [3:0]: APC [3:0] or AMC [3:0]).

Figure 16 presents the simulation results under the varying temperature conditions.

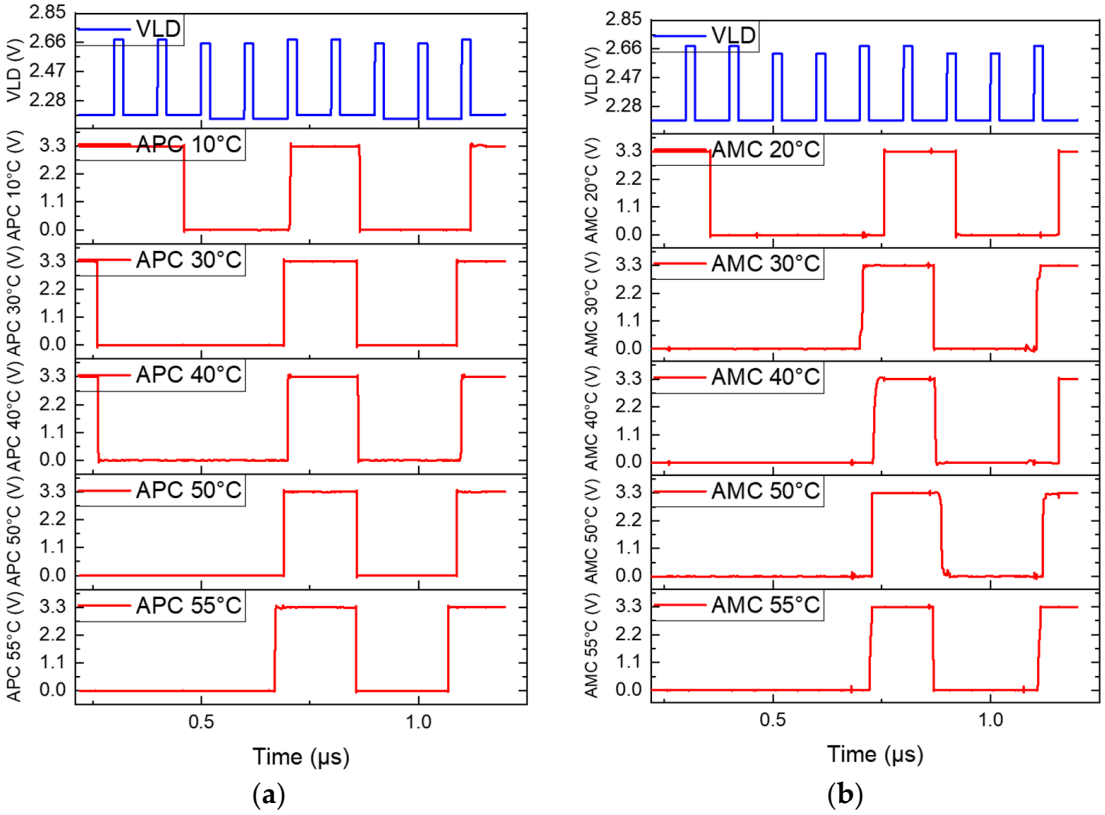


Figure 16. Simulation results of the APC and AMC loops under the varying temperature conditions: (**a**) the APC signals and (**b**) the AMC signals.

Figure 16a shows the APC signals when the APC loop operates over a temperature range of 10 °C to 55 °C. Figure 16b depicts the AMC signals when the AMC loop functions from 20 °C to 55 °C. In the AMC loop, the op-amp following the S/H stage has a reference voltage that varies with temperature, i.e., 1.706 V at 20 °C, 1.201 V at 30 °C, 940 mV at 40 °C, 838 mV at 50 °C, and 816 mV at 55 °C, respectively.

Table 1 compares the proposed APMC circuit with previously reported CMOS-based APC and AMC implementations. Ref [9] introduced the use of current, power, and temperature loops to compensate for the degradation of the laser diode (LD) performance. The current loop controlled the current through the LD in an analog manner via a low dropout regulator, while the power loop controlled the power in a digital manner through the MCU (microcontroller unit). The usage of these multiple loops and the control methods provided the stable operations of the laser diode across different operating conditions. However, the integration of the MCU led to a larger physical system, thus increasing the complexity of the setup.

Ref. [11] proposed an analog APC architecture that utilized a low-pass filter (LPF) to extract the average voltage. While the overall structure was relatively simple, the LPF required a physically large capacitor, thus resulting in an increased overall chip area. In addition, LPF-based approaches inherently produced ripples. In this case, a bias current ripple of approximately 0.5 mA was observed. The presence of such a ripple indicates that the VCSEL cannot be maintained in a stable manner. Furthermore, Ref. [11] addressed only the APC functionality without incorporating AMC.

Table 1. Performance comparison with previously reported CMOS APC/AMC ICs.

Parameters	[9]	[11]	[14]	[15]	This Work
CMOS Process (nm)	N/A	180	130	130	180
Optical Device	LD	VCSEL	VCSEL	VCSEL	VCSEL
Driver Type	Common Anode	Common Cathode	Common Cathode	Common Anode	Common Cathode
Monitoring Photodiode	Yes	No	No	No	No
Supply Voltage (V)	5	N/A	3.3	1.2/3.3	3.3
Max. Power Consumption (mW)	N/A	N/A	371 (with 4 CH VCSEL driver)	471.36 (with VCSEL driver)	18.2
Signal Type	Analog and Digital	Analog	Digital 10-bit	Digital 10-bit	Digital 4-bit
Processing Method	Controlled by LDO and MCU	LPF + Comparator	Flash + SAR ADC	Time-interleaved Flash + SAR ADC	Comparator + Counter
Chip Area (mm^2)	N/A	1.02 (chip)	4.247 (chip)	4.2 (chip)	0.131 (core)

Refs. [14,15] included the integrated VCSEL drivers and utilized flash ADCs, flash–SAR ADCs, or time-interleaved ADCs to generate digital control codes for the APC and the AMC operations.

In contrast, the proposed APMC circuit generates 4-bit digital control codes by using only a comparator and a counter, thereby eliminating the need for complex ADCs and leading to a highly compact architecture with a chip area of 0.131 mm^2. Also, the proposed APMC circuit does not require a monitoring photodiode, as it generates control signals based on the voltage of the VCSEL diode itself, therefore making it a simple and efficient analog APC and AMC structure suitable for low-power transmitter systems. Since the proposed work uses a 4-bit digital control word, it may seem short compared to previous works. However, the meaning of the digital code is very different in this work. In previous research, the digital codes mostly represented the values converted through ADCs, providing finer detection resolution with longer bit lengths. On the contrary, the proposed APMC in this work focuses on counting the compensation actions based on a reference voltage. Hence, longer bit lengths would simply allow for more compensation cycles.

4. Conclusions

This paper presents an analog integrated circuit for automatic power and modulation control (APMC) that directly senses the anode voltage of the VCSEL diode, eliminating the need for an external monitoring photodiode. The proposed APMC circuit detects a 25 mV drop corresponding to a 1 mA increase in the threshold current in the APC path and a 50 mV reduction in modulation voltage caused by optical conversion efficiency degradation for the AMC path. Using a compact comparator-and-counter-based architecture, the circuit generates 4-bit digital control codes for both APC and AMC paths without the need for high-speed ADCs.

The APMC circuit, designed in a 180 nm CMOS process, operates with a low power consumption of 18.2 mW from a single 3.3 V supply. This simple and low-power design makes the proposed APMC solution suitable for compact and cost-effective LiDAR transmitters. Moreover, it can be easily integrated into existing transmitter systems to ensure long-term performance reliability, hence offering a significant advantage in terms of both size and energy efficiency.

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