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Preliminary Study on Automatic Detection of Hard Defects in Integrated Circuits Based on Thermal Laser Stimulation

Wenjian Wu [1,2], Yingqi Ma [1,3,*], Minghui Cai [1,3] and Jianwei Han [1,3]

[1] National Space Science Center, Chinese Academy of Sciences, Beijing 100190, China; wuwenjian20@mails.ucas.ac.cn (W.W.)
[2] School of Electronic, Electrical and Communication Engineering, University of Chinese Academy of Sciences, Beijing 100049, China
[3] School of Astronomy and Space Science, University of Chinese Academy of Sciences, Beijing 100049, China
* Correspondence: myq@nssc.ac.cn

Abstract: Locating the fault position is a crucial part of the failure mechanism analysis of integrated circuits. This paper proposes a hard defect locating system based on Thermal Laser Stimulation (TLS) technology. The equation for laser-induced changes in the electrical parameters of semiconductor devices is a good guide to the hardware and software design of the hard defect locating system. The scanning mode of fast total scanning combined with slow point-to-point scanning can quickly locate abnormal areas. A modified median absolute difference (MAD) method is applied to the extraction of anomalous data. The system software can automatically and collaboratively control the 3D mobile station, laser, and signal acquisition unit. It also can intuitively display the distribution of abnormal points on the infrared image. Using a failure MRAM chip and a good one to conduct a comparative test, the abnormal points distributed on the infrared image of the chip indicate that the failure area is in the digital module or eFuse module of the chip, and the Emission Microscopy (EMMI) experiment also verifies the accuracy of the test system.

Keywords: hard defect; thermal laser stimulation; scanning mode; abnormal signal extract; EMMI

Citation: Wu, W.; Ma, Y.; Cai, M.; Han, J. Preliminary Study on Automatic Detection of Hard Defects in Integrated Circuits Based on Thermal Laser Stimulation. *Photonics* **2023**, *10*, 540. https://doi.org/10.3390/photonics10050540

Received: 22 March 2023
Revised: 3 May 2023
Accepted: 5 May 2023
Published: 6 May 2023

1. Introduction

With the decreasing size and increasing complexity of Integrated Circuits (ICs) processes, it is increasingly difficult to locate defects in integrated circuits. Therefore, defect location plays an important role in IC failure analysis, which cannot be achieved without the development of various failure analysis techniques. There are different localization techniques for different failure principles, such as micro-optical microscopy (PEM) for PN junction leakage and latch-up [1–3], Optical Beam Induced Resistance Change (OBIRCH) for meta or poly bridge defects [4–6], Thermal Emission Microscopy (EMMI) for via/contact resistance anomaly, and dielectric leakage [7–9].

Many studies have been conducted on the application of the OBIRCH technique: Ref. [10] proposed a numerical aperture increasing lens (NAIL) technology to increase image resolution. Ref. [11] proposed a design to increase the resistance value of the measurement circuit to improve the fault isolation success of the system in measuring short-circuit defects. Ref. [12] described a method to locate the IC leakage current by combining IR-OBIRCH and PEM techniques. The OBIRCH technique is part of the Thermal Laser Stimulation (TLS) technique. TLS technology contains the OBIRCH technique, the Thermally Induced Voltage Alteration (TIVA) technique [13], and the SEI technique [14]. The Seebeck effect (SEI) signal affects the OBIRCH signal in thermal laser localization experiments [15,16]. A simulation model of OBIRCH and TIVA was proposed early [17], and there is also a study on the models of TLS [18]. However, no one has constructed a corresponding defect localization system based on an analytical model of TLS.

In this paper, a design method for a static defect localization system based on TLS technology is proposed. The system consists of a hardware part and a software part. First, the paper gives the equations for the temperature change of the metal wire, diode, and MOSFET during 1310 nm continuous laser heating, and the equations for the change of electrical parameters due to the temperature change. Then, the paper describes the hardware design of the system and how the software can automatically control the laser, mobile stage, and data acquisition unit. Several methods to help users quickly locate defects in the system are presented, including the scanning method, eliminating the Seebeck signal, and extracting the anomaly signal. Finally, the localization experiment on the MRAM sample verifies the localization capability of the system, and the integrated localization accuracy can reach 1 μm. The system can provide good help for the failure analysis of the device.

2. Model of TLS

When laser irradiates the Integrated Circuit(IC), the thermal stimulation will cause the temperature of the material to rise, and the temperature rise will affect the carrier density and mobility, resulting in a change in resistivity [17]. TLS technology locates these defect points by identifying the resistance changes. TLS technology includes three subtechnologies: OBIRCH, TIVA, and SEI, as shown in Figure 1. OBIRCH technology uses a constant voltage source to supply power to the Device Under Test (DUT), measures the change in current to measure the resistance change, and then locates the defect point. TIVA technology uses a constant current source to supply power to the DUT, measures the change in voltage to measure the resistance change, and then locates the defect point. When there is a temperature difference, the diffusion of carriers inside the material will create a potential difference. SEI technology locates the defect point by detecting abnormal voltage changes at the defect point [19].

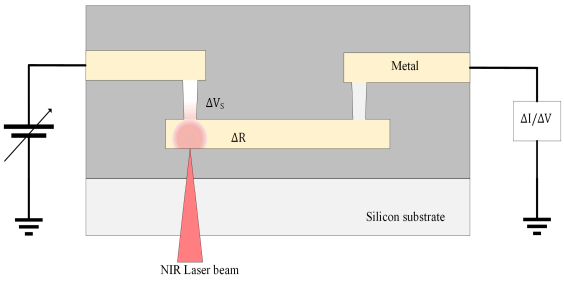


Figure 1. The laser thermal effect affects the change of electrical parameters.

To reasonably set the parameters of the system scanning and positioning, we also need to conduct an in-depth analysis of the influence of the parameters of the laser device on the electrical parameters.

For metal wiring, when a device is biased with a constant voltage V_0, the variation of current ΔI is [20]:

$$\Delta I = \frac{V_0}{R + \Delta R} - \frac{V_0}{R} \approx -\frac{\Delta R}{R^2} V_0 \quad (1)$$

When a device is biased with a constant current I_0, the variation of current ΔV is [20]:

$$\Delta V = I_0(R + \Delta R) - I_0 R = \Delta R I_0 \quad (2)$$

R is the fixed resistance of the circuit, and ΔR is the change in resistance due to thermal change. According to the resistance formula, suppose the laser irradiation region is modeled as a small metal region of length Δl and cross-sectional area ΔA and scanned along the X-axis, ΔR can be calculated from Equation (3) as follows:

$$\Delta R = \int \Delta\rho \frac{dl}{A} = \int \rho_0 \alpha_{TCR} \frac{\Delta T}{A} dl = \rho_0 \alpha_{TCR} \frac{\Delta l}{\Delta A} \Delta T \quad (3)$$

Combined with Formula (3), under the condition of constant voltage bias, the current change of the metal resistor is:

$$\Delta I_{TLS} = \frac{\rho_0 \alpha_{TCR} \Delta l V_0}{R^2 \Delta A} \Delta T \quad (4)$$

For a diode, the PN junction of the diode is considered an ideal PN junction, the Shockley equation is satisfied between the forward current and the voltage, the terminal current is completely a diffusion current, and the current variation formula with temperature is [21]:

$$I_f \propto T^{3+\gamma/2} \exp\left(\frac{eV_F - E_g}{k_B T}\right) \quad (5)$$

where γ is a constant related to the carrier coefficient and concentration; e is the charge of the electron; E_g is the band gap; k_B is the Boltzmann constant; and V_F is the voltage across the diode. When the applied voltage V_0 is less than the forward voltage of the diode V_{th}, $V_F = V_0$. When V_0 is greater than V_{th}, $V_F = V_{th}$, the typical value of V_{th} is 0.5–0.8 V for silicon diodes, and the value of E_g is 1.169 eV. Therefore, $eV_F - E_g < 0$. The e-function value increases with temperature.

For the MOSFET, when the device is in the saturation region, the drain current is i_D as follows [22]:

$$I_D = \frac{\mu C_{OX} W}{2L} (v_{GS} - V_T)^2 \quad (6)$$

where W is the channel width; L is the channel length; C_{OX} is the capacitance per unit area of the gate oxide layer; v_{GS} is the gate bias voltage; V_T is the threshold voltage; and μ is the carrier mobility. The specific formula of μ is as follows:

$$\mu = \mu_0 \left(\frac{T}{300}\right)^{-\theta} \quad (7)$$

where μ_0 is the carrier mobility at 300 K; θ is an empirical value; and V_T is legate conduction threshold voltage [23]:

$$V_T = 2\varphi_F + \frac{K_s l_0}{K_0} \sqrt{\frac{4eN_A\varphi_F}{K_s \varepsilon_0}} \quad (8)$$

where φ_F is the reference voltage of the semiconductor impurity concentration; K_s is the dielectric constant of the semiconductor; l_0 is the thickness of the oxide layer; K_0 is the dielectric constant of the oxide layer; N_A is the total number of acceptor atoms; and ε_0 is the dielectric constant of the oxide layer.

$$\varphi_F = \frac{k_B T}{e} ln\left(\frac{N_A}{n_i}\right) \quad (9)$$

where k_B is the Boltzmann function; e is the charge of an electron; N_A is the total number of atoms in the acceptor; and n_i is the intrinsic carrier concentration.

$$n_i = 2\left(\frac{2\pi k_B T}{h^2}\right)^{\frac{3}{2}} (m_n m_p)^{3/4} e^{-\frac{E_g}{2k_B T}} \quad (10)$$

where h is the Planck constant, and m_n and m_p are the effective masses of electrons and holes, respectively.

Firstly, the Formulas (6)–(10) are derived, then n_i', φ_F', V_T', μ' are substituted into ΔI_D, which leads to the change in MOSFET's electrical parameter caused by temperature,

$$\Delta I_D = \frac{\mu C_{OX} w}{L}(v_{GS} - V_T)\left(\frac{E_g}{2e} - \varphi_F\right)\left(2 + \frac{4eN_A l_0}{K_0 \varepsilon_0}\left(\frac{4eN_A \varphi_F}{K_s \varepsilon_0}\right)^{-1/2}\right)\frac{\Delta T}{T} - \frac{\theta\, \mu_0\, C_{OX}\, w}{600L}(v_{GS} - V_T)^2 \left(\frac{T}{300}\right)^{-(\theta+1)} \Delta T \quad (11)$$

Assume that the laser obeys a Gaussian distribution in space; when the laser is incident on the material, the coordinate values of the x- and y- axes are much larger than the value of the z-axis, and TLS technology generally provides two-dimensional positioning coordinates. Therefore, we ignore the case of z-axis conduction. We let the spot incident on the surface of the material be the minimum spot; the scanning speed is v, and the Gaussian laser heat source $\mathrm{Q}(x, y, \mathrm{t})$ can be expressed as follows [17]:

$$\mathrm{Q}(x, y, \mathrm{t}) = \frac{(1 - R_m)P_0}{\pi {\omega_0}^2} \exp\left(-\frac{(x - vt)^2 + y^2}{{\omega_0}^2}\right) \quad (12)$$

where R_m is the reflectivity of the material surface to the laser; P_0 is the power of the laser incident on the material surface; and ω_0 is the minimum spot radius of the laser. According to Fourier's heat transfer law, the heat conduction equation is:

$$\rho c \frac{\partial T}{\partial t} - k\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2}\right) = \mathrm{Q}(x, y, \mathrm{t}) \quad (13)$$

where ρ is the density of the material; c is the specific heat capacity; and k is the thermal conductivity. Considering the scanning area as infinite, the first type of boundary conditions is:

$$T(\vec{r}, \mathrm{t})|_{|\vec{r}| \to \infty} = T_0, \qquad T(\vec{r}, \mathrm{t})|_{|\vec{t}| \to \infty} = T_0 \quad (14)$$

To solve the above equation, we assume that the temperature $T(x, y, t)$ of the irradiated surface is affected by the heat flow at any location (x', y') at any time t':

$$T(x, y, t) = \int_0^t dt' \iint_{\Sigma} G(x, y, t; x', y', t') \frac{Q(x', y', t')}{\rho c} dx' dy' \quad (15)$$

where Σ is the area where the chip is irradiated, and $G(x, y, t; x', y', t')$ is the Green's function.

$$G(r', \mathrm{t}'; \mathrm{r}, \mathrm{t}) = \frac{\rho c}{4\pi k(\mathrm{t}' - \mathrm{t})} \exp\left(-\frac{(x' - x)^2 + (y' - y)^2}{4\pi(t' - t)}\right) \quad (16)$$

Where $\mathrm{D} = \frac{k}{\rho c}$, and $r^2 = (x - x')^2 + (y - y')^2;\ t' > t$. When Equations (12), (13), and (16) are combined with the first type of boundary conditions (14), we can obtain the temperature change formula after integration.

$$T(x, y, t) = \frac{(1 - R_m)P_0}{\sqrt{\pi \rho c}} \int_0^t \frac{exp\left(-\frac{(x - vt')^2 + y^2}{{\omega_0}^2 + 4Dt'}\right)}{\sqrt{t'}({\omega_0}^2 + 4Dt')} dt' \quad (17)$$

where v is scanning speed. The laser scans cyclically along the x-axis, with an interval of Δy on the y-axis. The points that experience the smallest temperature increase during the scanning heating process are $(x, y - \Delta y/2)$ and $(x, y + \Delta y/2)$. The minimum change in temperature for the entire heated area is obtained.

$$\Delta T = \frac{P_0(1 - R_m)}{\sqrt{\pi \rho c}} \sum_{i=1}^{t/\Delta t} \frac{exp\left\{-\frac{[v(t - \Delta t \times i)]^2 + (\frac{\Delta y}{2})^2}{{\omega_0}^2 + 4D(t - \Delta t \times i)}\right\}}{\sqrt{t - \Delta t \times i}[{\omega_0}^2 + 4D(t - \Delta t \times i)]} \quad (18)$$

When Equations (4) and (18) are combined, Equation (1) can be converted into:

$$\Delta I = -V_0 \frac{P_0(1-R_m)\rho_0\alpha_{TCR}\Delta l}{R^2\Delta A\sqrt{\pi\rho c}} \sum_{i=1}^{t/\Delta t} f(x,y,v,t) \tag{19}$$

Equation (2) can be converted into:

$$\Delta V = I_0 \frac{P_0(1-R_m)\rho_0\alpha_{TCR}\Delta l}{\Delta A\sqrt{\pi\rho c}} \sum_{i=1}^{t/\Delta t} f(x,y,v,t) \tag{20}$$

where:

$$f(x,y,v,t) = \frac{exp\left\{-\frac{[v(t-\Delta t\times i)]^2+(\frac{\Delta y}{2})^2}{{\omega_0}^2+4D(t-\Delta t\times i)}\right\}}{\sqrt{t-\Delta t\times i}[{\omega_0}^2+4D(t-\Delta t\times i)]} \tag{21}$$

According to Equation (18), the system can calculate the temperature change of different devices based on scanning speed, laser energy, spot size, and other parameters we set, thereby assisting users in setting reasonable scanning parameters. At the same time, to protect the device from being damaged due to excessive laser heating temperature, it is also necessary to use the above formula to limit the parameter setting range. From Equations (4), (5), and (11), it can be noted that the change in the electrical parameter is negative when the laser heats the metal interconnection wires, the change is positive when the laser heats the diode, and the change may be positive or negative when laser heats the triode. Therefore, we can judge the type of damaged components in the IC preliminarily according to the positive or negative of the measured electrical parameter change value.

3. Testing System

3.1. Composition and Working Principle of the System

Figure 2 is a scheme of the hard defect scanning and testing system [18]. It includes a laser energy control unit, an image acquisition unit, a mechanical motion unit, a data acquisition unit, a computer, etc. The defect location system's working process is as follows: Firstly, the system will obtain the electrical signal through the data acquisition unit and coordinate data through the mechanical motion unit synchronously with the DUT under the infrared laser. Second, the application software processes the electrical signal data. Finally, the defect position can be obtained by coordinating information corresponding to the abnormal data point.

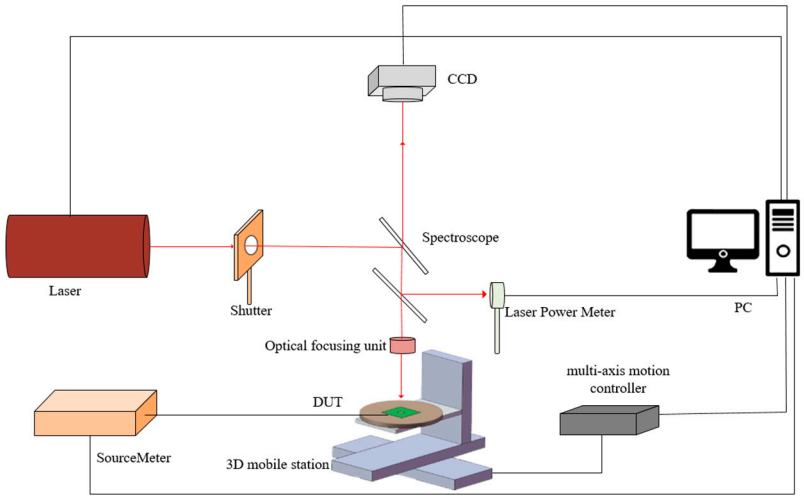


Figure 2. The framework of hard defect laser scanning and testing system.

The system uses a three-dimensional moving table to move the sample to be measured to scan and heat the sample. The static defect spot location information is obtained from the moving table's x- and y-axis coordinates output. The spot size affects the size of the heating area. Although it affects the setting of the longitudinal scan interval, it does not affect the specific transverse position during the moving scan because the transverse scan will experience all positions in the transverse direction.

When the energy of the scanning beam is greater than the bandgap of silicon, the thermal effect will dominate [24]. Therefore, we select a 1310 nm wavelength laser as the stimulation source. Due to the higher absorption rate of infrared light by infrared cameras, the same amount of absorption of laser energy by infrared cameras has a higher risk of damage. Therefore, we chose Si-CCD cameras to detect the scanning status during laser scanning. Today's IC employs multiple levels of metal that obscure lower conductor levels, which makes IC front-side examination techniques either difficult or impossible to apply, and most defects need to be irradiated from the IC backside [25]. When the laser is reflected by the surface of the chip substrate, it forms the first light spot on the Si-CCD and passes through the substrate, forming the second light spot by the reflection of metal wire [26]. Using the image binarization algorithm to treat the spot graphic, we can calculate the light spot diameter. The maximum electric parameter changes are caused by laser heating on metal wires or heavily doped semiconductor regions. By observing the imaging effect of the second light spot, we can determine the most suitable heating depth inside the chip (corresponding to the Z-axis value) [27]. The system uses a high-precision moving stage with an accuracy of up to 1 μm. Although the laser with a wavelength of 1.3 μm will produce an Airy spot of not less than 1 μm^2, the internal light intensity of the Airy spot is approximately Gaussian distributed, and the temperature field generated by the spot at different locations still differs. If this difference can be identified, the positioning accuracy of 1 μm can be achieved. The system source measurement unit can provide a four-quadrant operating power supply for the sample, with a maximum output of 10 A and a maximum voltage of 1100 V, which can meet the operating conditions of most devices.

3.2. Software Control

Figure 3 shows the control structure of the system software for the mobile table, the laser source, and the signal acquisition part. The software controls the irradiation of the laser source using a shutter. Before the scanning experiment, it is necessary to set the mobile stage's scanning operation scheme and the device's operating voltage or current. After the start of the run, the software automatically opens the shutter, and the power supply starts moving the sample. Two software threads synchronize to obtain the coordinates and electrical parameters of the moving table and then pass the data to the main thread and display it in real-time. After the scanning program is completed, the software automatically turns off the shutter and the energy output of the source meter.

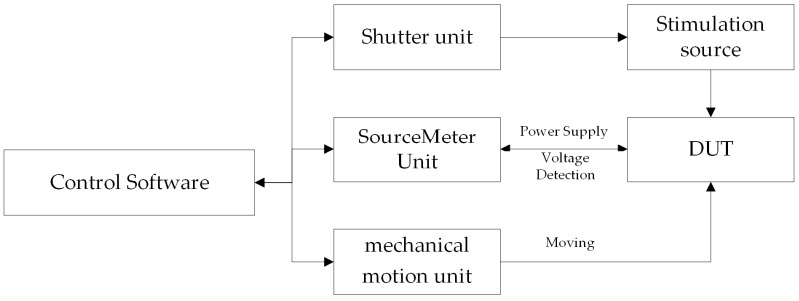


Figure 3. The control structure of the system software.

4. Methodology

This section describes the ways to improve system reliability, including the operating mode of scanning and location, eliminating the influence of the Seebeck effect, and extracting the defect spots from test data when encountering different samples.

4.1. Scanning Method

The system defaults to a 50× objective and divides the scanning process into two parts: fast and slow scan modes. The fast scan mode has a high scanning speed; however, it is affected by the coordinate output of the moving table, the sampling rate of the source table, and the running speed of the control software, which cannot obtain all the coordinate information and affects the positioning accuracy. In the fast scan mode, the device can be set with more considerable laser power and voltage or current value bias to obtain a higher thermal response. We can also appropriately reduce the scan speed to obtain enough sampling heating time and more sampling data for each point. The slow scan mode uses point-to-point scanning when the laser spot size is fixed. Consistent with the Section 2, we consider the laser spot to have a consistent light intensity distribution within its focused spot size ω_0, divide the active area into individual points concerning the spot size, then perform point-by-point scanning. Scanning speed and laser power affect the heating temperature in the whole system. We can reduce the test time by increasing the scanning speed and obtaining sufficient temperature rise by an internal laser power adjustment. The time required to change the electrical parameters due to temperature change is negligible compared to the temperature rise.

In the actual scanning process, we first use the fast mode to determine the distribution of anomalies in the device. Then, we should reduce the scan speed and laser power in slow mode. Finally, the system will scan the marked area point by point to determine the exact coordinates of the defects.

As shown in Figure 4, area A indicates the fast scan area and area B indicates the slow scan area we chose. C is the area affected by laser heating. A certain additional distance Δx needs to be set to ensure a uniform scanning speed. Δy is the vertical interval of the scan path, and its value is determined by the laser energy, spot size, and scanning speed. By preliminary analyzing the laser heating formula and summarizing the experimental data, we can know the temperature value decreases by about one-third at a distance of two times the diameter of the principal laser center, so we recommend that the value of Δy be set to no more than twice the laser diameter. Before scanning starts, we need to adjust the mobile platform to let the substrate surface on the same horizontal surface, and set reasonable laser energy and scan speed to ensure that all areas have sufficient temperature rise during laser irradiation.

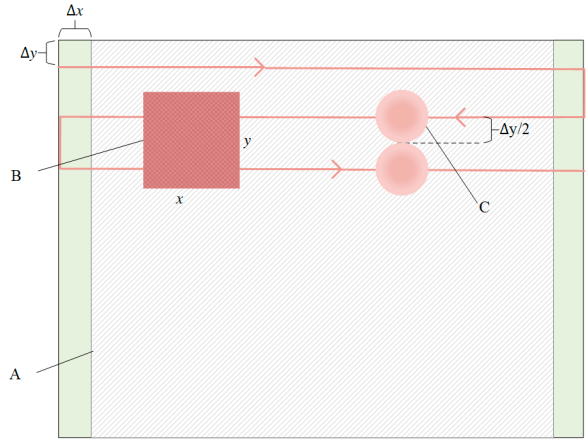


Figure 4. Shows the system software scanning method.

By analyzing Equation (17), we can see that an increase in laser power of 10 mW will result in a temperature increase of 42 degrees (with sufficient heating time). In order to make the current change significant, the current change should be at least twice that of room temperature, so the temperature change should be greater than twice that of room temperature. The working temperature of typical industrial devices does not exceed 85 °C. Therefore, to ensure that the heating temperature does not exceed the device's working temperature and that there is sufficient current change, we recommend setting the laser power to be greater than 5 mW but not more than 20 mW. The scanning speed has a small impact on the temperature rise, but the real-time sampling speed of the system limits its fast scanning. Considering the system's sampling speed (1000 S/s), the minimum movement distance (1 μm), and the diameter of the focused spot under a 50× objective lens (approximately 6 μm), we recommend a scanning speed of no more than 5000 μm/s.

4.2. Eliminate the Influence of the Seebeck Effect

When laser heating is applied, the temperature change affects the resistivity of the semiconductor material, and a temperature gradient is generated at the junction of some materials. Changing resistance can produce a current signal, called the OBIRCH signal, and the temperature gradient also can produce a voltage signal, called the Seebeck signal. The variation of current under laser stimulation is influenced by OBIRCH and Seebeck signals. OBIRCH and SEI signals have negative effects on each other [18]. When the bias voltage is low, the SEI signal dominates; when the bias voltage is high, the OBIRCH signal dominates. When a constant voltage bias V_0 is applied, the current I_{TLS} measured under laser heating is composed of the current variation ΔI_{SEI} due to Seebeck signal, the current variation ΔI_W due to OBIRCH signal, and the device current V_0/R under normal operation. For metal wiring, the current variation ΔI_W is:

$$\Delta I_W = I_{TLS} - \Delta I_{SEI} - \frac{V_0}{R} \tag{22}$$

When a constant current bias I_0 is applied, the voltage variation ΔV_W due to the OBIRCH signal is:

$$\Delta V_W = V_{TLS} - \Delta V_S - I_0 R \tag{23}$$

where V_{TLS} is the voltage value measured during laser heating; ΔV_S is the Seebeck voltage; and $I_0 R$ is the voltage change caused by the current bias.

For MOSFETs, if the generated Seebeck voltage ΔV_S inside due to laser heating is taken into account, the current at this time is:

$$I_{TLS} = \frac{\mu C_{OX} W}{2L} (v_{GS} + \Delta V_S - V_T)^2 \tag{24}$$

Similar to Equation (22), the change in MOSFET current ΔI_{MosFET} caused solely by temperature variations is:

$$\Delta I_{MosFET} = I_{TLS} - \frac{\mu C_{OX} W}{L} (v_{GS} - V_T) \Delta V_S \tag{25}$$

For components using materials with a high Seebeck coefficient (greater than 200 μV/K), we can eliminate the influence of the Seebeck signal in three steps. First, measuring the current without a bias voltage. Second, measuring the current with normal bias voltage. Finally, the data of the second measurement is subtracted from the data of the first to obtain the data without the Seebeck signal.

In slow mode, the system first measures the Seebeck signal at zero bias during laser scanning at each point and then measures the TLS signal at a constant bias. After the measurement is completed, the system can calculate the resistance change signal of each point based on the coordinate information.

As a type of laser thermal effect, the Seebeck effect is a phenomenon commonly found within materials. Therefore, in this section, we analyze how to measure the current/voltage data affected by the Seebeck voltage [28]. However, for common materials in semiconductor devices, the Seebeck coefficient is relatively low. For example, the Seebeck coefficient of Al is −3.5 μV/K, and Cu is 6.5 μV/K. The Seebeck voltage is in the microvolt range, which can be ignored compared to the voltage change caused by resistance (greater than or equal to millivolts level). In the preliminary experimental analysis, the effect of the Seebeck voltage can be ignored for normal silicon process devices.

4.3. The Method of Extracting Defective Point

For generic devices, the value of electrical parameters caused by resistive defects is usually large. Due to the complex structure of the circuit, it is complicated to calculate the changes in electrical parameters caused by laser heating through theoretical equations. During laser scanning, the electrical parameters change of good samples caused by temperature are within a specific range, but the changes of failure samples can exceed the specified range when the laser stimulates the defective area. Therefore, we set the specific range as the threshold to determine the defective spot.

For electrical signals with apparent changes in pulse amplitude, it can be judged directly by comparing the average of the amplitude generally. However, some special non-defective areas can also cause abnormal changes in the electrical parameters when it is necessary to combine the actual situation to locate the analysis.

Under the test conditions with good samples for comparison, we can test the good sample first and then the failure sample under the same experimental conditions.

The system software uses the average value of electrical parameter changes multiplied by coefficient data as the threshold to calculate two sets of data representing signal anomalies and compare these two sets of data to obtain defect points. The software can also use the coordinate information from two sets of data to generate a distribution map of defective points on the infrared image of the DUT. By comparing the distribution maps between the good and failure samples, we can easily determine the location of the defect points.

Under the test conditions without good samples for comparison, we should first collect the scan data when the laser scans the area without large current changes when laser radiation, then calculate the average values of some normal area by way of sliding windows, and then take the maximum value and calculate the percentage change of the maximum value in the mean value of the window as the judgment threshold of failure samples. Set the standard area data as $(\alpha_1, \alpha_2, \alpha_3, \ldots, \alpha_n)$, the value of window length as m (m is an odd number), and set the mean values of m as $(\mu_1, \mu_2, \mu_3, \ldots, \mu_{n-m})$. Among them:

$$\mu_i = \sum_{i-\frac{m-1}{2}}^{i+\frac{m-1}{2}} \alpha_k / m \quad \left(i > \frac{m-1}{2}, k \epsilon (i - \frac{m-1}{2}, i + \frac{m-1}{2})\right) \tag{26}$$

when $i \ll \frac{m-1}{2}$ or $i > \frac{n-(m-1)}{2}$, $\mu_i = \alpha_i$. The amplitude change ΔA_i is:

$$\Delta A_i = |u_i - \alpha_i| \tag{27}$$

The maximum amplitude ΔA_{max} is:

$$\Delta A_{max} = MAX\{|\Delta A_1 - \Delta A_2|, |\Delta A_2 - \Delta A_3|, \ldots, |\Delta A_{n-1} - \Delta A_n|\} \tag{28}$$

If we obtain ΔA_{max} when the sequence number is i, the threshold value of the electrical signal amplitude variation $A_{threshold}$ is:

$$A_{threshold} = \Delta A_{max} / A_i \tag{29}$$

Considering the complexity of the internal structure of the chip and the uncertainty of the induction signal level of thermal laser scanning, some normal areas may also cause

changes in electrical parameters during fast scanning, so if the threshold calculated by the above method is less than 10%, typically the threshold is also set to 10% [17].

For signals with insignificant amplitude changes, the system uses the sliding window's algorithm to judge abnormal data by the average and variance values in every window. The variance is suitable for detecting signal data's upper and lower edges, but a rectangular pulse will form two variance peaks, so we need to combine them. At the same time, there will be limitations on the oscillating signal when abnormal judgment data is just by average, but the signal can be well identified by the variance. Similar to the condition with noticeable amplitude change, the average and variance values will be obtained by applying statistical methods to data within a sliding window. At this time, the pulse signal detection intensity needs three thresholds; the upper threshold μ_{up}, lower threshold μ_{down}, and variance threshold $\sigma^2_{threshold}$ of the average value. Considering the symmetry of the vibration signal when the amplitude is not apparent, the upper and lower thresholds are set the same. The specific value set principle is the same as the method described above, and the maximum value of the average value variation of adjacent windows $\Delta\mu_{max}$ is:

$$\Delta\mu_{max} = MAX\{|\mu_1 - \mu_2|, |\mu_2 - \mu_3|, \ldots, |\mu_{n-1} - \mu_n|\} \quad (30)$$

the variance of adjacent windows $\Delta\sigma^2_{max}$ is:

$$\Delta\sigma^2_{max} = MAX\{|\sigma_1^2 - \sigma_2^2|, |\sigma_2^2 - \sigma_3^2|, \ldots, |\sigma_n^2 - \sigma_{n-1}^2|\} \quad (31)$$

After the data acquisition unit obtains the above data, the failure point will be identified after the data acquisition is completed because of the massive data. In addition to the input and reference threshold calculated by the system, there is a variable threshold value designed for the application with more pulsed anomalous data. This value is smaller than the input threshold. Adjusting this value to filter the hot spots displayed on the IR image allows a visual comparison of hot spots of good samples and hot spots of anomalous samples.

5. Experiment

5.1. DUT

The DUT was an STT-MRAM device with a standard operating voltage of 3.3 V and an operating current of 2.1 mA. It was damaged accidentally during a pulsed laser evaluation of single event effects with an energy of 1.5 nJ. Figure 5 shows the I-V curves between VDD and GND separately for the usual chip and the failed sample. The current change of the sound sample can be divided into three stages: The first stage is when the constant voltage V_0 is less than 1.5 V, the internal circuit is shut down, and with the voltage increase, the current slowly increases.

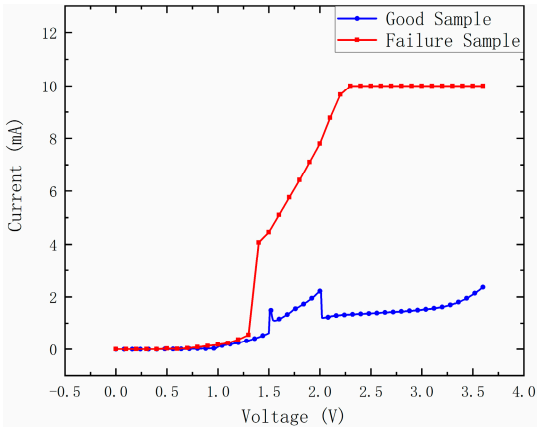


Figure 5. I-V curves.

When $1\text{ V} < V_0 < 1.5\,V$, the current growth rate with voltage change is 1.05 mA/V. There is a steep increase in current when $V_0 > 1.5$ V, and a sudden drop in current to 1.6 V, with an overall current increase of 0.4 mA. The second stage is 1.6–2 V, and the current growth rate is 2.13 mA/V. The third stage is V_0 greater than 2.0 V. The second to third stage current has a 0.8 mA sudden drop process. The current change can be seen in the three different stages of the device's internal response circuit, and different stages have similar current growth rates with voltage changes. The bad sample has two current curve abnormal stages. It will produce a larger current abnormality when it is working. The current growth rate is in a normal range of 1.26 mA/V in the first stage, so we set the cross-voltage value within 1.3–2 V and then test the laser scanning static defect points of the good and bad samples working in the first and second stages separately.

5.2. Defect Location

The active area is 2150 μm × 1940 μm, and the substrate thickness is 94 μm. Before scanning, we need to adjust the three-axis precision panning table on the mobile table to ensure that the chip is at the same level, so that the laser irradiation to each area has the same energy. Then, set the origin, x-axis, y-axis, scanning direction, and the parameters such as scanning speed, longitudinal scanning interval, DC output, and laser energy. Next, a coordinate system is established on the sample surface, as shown in Figure 6, setting the upper left corner direction of the chip as the origin, the horizontal direction as the x-axis, and the vertical direction as the y-axis. First, we set the device to be in the first voltage stage, and setting the scanning bias voltage to 1.35 V, laser energy at 0.5 mW, scanning speed at 2000 μm/s, longitudinal interval at 10 μm and the variation of current value I with scanning time t as shown in Figure 7a. Then, the device was set to be in the second voltage stage, with a voltage value of 1.7 V; other parameters were kept constant, the results are shown in Figure 7c. A good sample was used for the comparison test. Figure 7b shows the current variation under 1.35 V supply for the good sample, and Figure 7d shows the current variation under 1.7 V supply for the good sample. During the test data processing, the 5× IR scan image of the sample was imported into the scan test software (the generated anomaly distribution is shown in Figure 8), and the subplots in Figure 8 correspond to the data in Figure 7 one by one. It is obvious from the graph that there are the same anomalous points and different anomalous points for different voltage scans. After comparing the measured data of good and failure samples, we can know that the abnormal part of the chip may be the digital module (red box on the left in Figure 8a) and the eFuse module (red box on the right in Figure 8a) of the chip.

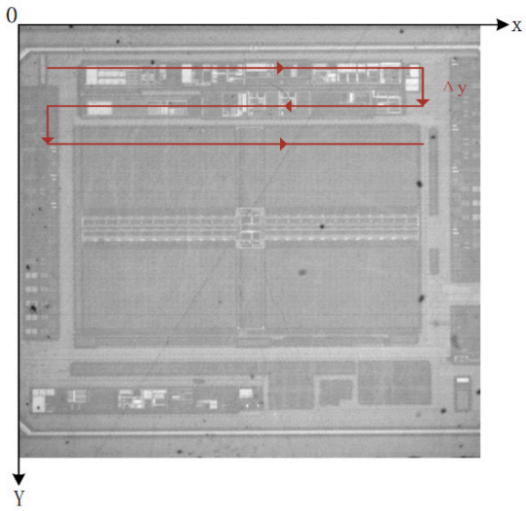


Figure 6. Scanning Solutions.

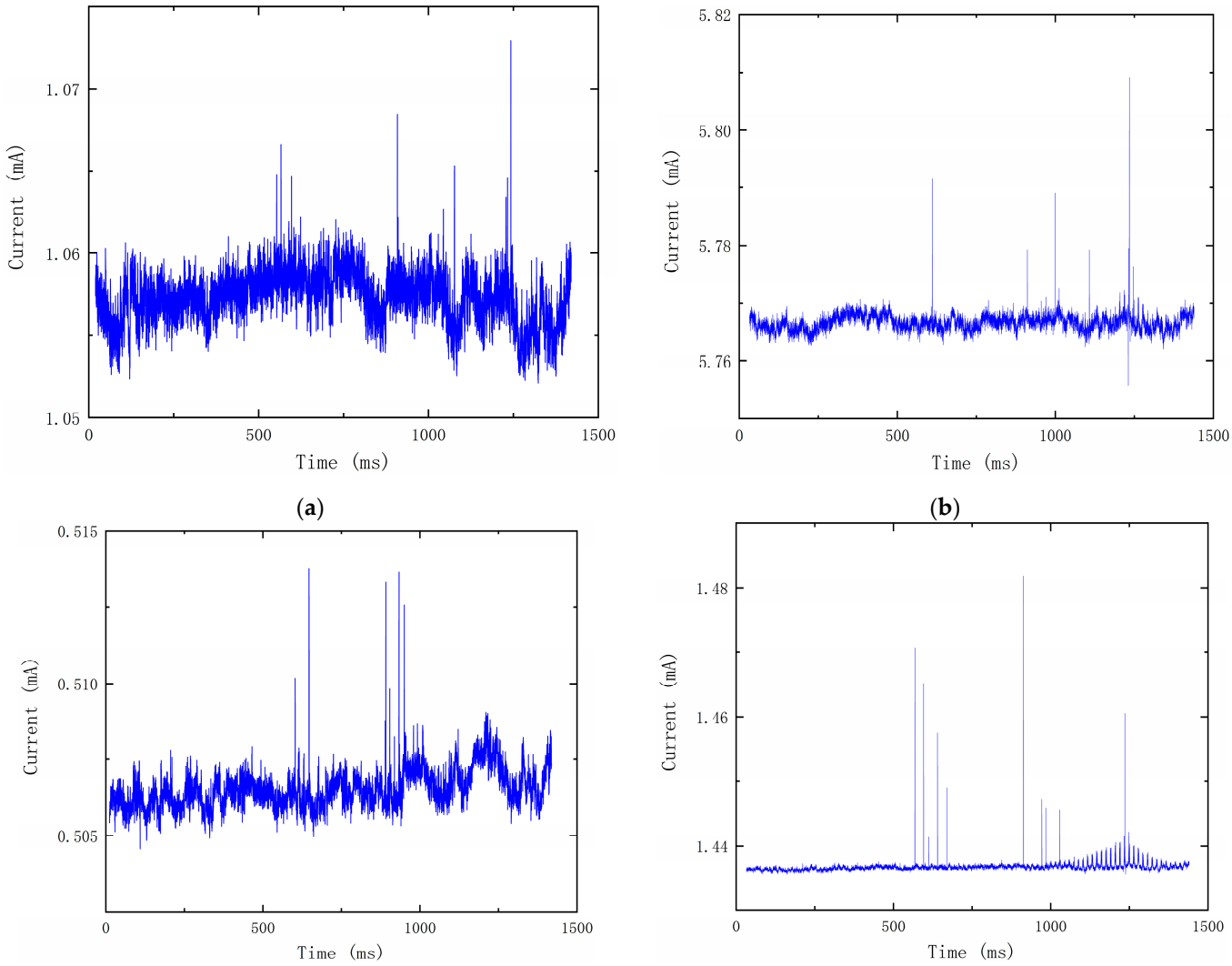
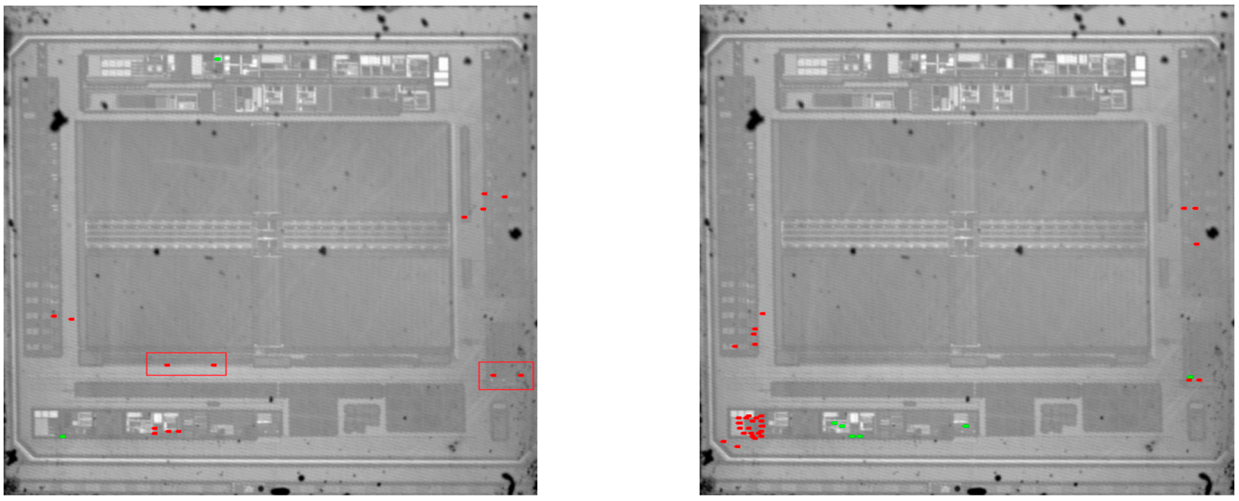
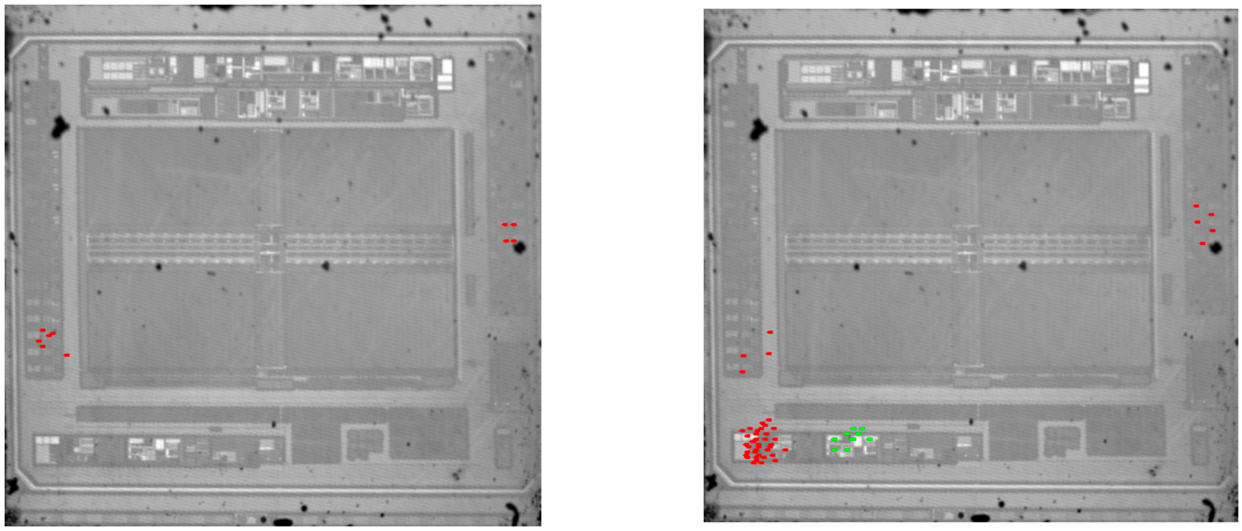


Figure 7. Scan data comparison of good and bad samples. Scan data of failure sample at (**a**) 1.3 V/(**c**) 1.7 V bias voltage. Scan data of normal sample at (**b**) 1.3 V/(**d**) 1.7 V bias voltage.

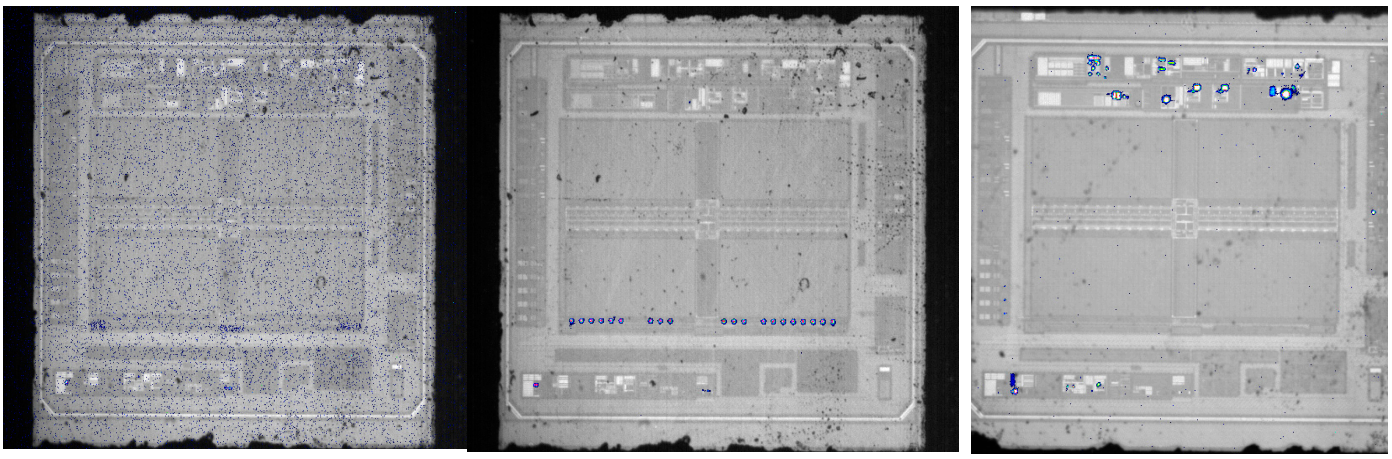




(**c**) (**d**)

Figure 8. Distribution of abnormal scan data in chip infrared image. Hot point (red point indicate data increase exceptions, green indicates decrease exceptions) distribution of failure sample at (**a**) 1.3 V(the red box on the left digital module and the right is eFuse module) and (**b**) 1.7 V bias voltage. Hot point distribution of normal sample at (**c**) 1.3 V and (**d**) 1.7 V bias voltage.

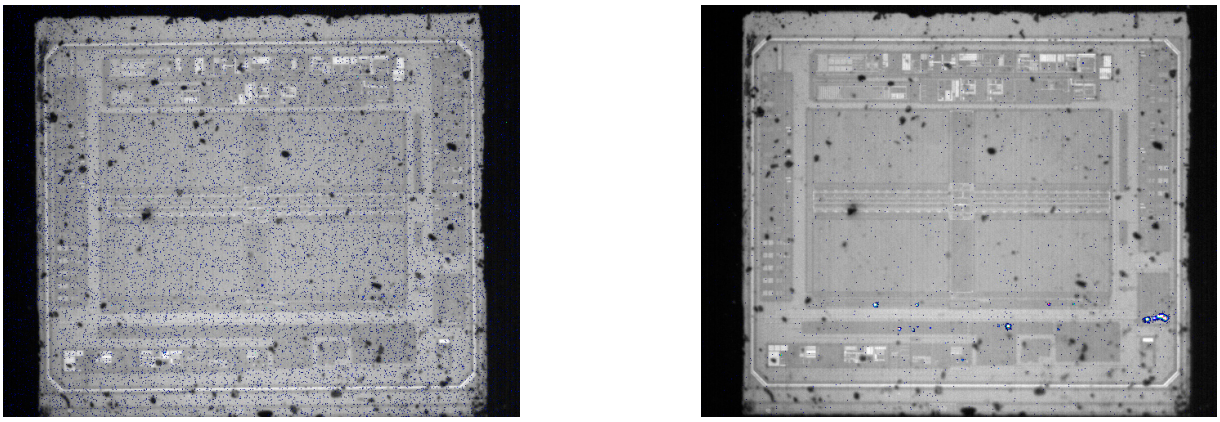
After testing with the location system, we also tested the good and failure samples using the PHEMOS-1000 system [29], setting the system using a 5× objective with a 15 s exposure time. Figure 9 shows the hot spot distribution obtained by the InGaAs camera for a good sample. From left to right are the hot spot maps shown for 1.4 V, 1.7 V, and 3.0 V voltage bias, respectively. The hot spots are the regions of strong photon emission inside the device.



(**a**) (**b**) (**c**)

Figure 9. EMMI plot of a good sample at (**a**) 1.3 V; (**b**) 1.7 V; and (**c**) 3.0 V voltage bias under a 5× objective.

Figure 10 shows the images for a failure sample under 1.4 V and 1.7 V bias voltages. Comparing the bright spot distribution maps of the good and failure samples, we can know that the digital module and the eFuse module also be shown as a normal area of the chip. It can be verified that the defect localization system we proposed has good static defect localization ability.



(**a**) (**b**)

Figure 10. EMMI plot of a failure sample at (**a**)1.3 V; and (**b**) 1.7 V voltage bias under a 5× objective.

The IV curve shows the changes in the internal functional unit state of the device with the voltage, and the distribution of abnormal points in the defect system and EMMI equipment also confirms this conclusion. During the experiment, it was found that the distribution of bright spots under different bias voltages was different. This indicates that the circuit at the failure area needs to be activated at a specific voltage (because different circuit modules work at different voltages). Therefore, it is necessary to preliminarily confirm the fault mode by electrical experiments before locating defects.

For complex integrated circuits, we usually receive abnormal points more than once. In this case, we need to analyze the points that are more likely to cause device failure through the circuit schematic and experiment data. We can then use other experimental devices to find the physical location. The MRAM sample used in the experiment was damaged during the radiation-resistant experiment. According to the I-V curve of the circuit, the entire failed chip's electrical characteristics show resistance properties (current increases proportionally with voltage). Therefore, it can be preliminarily considered that the probability of failure caused by eFuse module burnout is high.

6. Conclusions

This paper introduces the composition of the integrated circuit hard defect scanning and positioning system, including the hardware composition and some software algorithms. The article presents a detailed derivation of the equations for the temperature change of different devices during laser irradiation and the equations for the change of electrical parameters caused by the temperature change. It also introduces some methods to improve the efficiency and accuracy of the system positioning. The ability of the system to locate abnormal devices is verified by the experiment of an STT-MRAM. To better display the localization effect, we have corresponded the coordinates of the scanning data to the infrared image of the device in the form of equal scale scaling. The system chose a Si-CCD camera as the image acquisition unit, which could not directly obtain the image of the chip interior. We need to input the infrared image of the chip into the software system, which also introduces errors in the system. In the future, we will upgrade the optical path to allow the infrared camera to replace the existing cameras so that the infrared camera can detect the state of the laser scan in a safe environment. We will upgrade the optical path to allow the infrared camera to replace the existing cameras so that the system can acquire the infrared image directly and monitor the status of the laser in real-time.

Author Contributions: Conceptualization, W.W., M.C., J.H. and Y.M.; methodology, W.W., Y.M.; software, W.W.; validation, W.W., M.C., J.H. and Y.M.; formal analysis, W.W.; investigation, W.W.; resources, J.H. and Y.M.; writing—original draft preparation, W.W.; writing—review and editing,

J.H. and Y.M.; visualization, W.W.; supervision, Y.M.; project administration, M.C. and Y.M.; funding acquisition, Y.M. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by a Grant from the Foundation for Study Encouragement to Youth Innovation Promotion Association Member of Chinese Academy of Sciences, Chinese Academy of Sciences, China (Grant No. Y2022057).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest: The authors declare no conflict of interest.

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