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Non-Isolated High-Voltage-Gain Step-Up DC–DC SISC Converter for Renewable Energy Applications

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Abstract

This paper presents two new step-up DC–DC converters that have high voltage gains and low voltage stresses across their main switches with respect to their output voltages. These high voltage gains are achieved with the help of voltage multiplier cells (VMCs). By inserting VMCs that are switched inductors (SIs) and switched capacitors (SCs), the voltage gains increased substantially compared to the conventional converters, such as the traditional boost converter (TBC), Luo converter, or Zeta converter. Furthermore, the TBC has a voltage stress across its main switch that equals the output voltage, while the two proposed step-up converters have voltage stresses across their main switches that are lower than their output voltages. An extended converter is obtained from the main topology, which has a higher voltage gain than the main one. This paper investigates both topologies in continuous conduction mode (CCM) operation and shows a detailed analysis deriving the voltage gain and the voltage stress between the switches. In the main topology, when the duty ratio (D) is 0.75, the output voltage equals around thirty times the input voltage. In the extended topology, when D is 0.75, the output voltage equals around sixty times the input voltage. The voltage stresses across the main switches in both topologies are half of their output voltages when D is 0.75. Simulation models using Matlab/Simulink are carried out for both the main and extended topologies, showing how these agree with the theoretical derivations.

Keywords: DC–DC converter; high voltage gain; switched inductor; switched capacitor; renewable energy

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1. Introduction

Today, DC microgrids integrate primarily renewable energy resources, such as photovoltaics (PVs) and fuel cells, which are receiving increasing attention. This attention is due to the fact that the use of renewable energy resources is more environmentally friendly compared to fossil fuels [1,2]. However, the output voltage of renewable energy resources is typically low, necessitating an increase before they can be connected to the load [3,4]. Consequently, a high-voltage-gain step-up DC–DC converter is essential. Figure 1 shows a standard diagram of a two-stage renewable energy system. The system consists of a renewable energy source, PVs, located on the source side. It includes a high-voltage-gain step-up DC–DC converter, which is the main focus of this paper, as well as a DC load or a grid-connected inverter on the load side to supply AC loads [5].

High-voltage-gain DC–DC converters consist of two groups: isolated converters, such as bridge converters and push–pull converters, and non-isolated converters, such as traditional boost converters (TBCs) and Zeta converters. The use of isolated converters is

discouraged due to their large mass and volume, and their efficiency is low because they use a transformer in their design. The use of a transformer often results in producing a high voltage spike between the switches, although they can attain a high voltage gain by adjusting the turn ratio of the coils without utilizing a high percentage of duty cycles [6,7]. However, the use of non-isolated converters is encouraged because of their simplicity, better efficiency, and wide voltage gain without utilizing any transformers.

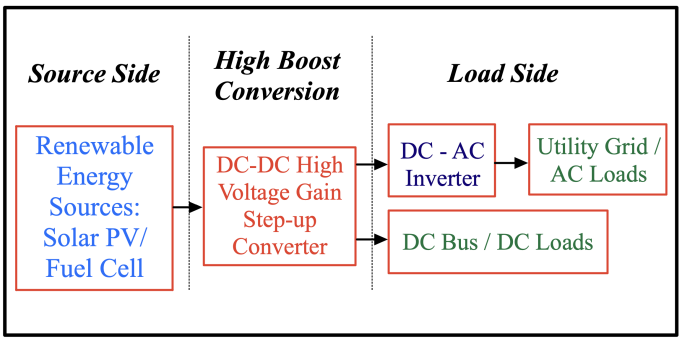
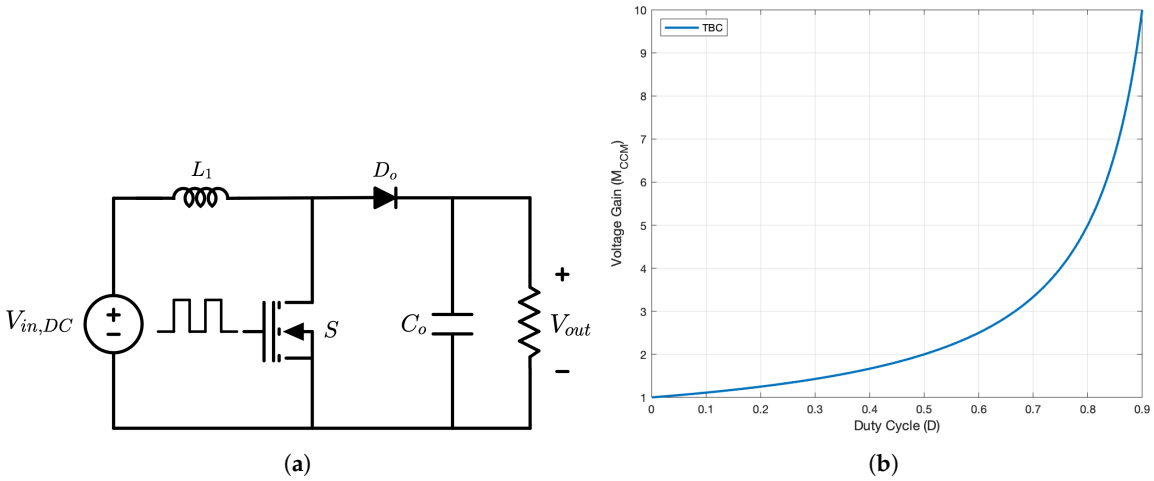


Figure 1. Block diagram of a renewable energy system utilizing a high-voltage-gain DC–DC converter.

The TBC, which is shown in Figure 2, is the simplest and most fundamental topology of a non-isolated step-up DC–DC converter. That is because it has different advantages: the use of a single switch, the continuity of the source current, and the sharing of a common ground between the source and the load. However, in addition to these advantages, two main disadvantages make using TBCs undesirable: the low voltage gain with duty cycles lower than one and the high voltage stress between the main switch with respect to the output voltage. Operating TBCs or any other converter at a high duty cycle leads to an increase in current stress, resulting in increased conduction and switching losses and reduced efficiency [7]. Different techniques have been employed to overcome these issues in TBCs. One of these techniques is to insert a multistage switched inductor (SI) instead of the single inductor into the TBC to boost the voltage gain [8]. However, this multistage SI contains a large number of diodes and inductors, which will increase the number of elements in the circuit and, therefore, make it complex and inefficient. Another technique is to insert SI cells and switched capacitor (SC) cells into the TBC in a topology called a switched-inductor multilevel boost converter [9] to increase the voltage gain. However, the problem of requiring a large number of components reemerges, resulting in a larger complexity and inefficiency in the converter. Furthermore, in both techniques, the output voltage is low and fails to reach the desired high levels.

Different techniques are employed with non-isolated step-up DC–DC converters to increase their voltage gain, such as cascade [10,11], coupled inductor [12–14], quadratic [15,16], interleaved [17–19], or multilevel [20–22] converters. Cascaded converters can attain high voltage gain by merging various stages. However, they consist of a large number of circuit elements and have low efficiency. Similar to the isolated converters, coupled inductor converters can attain high voltage gains by selecting a specific value for the turn ratio. However, the overall efficiency of the converter is low due to leakage inductance, and the structure of the circuit design is complex due to the need for a snubber circuit to resolve the issue of leakage inductance. Moreover, quadratic converters can maintain high voltage gains; however, the circuit becomes complex due to the use of numerous elements, resulting in a reduction in efficiency. Although interleaved converters can attain high voltage gains, they utilize a large number of components, which is the main drawback of constructing such types of converters. Furthermore, multilevel converters also face the previously mentioned issue of having an increased number of components. The voltage gain of the multilevel converter that is presented in [23] depends on the number of voltage

multipliers (VMs), mainly Cockcroft–Walton voltage multipliers that consist of several diodes and capacitors. As the number of VMs in the multilevel converters increases, the voltage gain will consequently increase. Ref. [24] presents several step-up and step-down voltage multiplier cells that can be integrated into different types of non-isolated DC–DC converters. In the proposed converters, an SI, which consists of two inductors, one capacitor, and two diodes, and an SC, which consists of two capacitors and two diodes, are utilized to design step-up converters that have high voltage gain while keeping the number of elements used at its minimum.



(**a**) (**b**)

Figure 2. Traditional boost converter (TBC): (**a**) layout; (**b**) voltage gain vs. duty cycle.

This paper is organized as follows: Section 2 describes the proposed SISC converter, including its two modes of operation and a comprehensive investigation of the derivation of the voltage gain and voltage stress equations. Similarly, Section 3 describes the proposed extended version of the SISC (ESISC) converter, including its two modes of operation and a comprehensive investigation of the derivation of the voltage gain and voltage stress equations. In Section 4, a comparison is made between the two proposed topologies and different early published converters in terms of the voltage gain, the voltage stress between the main switch, the switching frequency, and the total number of components. In Section 5, the simulation results are presented and discussed to determine whether they match the theoretical predictions. Finally, this paper concludes with a summary that highlights the key accomplishments made.

2. SISC Converter

Figure 3 illustrates the proposed SISC converter, consisting of two VM cells: an SI and an SC. The SISC converter consists of two inductors (L_1 and L_2), four capacitors (C_1, C_2, C_3, and C_0), five diodes (D_1, D_2, D_3, D_4, and D_0), and a switch (S). As can be clearly seen from the structure of the circuit, the output voltage polarity is positive, guaranteeing compatibility with downstream elements.

To obtain the fundamental expressions of the proposed SISC and ESISC converters, the subsequent assumptions are posited:

- All the circuit elements are lossless.
- The inductors' values are adequately high to guarantee working in continuous conduction mode (CCM).
- The capacitors' values are adequately high to provide constant voltage without any ripples during converter operation.

- The two proposed topologies have two modes according to the operation of their semiconductor switches.

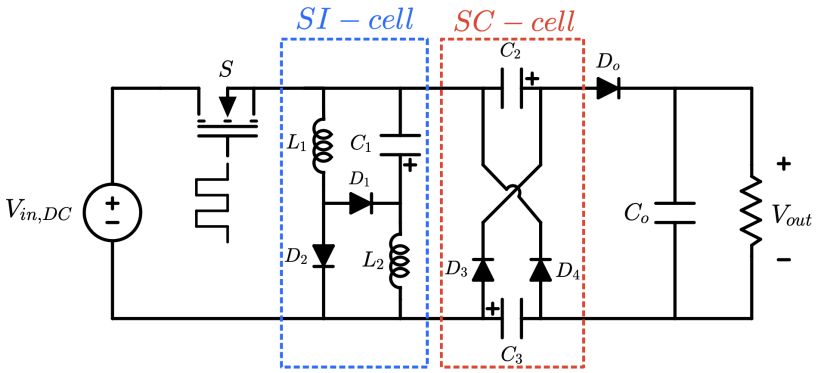


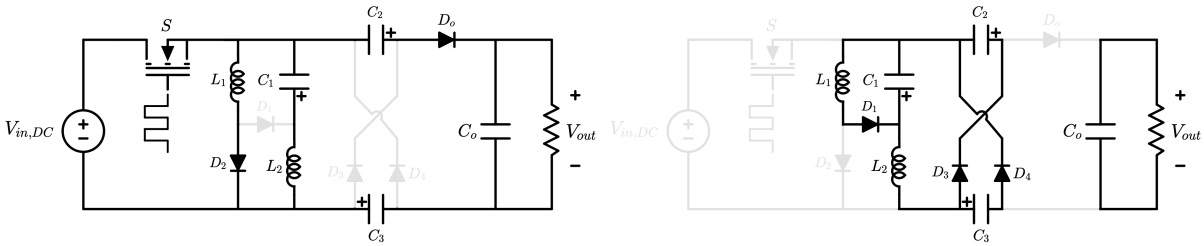
Figure 3. Main circuit of the SISC converter.

The equivalent circuit of the first mode of the proposed SISC converter is shown in Figure 4a. As shown in this figure, the switch (S) is ON and three diodes are reverse-biased, which are D_1, D_3, and D_4. However, two diodes are forward-biased, which are D_2 and D_0. During this mode, the first inductor (L_1) is magnetized and charged by the input voltage (V_{in}).

$$V_{L_1} = V_{in} \tag{1}$$

Similarly, the second inductor (L_2) is magnetized and charged by V_{in} with the discharged energy of the first capacitor (C_1).

$$V_{L_2} = V_{in} + V_{C_1} \tag{2}$$



(**a**) (**b**)

Figure 4. SISC converter: (**a**) Mode 1; (**b**) Mode 2.

The load is supplied by the discharged energy of the second and third capacitors (C_2 and C_3) with V_{in}.

On the other hand, the equivalent circuit of the second mode of the proposed SISC converter is shown in Figure 4b. As shown in this figure, S is OFF and three diodes are forward-biased, which are D_1, D_3, and D_4. However, two diodes are reverse-biased, which are D_2 and D_0. During this mode, L_1 and L_2 are demagnetized due to the negative voltage on them, and they charge C_1, C_2, and C_3. Hence, $C_2 = C_3$.

$$V_{L_1} = -V_{C_1} \tag{3}$$

$$V_{L_2} = V_{C_1} - V_{C_2} \tag{4}$$

At the same time, the load is powered by the discharged energy of the output capacitor (C_0). According to the voltage-second balance principle, the average voltage between L_1 and L_2 is zero; therefore, the following two equations are derived.

$$V_{in}D - V_{C_1}(1-D) = 0 \tag{5}$$

$$(V_{in} + V_{C_1})D + (V_{C_1} - V_{C_2})(1-D) = 0 \tag{6}$$

By solving Equation (5), the voltage between C_1 is obtained.

$$V_{C_1} = \frac{D}{1-D}V_{in} \tag{7}$$

By solving Equation (6) and considering Equation (7), the voltage between C_2, which is the same voltage between C_3 is obtained.

$$V_{C_2} = V_{C_3} = \frac{2D - D^2}{(1-D)^2}V_{in} \tag{8}$$

Consequently, the proposed SISC converter's voltage gain in CCM is obtained.

$$M_{CCM_{SISC}} = \frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{1 + 2D - D^2}{(1-D)^2} \tag{9}$$

Now, the derived voltages between the capacitors and inductors are utilized to find the voltage stresses between the switches. Voltage stress refers to the amount of voltage present between either the main switch or the diode when they are turned OFF. During the first mode, D_1, D_3, and D_4 are OFF; therefore, the voltage stresses between them are calculated.

$$V_{D_1} = \frac{V_{in}}{1-D} = \frac{(1-D)V_{out}}{1 + 2D - D^2} \tag{10}$$

$$V_{D_3} = V_{D_4} = \frac{V_{in}}{(1-D)^2} = \frac{V_{out}}{1 + 2D - D^2} \tag{11}$$

Similarly, during the second mode, D_2, D_0, and S are OFF; therefore, the voltage stresses between them are calculated.

$$V_{D_2} = \frac{DV_{in}}{(1-D)^2} = \frac{DV_{out}}{1 + 2D - D^2} \tag{12}$$

$$V_{D_0} = V_S = \frac{V_{in}}{(1-D)^2} = \frac{V_{out}}{1 + 2D - D^2} \tag{13}$$

The designs of the inductors' values used in this converter with the help of V_{in}, V_{out}, D, f_S, and Δi_L, which is the inductor ripple, are computed using the following expressions:

$$L_1 = \frac{DV_{in}}{\Delta i_{L_1} f_S} = \frac{D(1-D)^2 V_{out}}{(1 + 2D - D^2)\Delta i_{L_1} f_S} \tag{14}$$

$$L_2 = \frac{DV_{in}}{(1-D)\Delta i_{L_2} f_S} = \frac{D(1-D)^2 V_{out}}{(1-D)(1 + 2D - D^2)\Delta i_{L_2} f_S} \tag{15}$$

3. Extended Topology of SISC Converter

Figure 5 clarifies the proposed extended SISC (ESISC) converter, which is composed of three inductors, three capacitors, eight diodes, and a switch. Similar to the proposed SISC converter, the extended one has a positive polarity at the output. The ESISC converter

is obtained by replacing L_2 in the SISC converter with another SI, which involves two inductors (L_2 and L_3) and three diodes (D_5, D_6, D_7). Therefore, the ESISC converter has in total three inductors, four capacitors, eight diodes, and a single switch.

The equivalent circuit of the first mode of the proposed ESISC converter is shown in Figure 6a. As shown in this figure, S is ON and four diodes are reverse-biased, which are D_1, D_3, D_4, and D_6. However, four diodes are forward-biased, which are D_2, D_5, D_7, and D_0. During this mode, L_1 is magnetized and charged by V_{in}.

$$V_{L_1} = V_{in} \tag{16}$$

Similarly, L_2 and L_3, which is the third inductor, are magnetized and charged by V_{in} with the discharged energy of C_1. Hence, $L_2 = L_3$.

$$V_{L_2} = V_{L_3} = V_{in} + V_{C_1} \tag{17}$$

The load is supplied by the discharged energy of C_2 and C_3 with V_{in}.

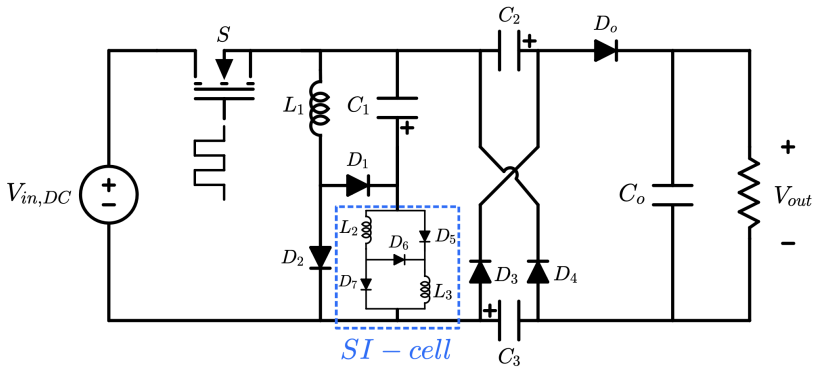
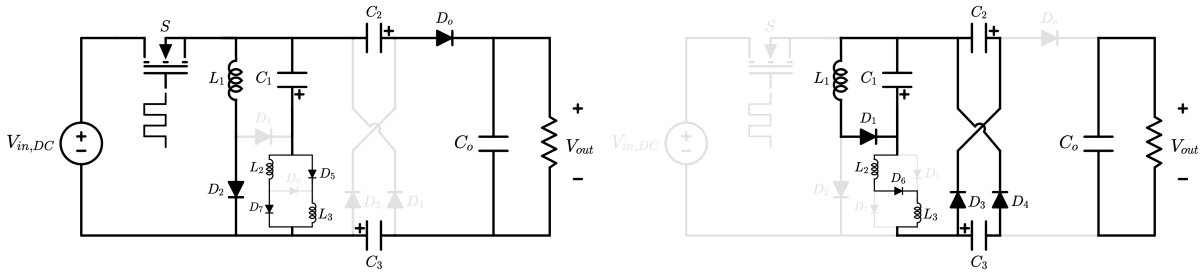


Figure 5. Basic circuit of the ESISC converter.



(**a**) (**b**)

Figure 6. ESISC converter: (**a**) Mode 1; (**b**) Mode 2.

On the other hand, the equivalent circuit of the second mode of the proposed ESISC converter is shown in Figure 6b. As shown in this figure, S is OFF and four diodes are forward-biased, which are D_1, D_3, D_4, and D_6. However, four diodes are reverse-biased, which are D_2, D_5, D_7, and D_0. During this mode, L_1, L_2, and L_3 are demagnetized due to the negative voltage on them, and they charge C_1, C_2, and C_3. Hence, $C_2 = C_3$.

$$V_{L_1} = -V_{C_1} \tag{18}$$

$$V_{L_2} = V_{L_3} = \frac{V_{C_1} - V_{C_2}}{2} \tag{19}$$

At the same time, the load is powered by the discharged energy of the output capacitor (C_0). According to the voltage-second balance principle, the average voltage between L_1, L_2, and L_3 is zero; therefore, the following two equations are derived.

$$V_{in}D - V_{C_1}(1-D) = 0 \tag{20}$$

$$(V_{in} + V_{C_1})D + (\frac{V_{C_1} - V_{C_2}}{2})(1-D) = 0 \tag{21}$$

By solving Equation (20), the voltage between C_1 is obtained.

$$V_{C_1} = \frac{D}{1-D}V_{in} \tag{22}$$

By solving Equation (21) and considering Equation (22), the voltage between C_2, which is the same voltage between C_3 is obtained.

$$V_{C_2} = V_{C_3} = \frac{3D - D^2}{(1-D)^2}V_{in} \tag{23}$$

Consequently, the proposed ESISC converter's voltage gain in CCM is obtained. Although only five elements are added to the extended one, the voltage gain of the extended converter is approximately twice that of the SISC converter when $D = 75\%$, as can be seen in Equation (24).

$$M_{CCM_{ESISC}} = \frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{1 + 4D - D^2}{(1-D)^2} \tag{24}$$

Now, the derived voltages between the capacitors and inductors are utilized to find the voltage stresses between the switches. During the first mode, D_1, D_3, D_4, and D_6 are OFF; therefore, the voltage stresses between them are calculated.

$$V_{D_1} = V_{D_6} = \frac{V_{in}}{1-D} = \frac{(1-D)V_{out}}{1 + 4D - D^2} \tag{25}$$

$$V_{D_3} = V_{D_4} = \frac{(1+D)V_{in}}{(1-D)^2} = \frac{(1+D)V_{out}}{1 + 4D - D^2} \tag{26}$$

Similarly, during the second mode, D_2, D_5, D_7, D_0, and S are OFF; therefore, the voltage stresses between them are calculated.

$$V_{D_2} = \frac{2DV_{in}}{(1-D)^2} = \frac{2DV_{out}}{1 + 4D - D^2} \tag{27}$$

$$V_{D_5} = V_{D_7} = \frac{DV_{in}}{(1-D)^2} = \frac{DV_{out}}{1 + 4D - D^2} \tag{28}$$

$$V_{D_0} = V_S = \frac{(1+D)V_{in}}{(1-D)^2} = \frac{(1+D)V_{out}}{1 + 4D - D^2} \tag{29}$$

The designs of the inductors' values used in this converter with the help of V_{in}, V_{out}, D, f_S, and Δi_L, which is the inductor ripple, are computed using the following expressions:

$$L_1 = \frac{DV_{in}}{\Delta i_{L_1} f_S} = \frac{D(1-D)^2 V_{out}}{(1 + 4D - D^2)\Delta i_{L_1} f_S} \tag{30}$$

$$L_2 = \frac{DV_{in}}{(1-D)\Delta i_{L_2} f_S} = \frac{D(1-D)^2 V_{out}}{(1-D)(1 + 4D - D^2)\Delta i_{L_2} f_S} \tag{31}$$

4. Comparison Analysis

Table 1 summarizes a detailed comparison analysis of the proposed converters, SISC and ESISC, with the newly published non-isolated step-up DC–DC converters [25–30]. This comparison focuses on various criteria: the voltage gain in CCM, the voltage stress on the main switch, the switching frequency, the efficiency, the common ground availability, and the number of components. There are several factors to take into account when comparing step-up converters. The first factor is the voltage gain, which is considered the main aspect. Figure 7 shows a voltage gain comparison between the two proposed converters and other step-up converters as a function of the duty cycle. As this figure shows, the proposed converters have a higher voltage gain than all other suggested step-up converter topologies. The second factor is the voltage stress on the main switch S, (V_S/V_{out}). When the duty cycle is higher than 50%, the (V_S/V_{out}) will be around 50% of the output voltage. However, when the duty cycle is less than 50%, (V_S/V_{out}) is more than 50% of the output voltage but never exceeds one. In contrast, the other boost topologies are being compared with experienced voltage stresses on their main switch that are equal to or greater than the output voltages of those topologies. The step-up converter in [26] has a higher voltage gain than the SISC converter, but it also experiences voltage stress on the main switch that is equal to its output voltage. Unfortunately, the efficiency of the proposed converters is not high enough but is acceptable compared to other converters.

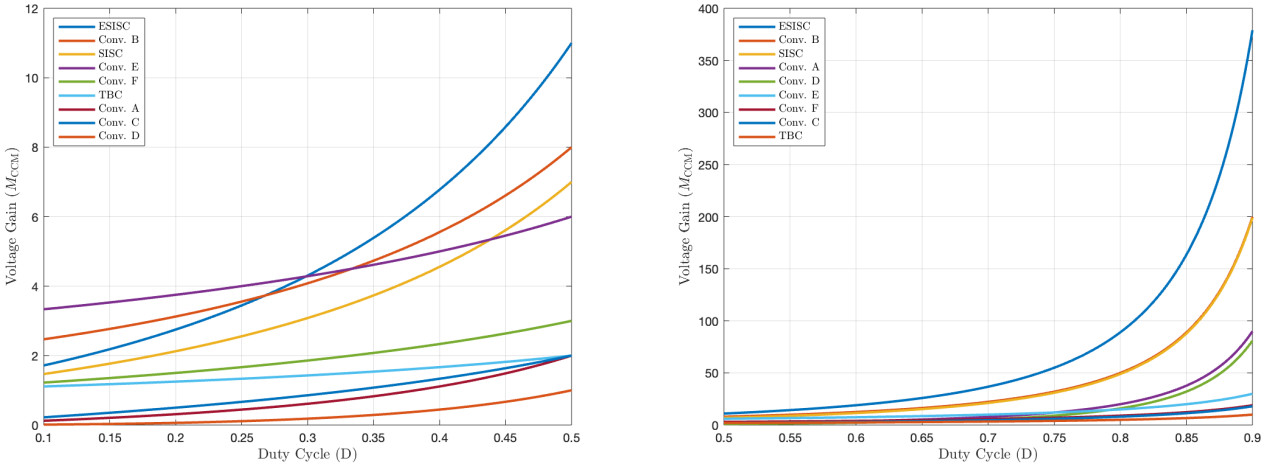
Table 1. Comparison of the proposed converters with related boost converters in term of voltage gain, voltage stress on the main switch, switching frequency, and number of components.

T	M_{CCM}	M_{CCM} at $D = 75\%$	$\frac{V_S}{V_{out}}$	V_S at $D = 75\%$	f_S	η	CG	S/D/L/C/T
TBC	$\frac{1}{1-D}$	4	1	V_{out}	-	-	✓	1/1/1/1/4
[25]	$\frac{D}{(1-D)^2}$	12	1	V_{out}	50 kHz	91.4%	✓	1/3/3/3/10
[26]	$\frac{2}{(1-D)^2}$	32	1	V_{out}	100 kHz	90%	✓	1/5/3/3/12
[27]	$\frac{2D}{1-D}$	6	1	V_{out}	10 kHz	96%	✓	1/6/2/4/13
[28]	$\frac{D^2}{(1-D)^2}$	9	$\frac{1}{D^2}$	$2V_{out}$	40 kHz	85%	✓	1/5/3/3/12
[29]	$\frac{3}{1-D}$	12	1	V_{out}	50 kHz	95.1%	✓	1/8/3/3/15
[30]	$\frac{1+D}{1-D}$	7	$\frac{1}{1-D}$	$4V_{out}$	100 kHz	97.4%	✓	1/8/3/3/15
SISC	$\frac{1+2D-D^2}{(1-D)^2}$	31	$\frac{1}{1+2D-D^2}$	$\frac{V_{out}}{2}$	50 kHz	84.2%	✓	1/5/2/4/12
ESISC	$\frac{1+4D-D^2}{(1-D)^2}$	55	$\frac{(1+D)}{1+4D-D^2}$	$\frac{V_{out}}{2}$	50 kHz	77.4%	✓	1/8/3/4/16

Note: M_{CCM} = voltage gain in CCM, $\frac{V_S}{V_{out}}$ = normalized voltage stress on main switch, V_S = voltage stress on main switch, f_S = switching frequency, η = efficiency, CG = common ground, ✓ = has common ground, S = no. of switches, D = no. of diodes, L = no. of inductors, C = no. of capacitors, T = total no. of components.

From a component count and cost viewpoint, the proposed SISC and ESISC converters, as well as the compared converters, utilize a single active switch and avoid the use of transformers or coupled inductors. Therefore, the number of passive components and the voltage stress on the main active switch primarily influence the overall cost. Although the ESISC topology requires a larger number of passive electric elements to achieve a substantial high voltage gain, the voltage stress on the main switch is reduced to half of the output voltage, allowing the use of a lower-rated and lower-cost active switch. The proposed SISC converter, with a component count equal to [26,28], offers a reasonable cost tradeoff while attaining a higher voltage gain. The proposed converters, along with the topologies described in [25,30], are primarily designed for renewable energy applications,

especially PVs, where a high step-up voltage gain is required. The converter presented in [26] is designed for high step-up DC systems requiring high voltage gain through quadratic and voltage multiplier techniques. The converter presented in [27] is designed for high-power, high-efficiency, and complex control applications, such as electric vehicle charging systems. The converter presented in [28] is designed for applications demanding a wide input voltage range with continuous input and output currents. Finally, Ref. [29] proposes a converter for DC microgrid applications, where high step-up capability and efficient power conversion are required. Additional information on these converters can be found in their relevant references.



(**a**) (**b**)

Figure 7. Voltage gain comparison as a function of duty cycle: (**a**) between 0% and 50% duty cycle; (**b**) between 50% and 90% duty cycle. Conv. A, Conv. B, and Conv. C, Conv. D, Conv. E, and Conv. F correspond to the converters presented in [25], [26], [27], [28], [29], and [30] respectively.

5. Simulation Results

The two proposed converters (SISC and ESISC) are designed and analyzed using Matlab/Simulink software, which is a well-suited and trusted simulator. Before starting to analyze the two converters, different values have to be set up, such as input voltage, output voltage, output power, switching frequency, duty cycle, capacitor values, and inductor values. All of these necessary values are provided in Table 2.

Table 2. Parameters of the Matlab/Simulink simulator.

Parameter	Value
Input voltage (V_{in})	12 V
Output voltages (V_{out})	345 V/605 V
Rated power (P_{out})	400 W
Switching frequency (f_s)	50 kHz
Duty cycle (D)	75%
Inductor (L_1)	1 mH
Inductors (L_2 and L_3)	5 mH
Capacitor (C_1)	200 µF
Capacitors (C_2 and C_3)	150 µF
Capacitor (C_0)	100 µF

5.1. SISC Converter

A 400 W, 345 V model is simulated and tested to validate the performance of the proposed SISC converter under steady-state operation conditions. The main purpose is

to justify the exact functionality of the proposed converter in terms of the voltage gain and the voltage stress between active and passive switches. The input voltage of 12 V is increased to an output voltage of 345 V with a duty cycle of 0.75 and an output power of 400 W, as shown in Figure 8. The voltage waveforms between the capacitors C_1, C_2, and C_3 are shown in Figure 9. Equations (7) and (8) predict the voltages of C_1 and C_2, which is the exact same voltage between C_3, are 36 V and 180 V, respectively. The voltage stresses between the diodes D_1, D_2, D_3, D_4, and D_0, and the main switch S when off are shown in Figures 10 and 11. As can be calculated from Equations (10)–(13), the voltage stresses between the switches are $V_{D_1} = 45$ V, $V_{D_3} = V_{D_4} = 178$ V, $V_{D_2} = 134$ V, and $V_{D_0} = V_S = 178$ V. The figures of the simulated waveforms, the derived equations, and the results clearly show their convergence.

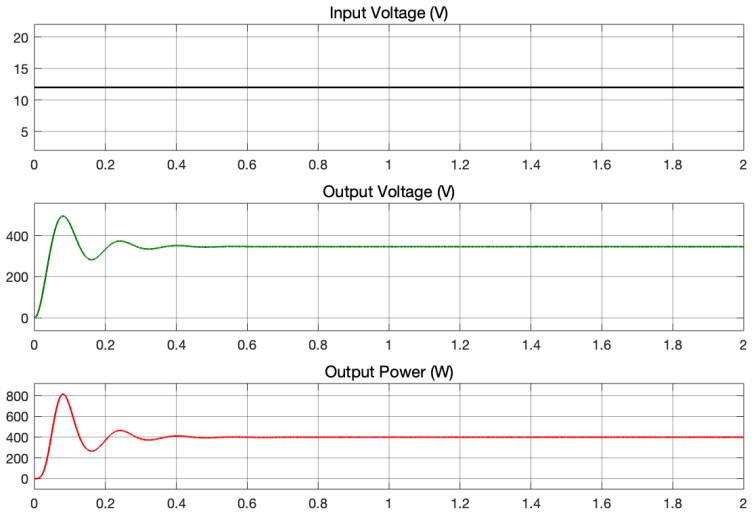


Figure 8. V_{in}, V_{out}, and P_{out} waveforms of the SISC converter.

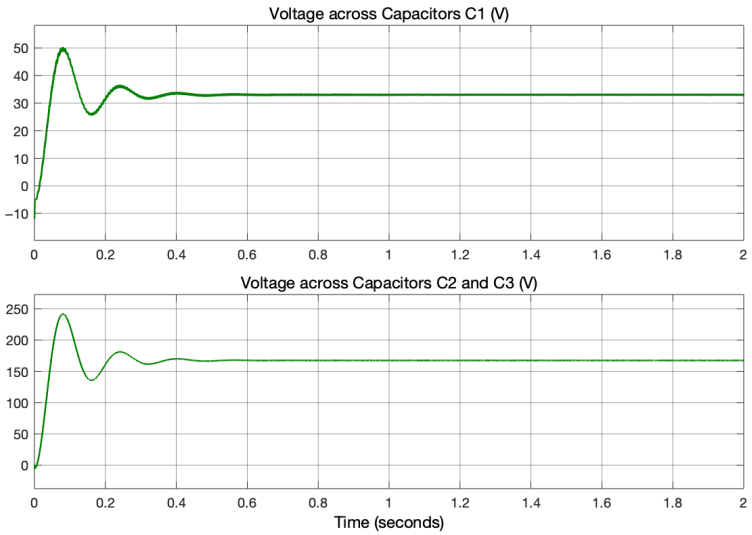
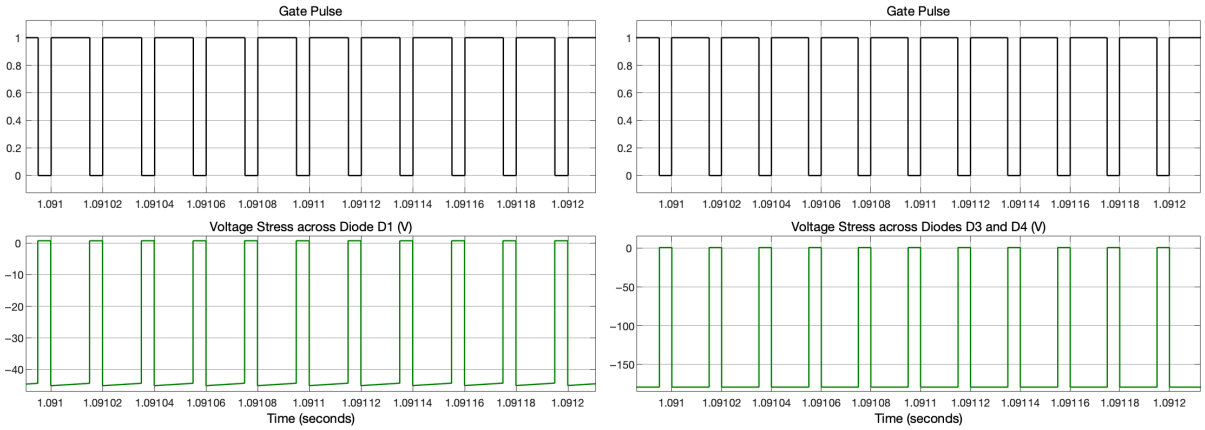
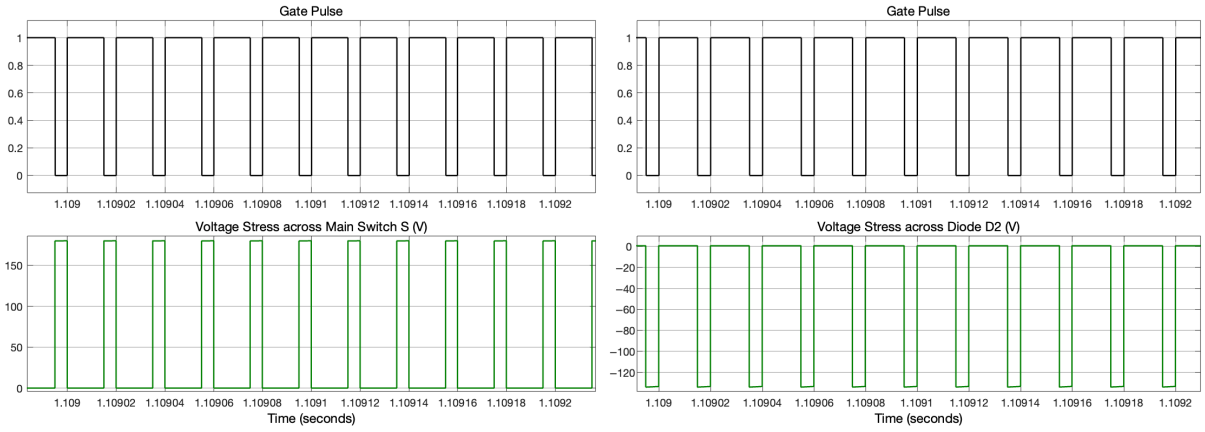


Figure 9. C_1, C_2, and C_3 waveforms of the SISC converter.

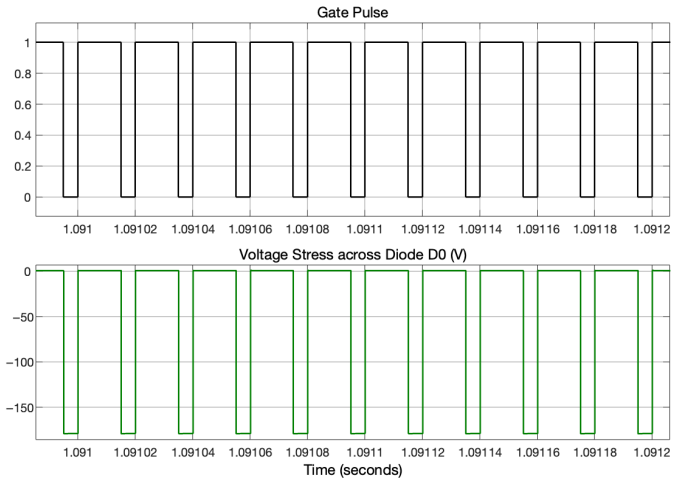


(**a**) (**b**)

Figure 10. Voltage stresses of the SISC converter in the ON-mode: (**a**) voltage stress between D_1; (**b**) Voltage stresses between D_3 and D_4.



(**a**) (**b**)



(**c**)

Figure 11. Voltage stresses of the SISC converter in the OFF-mode: (**a**) voltage stress between S; (**b**) voltage stress between D_2; (**c**) voltage stress between D_0.

5.2. ESISC Converter

A 400 W, 605 V model is simulated and tested to validate the performance of the proposed ESISC converter under steady-state operation conditions. The main purpose is

to justify the exact functionality of the proposed converter in terms of the voltage gain and the voltage stress between active and passive switches. The input voltage of 12 V is increased to an output voltage of 605 V with a duty cycle of 0.75 and an output power of 400 W, as shown in Figure 12. The voltage waveforms between the capacitors C_1, C_2, and C_3 are shown in Figure 13. Equations (20) and (21) predict the voltages of C_1 and C_2, which is the exact same voltage between C_3, 36 V and 324 V, respectively. The voltage stresses between the diodes D_1, D_2, D_3, D_4, D_5, D_6, D_7, and D_0, and the main switch S when off are shown in Figures 14 and 15. As can be calculated from Equations (23)–(27), the voltage stresses between the switches are $V_{D_1} = V_{D_6} = 44$ V, $V_{D_2} = 264$ V, $V_{D_3} = V_{D_4} = 308$ V, $V_{D_5} = V_{D_7} = 132$ V, and $V_{D_0} = V_S = 308$ V. The figures of the simulated waveforms, the derived equations, and the results clearly show their convergence.

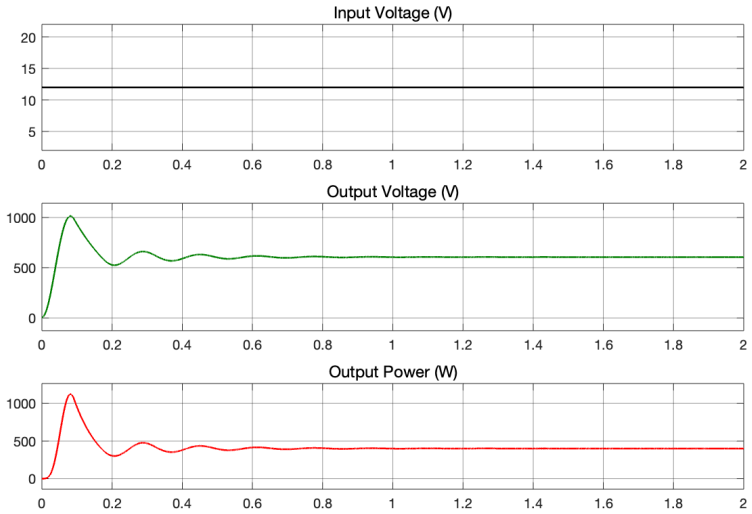


Figure 12. V_{in}, V_{out}, and P_{out} waveforms of the ESISC converter.

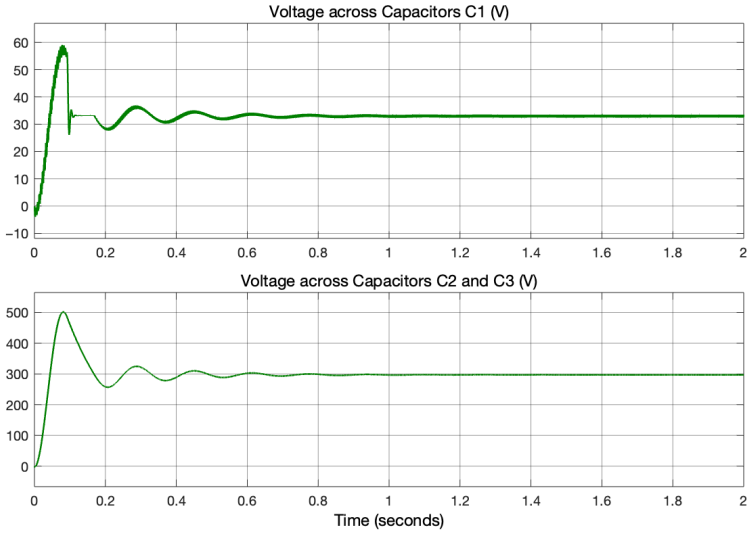
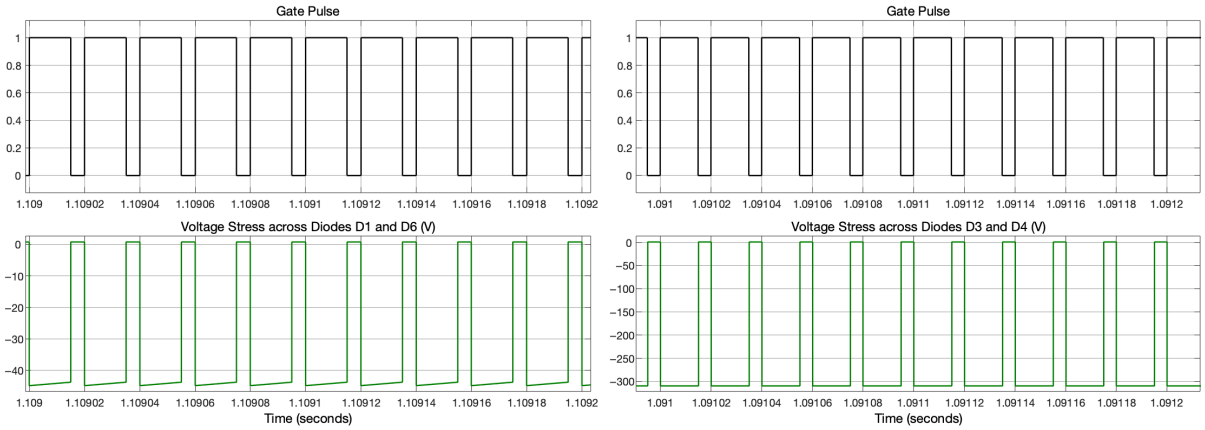
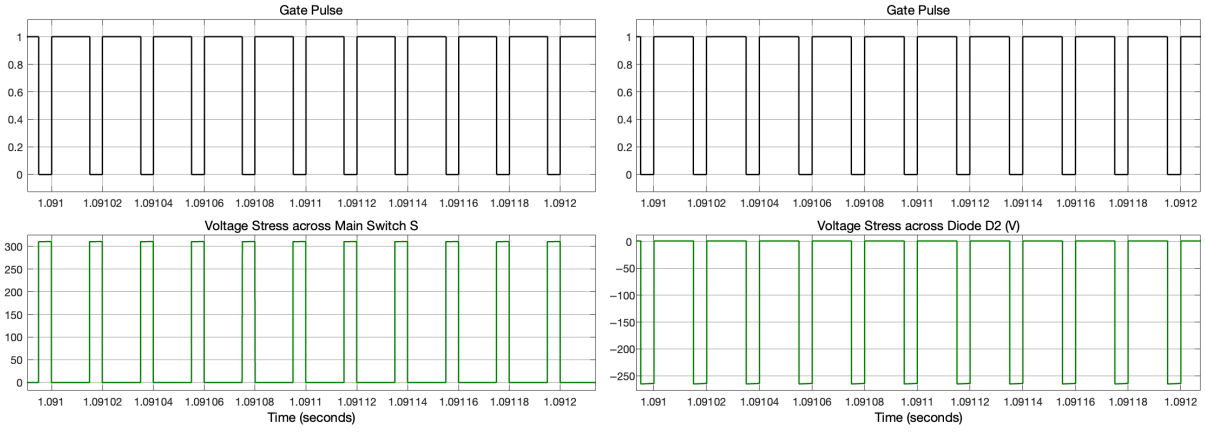


Figure 13. C_1, C_2, and C_3 waveforms of the ESISC converter.

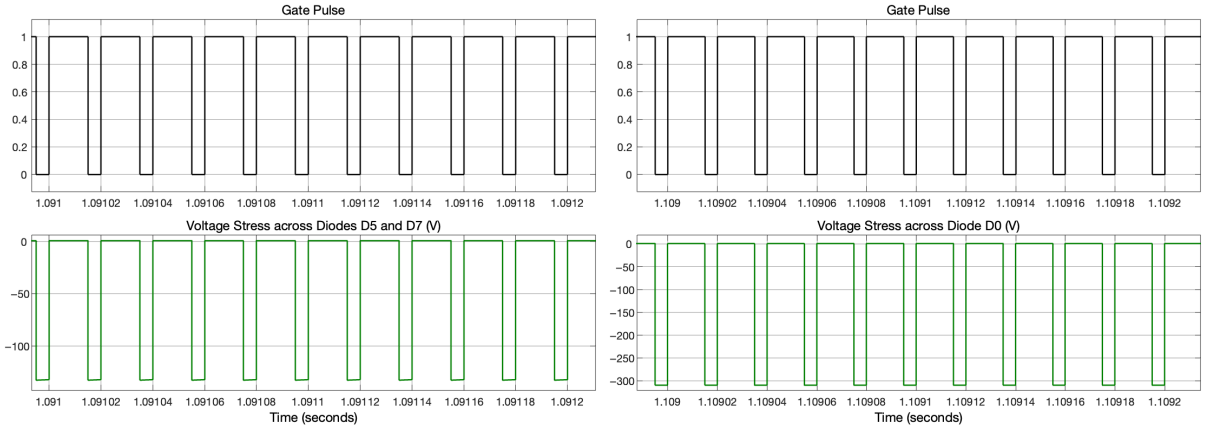


(**a**) (**b**)

Figure 14. Voltage stresses of the ESISC converter in the ON-mode: (**a**) voltage stress between D_1 and D_6; (**b**) voltage stresses between D_3 and D_4.



(**a**) (**b**)

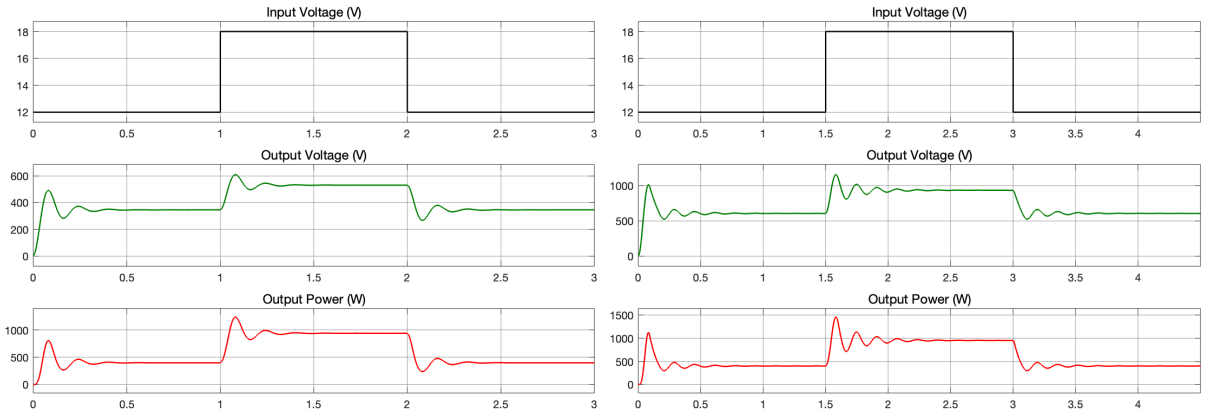


(**c**) (**d**)

Figure 15. Voltage stresses of the ESISC converter in the OFF-mode: (**a**) voltage stress between S; (**b**) voltage stress between D_2; (**c**) voltage stresses between D_5 and D_7; (**d**) voltage stress between D_0.

The stability of the two proposed converters is tested by introducing a disturbance to the input voltage and observing whether the output voltage will converge. A disturbance is applied by changing the input voltage from 12 V to 18 V, which represents an increase of 50%, and then returning to 12 V, as can be seen in Figure 16. The observed transient

overshoot is attributed to a sudden input voltage change and the absence of a closed-loop controller. The proposed converters remain stable, and all state variables converge to steady-state values.



(**a**) (**b**)

Figure 16. Time-domain response of the two proposed converters under an input voltage disturbance: (**a**) SISC converter. (**b**) ESISC converter.

6. Conclusions

This article has successfully discussed developing two topologies, SISC and ESISC, of step-up converters with high voltage gains. The method utilized to increase the input voltage involves the integration of an SI cell and an SC cell within the DC–DC converter. This substantial high voltage gain, which is approximately sixty times the input voltage when the duty cycle is 0.75 in the ESISC converter, is achieved without the use of a transformer, a very high duty cycle value, or coupled inductors. A comparison is made between the proposed topologies and different types of step-up DC–DC converters, showing that the proposed topologies are among the highest voltage gains. The proposed converters offer several advantages: high voltage gain; use of a single active switch; lower voltage stress on the main active switch with respect to the output voltage; and relatively few components, especially in the SISC converter. The voltage gain equations in steady-state are fully derived in detail, which agrees with the simulation results obtained by Matlab/Simulink software.

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Conflicts of Interest: The author declares no conflicts of interest.

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