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Grid State-Aware Adaptive Switching Between Grid-Following and Grid-Forming Modes Enabled by Fast Online Impedance Estimation

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Abstract

Changes in grid strength can impair the stability and dynamic performance of converters operated in fixed grid-following or grid-forming modes. Adapting the mode requires impedance estimation and preparation of the incoming controller. This paper proposes a single-converter strategy that combines impedance estimation using a notch–bandpass compound filter, hysteretic mode selection, and bidirectional controller state preparation. The estimator identifies resistance and inductance from the injected frequency response and reconstructs the fundamental frequency short-circuit ratio. The switching strategy coordinates grid strength requests with phase/amplitude synchronization and state initialization to reduce transfer transients. Conditional error and synchronization analyses establish the requirements linking estimation to mode execution. With matched measurement channels, 86 fixed-mode simulation configurations give a maximum final-interval short-circuit ratio error of 2.32 percent. In shared-input noiseless tests, the estimator has a median settling time of 130.85 milliseconds as measured from the network change command. At 20 kW, the converter peak current in a common transfer window from grid-following to grid-forming decreases from 217.41 to 45.83 A relative to direct transfer, a 78.9 percent reduction. These results support the proposed integration of online grid strength estimation and prepared mode transfer in the evaluated single-converter system.

Keywords: adaptive mode switching; grid-following converter; grid-forming converter; grid impedance estimation; short-circuit ratio; smooth mode switching

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1. Introduction

The increasing penetration of converter-interfaced renewable generation is changing the dynamic characteristics of power systems. Grid-following (GFL) converters regulate injected current by synchronizing with the point of common coupling (PCC) voltage, whereas grid-forming (GFM) converters establish an internal voltage vector and can provide voltage and frequency support. Their complementary operating ranges motivate adaptation when impedance in the external grid changes substantially [1–3]. Impedance-based analysis relates these ranges to converter control and grid strength, quantified here by the short-circuit ratio (SCR) [4–7].

Impedance-adaptive dual-mode control is established prior art. Li et al. combined 75-Hz interharmonic identification, SCR-dependent current source/virtual synchronous machine regions and prepared transfer [8]; other hybrid controls blend GFL and GFM behavior [9,10]. Passive estimation depends on available operating changes and network uncertainty [11,12]. Active approaches use event-triggered perturbations, harmonic currents, pseudo-random sequences, or short pulses [13–18]. These approaches trade off among excitation cost, frequency coverage, and response time. A filter-based extractor also has transient and observation window requirements; its latency cannot be inferred from the output update rate.

Controller preparation is a separate requirement. Gao et al. coordinated synchronization and controller/reference states for bidirectional GFL/GFM transfer [19]. Virtual resistance pre-synchronization also supports islanded to grid-connected GFM operation [20], a different transition from SCR-dependent GFL/GFM selection. Recent grid-forming stabilizers and power self-synchronization address wide-SCR stability and near-area multi-converter interactions [21,22]. They provide related stability results rather than online estimation benchmarks. Table 1 summarizes representative related methods, their reported quantitative evidence, and their relation to the present study.

Table 1. Representative related methods and their reported evidence. Metrics and platforms differ and do not establish a common ranking.

Study and Scope	Reported Quantitative Evidence	Relation to the Present Study
Mohammed et al. [13]; event-based estimation	2.2-kW experiment; a 0.3% voltage change triggers identification; reported estimates 1.40 Ω, 1.49 mH at 1.39 s.	Estimation without SCR-dependent GFL/GFM selection; estimates are not error values.
Li et al. [8]; integrated dual-mode control	100-kW experiment; SCR thresholds 20/3; identification < 40 ms; current THD about 2.81% at 5% injection.	Closest integrated precedent; 75-Hz MCCF/RDFT extraction differs from the present 525-Hz NBCF.
Gao et al. [19]; prepared transfer	15.8-kVA simulation, representative SCR 1.5; GFL-to-GFM current THD 17.56/0.22% without/with preparation.	Transfer-state coordination without online SCR estimation; a disclosed common-platform adaptation is assessed here.
Zhao et al. [20]; GFM presynchronization	10-kW hardware-in-the-loop setup; synchronization 0.2 s versus 0.4/0.8 s for its comparators.	Islanded/grid-connected GFM operation rather than GFL/GFM mode selection.

MCCF: multiple complex-coefficient filter; RDFT: recursive discrete Fourier transform; THD: total harmonic distortion.

The present study specifies and evaluates the interfaces of an estimation–decision–handover chain: reconstructed fundamental-frequency SCR qualifies a mode request, and synchronization and controller-state preparation govern its execution. The contributions are a matched-channel NBCF/projection model with conditional error propagation to SCR; executable confirmation, cancellation and synchronization rules; and common-frame command consistency conditions with explicit bidirectional assignments and local sampled synchronization analysis. These conditions make the connection between estimation and transfer traceable. Shared-input comparisons establish component-level comparability to the disclosed mature adaptations, while repeated SCR-driven sequences and a higher-power scheduled case assess the coordinated implementation. Complete coefficients, derivations and results, including unsuccessful cases, are provided in the Supplementary Material.

2. Converter Configuration and Grid Strength Definition

2.1. Shared Power Circuit and Dual-Mode Control

The three-phase voltage source converter (VSC) in Figure 1 connects to the PCC through an *LC* filter. The external network is represented by $Z_g(s) = R_g + sL_g$. Converter-side and grid-side currents are distinguished throughout. GFL control uses a phase-locked loop (PLL) and active/reactive power current references. GFM control uses a virtual synchronous generator (VSG) power–frequency loop and a reactive power–voltage loop to generate its internal voltage vector. Both modes share the power stage, modulator, and proportional–integral (PI) current controller. Thus, direct selection of unaligned angle/reference channels can change the commanded voltage even though physical inductor currents remain continuous.

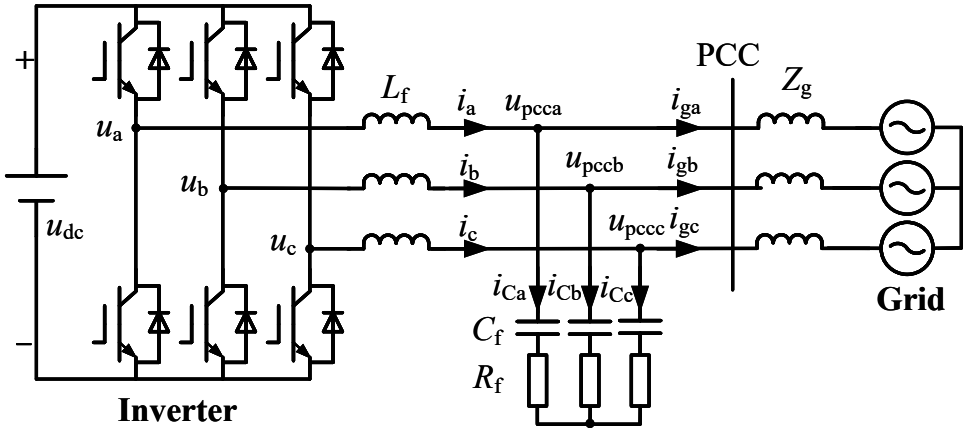


Figure 1. Configuration of the three-phase grid-connected converter used in this study. PCC voltage and grid-side current feed the estimator; converter-side current feeds the shared inner loop in Figure 2.

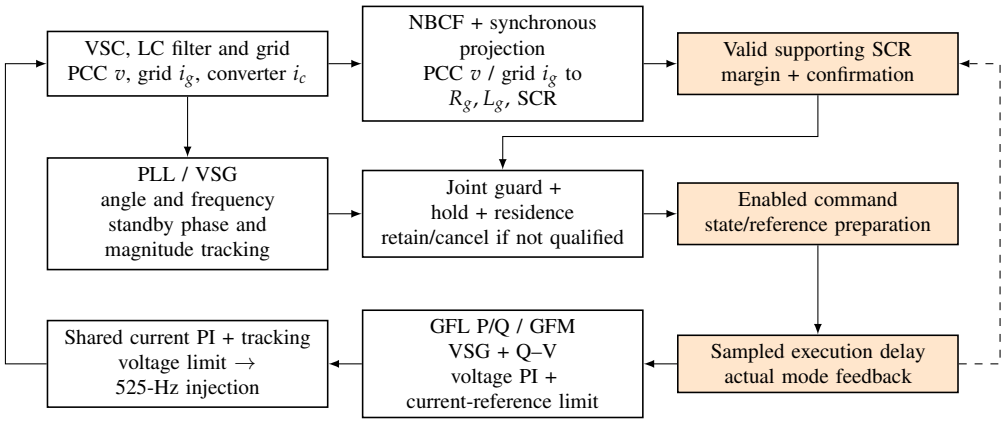


Figure 2. Executed sensing, request, preparation, and control paths. Dashed feedback uses actual mode; injection is added after the voltage command limit.

2.2. Injection Frequency Identification and Fundamental SCR

At angular injection frequency ω_h, $U_{\mathrm{pcc}}(h) = Z_g(h)I_2(h) + e(h)$, where $e(h)$ is the source background at that frequency. Neglecting this background and assuming a series-*RL* equivalent gives $\widehat{Z}_g(h) = U_{\mathrm{pcc}}(h)/I_2(h)$, $\widehat{R}_g = \mathrm{Re}\,\widehat{Z}_g(h)$, and $\widehat{L}_g = \mathrm{Im}\,\widehat{Z}_g(h)/\omega_h$. Both the DFT baseline and NBCF method reconstruct $\widehat{Z}_g(f_0) = \widehat{R}_g + j2\pi f_0 \widehat{L}_g$ before evaluating

$$\widehat{\mathrm{SCR}} = \frac{S_{\mathrm{ac}}}{P_e} = \frac{3U_{\mathrm{ph,rms}}^2}{P_e\left|\widehat{Z}_g(f_0)\right|} = \frac{U_{\mathrm{LL,rms}}^2}{P_e\left|\widehat{Z}_g(f_0)\right|}, \tag{1}$$

where P_e is the fixed rated active-power base shared by both modes. The line-to-line root mean square (RMS) voltage is $U_{\mathrm{LL,rms}} = \sqrt{3}U_{\mathrm{ph,rms}}$, with phase-to-neutral RMS voltage $U_{\mathrm{ph,rms}}$ and nominal frequency $f_0 = 50$ Hz. Operating P/Q references do not change the rated base. Using the magnitude at 525 Hz directly would give a different quantity. Reconstruction requires an adequate series-RL model at both frequencies; a frequency-dependent network requires a separate fundamental-frequency model or measurement.

3. Estimation and Guarded Mode Transfer

3.1. Matched Filtering and Causal Phasor Extraction

The NBCF applies identical fundamental-frequency notch and injection-frequency bandpass stages to the measured voltage and current:

$$N(s) = \frac{s^2 + \omega_0^2}{s^2 + (\omega_0/Q)s + \omega_0^2}, \tag{2}$$

$$B(s) = \frac{(\omega_h/Q_{\mathrm{bp}})s}{s^2 + (\omega_h/Q_{\mathrm{bp}})s + \omega_h^2}. \tag{3}$$

The notch and band-pass quality factors are Q and Q_{bp}, respectively; positive values give stable continuous filters, while their bilinear discretization maps poles inside the unit circle. Increasing Q_{bp} improves selectivity but lengthens the filter transient. The common steady-state complex gain cancels from the voltage/current ratio when the channels match, the injected response is nonzero, and the background is negligible. This cancellation does not require zero filter phase and does not remove measurement chain mismatches.

For the complex filtered $\alpha\beta$ signals v_f and i_f, the implemented causal projection is

$$\begin{aligned} a_v[k] &= \frac{1}{N_{\mathrm{p}}} \sum_{n=0}^{N_{\mathrm{p}}-1} v_f[k-n] e^{j\omega_h (k-n) T_s}, \\ a_i[k] &= \frac{1}{N_{\mathrm{p}}} \sum_{n=0}^{N_{\mathrm{p}}-1} i_f[k-n] e^{j\omega_h (k-n) T_s}, \\ \widehat{Z}_g(h,k) &= \overline{a_v[k]/a_i[k]}. \end{aligned} \tag{4}$$

The overbar denotes conjugation; the injected component rotates negatively under the model's coordinate convention. Both channels use the same carrier and timestamps. For a component $ce^{j\Omega k}$, the pre-conjugation extraction response is

$$a_x[k] = cH_d(e^{j\Omega}) W_{N_{\mathrm{p}}}(\Omega + \Omega_h) e^{j(\Omega+\Omega_h)k}, \qquad W_N(\nu) = \frac{1}{N} \sum_{n=0}^{N-1} e^{-j\nu n}, \tag{5}$$

where H_d is the product of the two discrete stages and $\Omega_h = \omega_h T_s$. The selected rotation has $W_N(0) = 1$; positive and negative fundamental rotations mix to $\Omega_h \pm \Omega_0$. Thus, notch leakage and finite-window rejection act jointly. A coherent background with the selected frequency and rotation is not separable by these filters.

The numerical implementation uses two second-order stages, $Q = Q_{\mathrm{bp}} = 25$, $T_s = 100$ µs, and $N_{\mathrm{p}} = 800$. The observation window is 80 ms and estimates update every 100 µs; neither is the total response time. Outputs require a filled window, finite non-negative identified R/L and a nonzero current denominator. This numerical screen is not an accuracy test. Filter states start at zero. Coefficients and baseline settings are listed in Supplementary Table S2. The historical digital signal processor (DSP) extraction configuration has not been recovered.

3.2. Conditional Error and Request Reliability

Let G_v, G_i be the residual complex measurement chain responses and $\varepsilon_v, \varepsilon_i$ the remaining extraction errors. With common gain H_h, the extracted phasors are $\widehat{U}_h = H_h G_v U_{\mathrm{pcc}}(h) + \varepsilon_v$ and $\widehat{I}_h = H_h G_i I_2(h) + \varepsilon_i$. If $|\varepsilon_i| < |H_h G_i I_2(h)|$, then the exact ratio error obeys

$$\left|\widehat{Z}_g(h) - Z_g(h)\right| \le \frac{\begin{array}{l}|H_h I_2(h) Z_g(h)|\,|G_v(j\omega_h) - G_i(j\omega_h)| \\ +\,|H_h G_v(j\omega_h) e(h)| \\ +\,|\varepsilon_v| + |Z_g(h)|\,|\varepsilon_i|\end{array}}{|H_h G_i(j\omega_h) I_2(h)| - |\varepsilon_i|}. \tag{6}$$

Background, mismatch, and residuals enter independently. A small extracted current can invalidate the denominator condition. For relative gain $g > 0$ and voltage-to-current delay $\Delta\tau = \tau_v - \tau_i$, the ideal matching error is $\widehat{Z}_g(h) = g e^{-j\omega_h \Delta\tau} Z_g(h)$, with the delay rotating injection frequency reactance into the resistance estimate. A common delay cancels in the steady ratio, but adds acquisition latency.

Define $\Delta Z_h = \widehat{Z}_g(h) - Z_g(h)$, $\Delta Z_0 = \widehat{Z}_g(f_0) - Z_g(f_0)$, and $\mathcal{T}(z) = \mathrm{Re}\, z + j(\omega_0/\omega_h)\,\mathrm{Im}\, z$. The actual fundamental-frequency reconstruction error is

$$\Delta Z_0 = \mathrm{Re}\,\Delta Z_h + j\frac{50}{525}\,\mathrm{Im}\,\Delta Z_h + b_{RL}, \qquad b_{RL} = \mathcal{T}(Z_g(h)) - Z_g(f_0). \tag{7}$$

Consequently, a small relative 525 Hz error need not imply a small relative 50 Hz error, and accurate injection frequency identification does not remove resonant network model bias. Supplementary Section S1 gives component error relations, conditional gain/delay regions, and residual budgets. These are analytic requirements, not demonstrated hardware specifications. Characterization of the complete probe/conditioning/acquisition chains remains necessary [23].

3.3. SCR Requests and Execution Guard

The nominal hysteresis selects GFM below 2 and GFL above 3, retaining the actual mode between these values; this band specifies a mode-preference policy with memory, but does not imply that only one mode is operable at each SCR. The values are converter-specific engineering settings rather than identified stability boundaries. Fixed-mode observations and the nominal switched sequence are examined separately in Section 4.3. With relative margin η, the implemented sufficient request conditions are

$$\begin{cases}(1-\eta)\widehat{\mathrm{SCR}} \ge 3, & \mathrm{GFM} \to \mathrm{GFL}, \\ (1+\eta)\widehat{\mathrm{SCR}} \le 2, & \mathrm{GFL} \to \mathrm{GFM}.\end{cases} \tag{8}$$

For $s = K/|Z_g(f_0)|$, $\widehat{s} = K/|\widehat{Z}_g(f_0)|$, and $K = U_{\mathrm{LL,rms}}^2/P_e$, the sufficient error premise is

$$\frac{|s-\widehat{s}|}{\widehat{s}} \le \frac{|\widehat{Z}_g(f_0) - Z_g(f_0)|}{|Z_g(f_0)|} \le \eta \quad \Longrightarrow \quad (1-\eta)\widehat{s} \le s \le (1+\eta)\widehat{s}. \tag{9}$$

Under this sample-wise premise, the request inequalities imply the correct true threshold direction. Confirmation rejects interrupted support, but cannot remove persistent bias or establish the premise. The synchronization guard tests controller alignment; it is not an online accuracy certificate.

Here, $\eta = 0.05$, giving sufficient request levels 1.9048 and 3.1579. Requests require 800 consecutive valid supporting samples (nominally 80 ms). Phase, magnitude, and frequency errors must then remain within 0.5°, 1% of rated phase-voltage peak (3.103 V), and 0.1 Hz

for 200 samples (nominally 20 ms). Residence is at least 0.1 s; nominal command-to-mode delay is one 100-µs sample. These numerical settings describe the simulation rather than recovered hardware tolerances.

An invalid estimate or loss of SCR support cancels the candidate and restarts confirmation; an interrupted guard hold restarts that hold. A continuously supported request waits if synchronization is incomplete, retaining the actual mode. No forced timeout transfer or verified hardware protection is included. A command-time guard also need not remain satisfied after an arbitrary execution delay; the sensitivity tests isolate this actuation path.

3.4. Synchronization and State Handover

Let $\boldsymbol{z}_i$ and (z_{vd}, z_{vq}) denote current- and voltage-PI integral states, while U_d, U_q denotes the PCC components in the selected synchronous frame. The shared current controller produces

$$\boldsymbol{u}_{dq} = K_{pi}(\boldsymbol{i}^*_{dq} - \boldsymbol{i}_{dq}) + \boldsymbol{z}_i + \omega_0 L_f \begin{bmatrix} -i_q \\ i_d \end{bmatrix}. \tag{10}$$

Let h_σ denote the voltage command map for mode σ, with controller states $\boldsymbol{x}_\sigma$, measured inputs $\boldsymbol{y}$, and references $\boldsymbol{r}_\sigma$. The ideal command consistency set is $\mathcal{M}_{a\to b} = \{h_b(\boldsymbol{x}_b, \boldsymbol{y}, \boldsymbol{r}_b) = h_a(\boldsymbol{x}_a, \boldsymbol{y}, \boldsymbol{r}_a)\}$ evaluated at one physical snapshot in a common stationary frame. This is an output equality condition, not a reset algorithm. With equal scalar current gains and cross-coupling coefficients, the applied-reference and integrator differences satisfy

$$\begin{aligned} \Delta\boldsymbol{i}^*_{\alpha\beta} &= R(\theta_b)\boldsymbol{i}^*_b - R(\theta_a)\boldsymbol{i}^*_a, \\ \Delta\boldsymbol{z}_{i,\alpha\beta} &= R(\theta_b)\boldsymbol{z}_{i,b} - R(\theta_a)\boldsymbol{z}_{i,a}, \\ \Delta\boldsymbol{u}_{\alpha\beta} &= K_{pi}\Delta\boldsymbol{i}^*_{\alpha\beta} + \Delta\boldsymbol{z}_{i,\alpha\beta}, \end{aligned} \tag{11}$$

where $R(\theta)$ maps dq components into the common stationary frame. The physical-current terms cancel because planar rotations commute with the common cross-coupling rotation. For the common radial voltage limiter Π_V, write $\delta_\theta = \mathrm{wrap}(\theta_b - \theta_a)$, $\epsilon_r = \|\boldsymbol{i}^*_b - \boldsymbol{i}^*_a\|_2$ and $\epsilon_z = \|\boldsymbol{z}_{i,b} - \boldsymbol{z}_{i,a}\|_2$. Non-expansiveness and the planar rotation norm give

$$\begin{aligned} \|\Pi_V(\boldsymbol{u}_b) - \Pi_V(\boldsymbol{u}_a)\|_2 \le K_{pi}\epsilon_r + \epsilon_z \\ + 2\left|\sin\frac{\delta_\theta}{2}\right|\left(K_{pi}\|\boldsymbol{i}^*_a\|_2 + \|\boldsymbol{z}_{i,a}\|_2\right). \end{aligned} \tag{12}$$

The commands and limiter in (12) are evaluated in the same stationary frame and physical snapshot. Exact aligned applied references and retained integral states give zero command jump; finite frame/reference mismatch gives the stated conditional bound. The unchanged injected voltage cancels in the difference. This output condition does not require every filter or physical state to be reset, and does not imply invariance under subsequent dynamics. The detailed rotation argument is given in Supplementary Section S2.

The GFM voltage loop produces the following current references before the common radial current reference limit:

$$\begin{aligned} i^*_d &= K_{pv}(E - U_d) + z_{vd} - \omega_0 C_f U_q, \\ i^*_q &= -K_{pv}U_q + z_{vq} + \omega_0 C_f U_d. \end{aligned} \tag{13}$$

Solving (13) for the held GFL reference gives the forward voltage-PI initialization below. The reverse assignment copies the GFM reference and aligns the auxiliary GFL angle:

$$\mathcal{R}_{\mathrm{GFL}\to\mathrm{GFM}}:\quad \begin{cases} \theta^{+}_{\mathrm{GFM}} \leftarrow \theta_{\mathrm{GFL}}, \quad \omega^{+}_{\mathrm{GFM}} \leftarrow 2\pi f_{\mathrm{PLL}}, \quad E^{+} \leftarrow U, \\ z^{+}_{vd} \leftarrow i^{*}_{d,\mathrm{hold}} + \omega_0 C_f U_q - K_{pv}(E^{+} - U_d), \\ z^{+}_{vq} \leftarrow i^{*}_{q,\mathrm{hold}} - \omega_0 C_f U_d + K_{pv} U_q, \end{cases} \tag{14}$$

$$\mathcal{R}_{\mathrm{GFM}\to\mathrm{GFL}}:\quad \begin{cases} \boldsymbol{i}^{*}_{\mathrm{GFL}} \leftarrow \boldsymbol{i}^{*}_{\mathrm{GFM}}, \\ \delta \leftarrow \mathrm{wrap}(\theta_{\mathrm{GFM}} - \theta_{\mathrm{PLL,raw}}), \quad \theta_{\mathrm{GFL}} = \theta_{\mathrm{PLL,raw}} + \delta. \end{cases} \tag{15}$$

At the forward command edge, substitution gives the held reference exactly in the aligned ideal case; an already-limited held reference is unchanged by the common radial current limit. In reverse, angle alignment and a common limited reference satisfy the same output condition. The shared current-PI integrals are retained; numerical equality alone is insufficient when their frames differ. The raw PLL is not reset. During GFL operation, inherited references track their P/Q targets and the auxiliary offset decays. Table 2 lists the continuously retained and assigned states. Held-sample age and command-to-execution mismatch are assessed numerically below.

Table 2. State treatment in the executed bidirectional transfer.

State or Signal	GFL → GFM	GFM → GFL
Physical electrical states	Continuous; no reset	Continuous; no reset
Raw PLL, acquisition/NBCF and power filters	Continue running	Continue running
GFM angle/frequency/magnitude	Inherit aligned PLL/filtered magnitude	Enter standby synchronization
Voltage-PI integrators	Initialize using (14)	Retain states; inactive branch runs
Shared current-PI integrators	Retain, with common tracking	Retain, with common tracking
GFL current-reference tracker	Held reference used for map	Inherit voltage-loop reference, then track target
PLL auxiliary offset	No raw-PLL reset	Prepare on command, then release
Phase-increment filter and held samples	Continue on their existing clocks	Continue on their existing clocks
Supervisor memories	Reset counts on mode change	Reset counts on mode change

Standby synchronization reduces phase and magnitude mismatch prior to these assignments. Its local convergence concerns controller alignment, whereas the reset equations concern command consistency at the handover instant.

Let $e_\theta = \mathrm{wrap}(\theta_{\mathrm{GFL}} - \theta_{\mathrm{GFM}})$ and $e_E = U - E_{\mathrm{GFM}}$, where U is the filtered PCC magnitude. Standby GFM frequency uses the filtered PLL angle increment rather than assuming that the separately filtered PLL frequency is its derivative:

$$\begin{aligned} \nu[k] &= \frac{\mathrm{wrap}(\theta_{\mathrm{GFL}}[k] - \theta_{\mathrm{GFL}}[k-1])}{T}, \\ \omega_\theta[k] &= \rho\omega_\theta[k-1] + (1-\rho)\nu[k], \qquad \rho = e^{-T/\tau_\theta}, \\ a[k] &= K_\theta e_\theta[k] - K_\omega(\omega_{\mathrm{GFM}}[k] - \omega_\theta[k]). \end{aligned} \tag{16}$$

Magnitude preparation uses $\dot{E}_{\mathrm{GFM}} = K_E e_E$. For constant local input and away from wrapping/limits, the phase error satisfies $\ddot{e}_\theta + K_\omega \dot{e}_\theta + K_\theta e_\theta = K_\omega(\omega_{\mathrm{ref}} - \omega_\theta)$. Positive gains give damped convergence, with rate filter error as a decaying input. The sampled

multiple-rate matrix and its pole check are given in Supplementary Section S2; this local result does not prove complete hybrid system stability or a finite preparation deadline.

The supervisor/integrator periods are 100/5 µs; $\tau_\theta = 20$ ms, $K_\theta = 400\ \mathrm{s}^{-2}$, and $K_\omega = K_E = 40\ \mathrm{s}^{-1}$. Active GFM operation retains the following separated damping and power–frequency droop:

$$J\dot{\omega} = \frac{P^* - P}{\omega_0} - D_d(\omega - \omega_{\mathrm{PLL}}) - \frac{K_f}{\omega_0}(f_{\mathrm{PLL}} - f_0), \qquad K_f = 27.2\ \mathrm{kW/Hz} \tag{17}$$

where $J = 0.14$, $D_d = 48$, and $K_f = P_e/(0.05 f_0)$ is a declared design choice. The controller uses PLL measurements, not the prescribed source frequency; hence, a 20-kW reference under frequency offset need not yield 20-kW output.

Both reference/offset tracking time constants are 50 ms. The common radial current reference and voltage command limits are 175.33 A and 427.5 V, respectively; PI tracking gains are 200/1000 s^{-1} for voltage/current loops. Injection is added after voltage limiting. Reference limiting does not impose an instantaneous physical-current ceiling. Supplementary Section S2 specifies the saturation/tracking implementation.

4. Numerical Results and Discussion

4.1. Common Settings and Evaluation Protocol

All primary results use the final controller described above. Table 3 separates fixed rating, electrical settings, and operating references, including pulse width modulation (PWM). The nominal switched network has a common 0.1 Ω resistance and two 4 mH branches in parallel, one through a breaker (10^{-4} Ω on-resistance, 10^6 Ω snubber). Commands at 2/4 s give nominal SCR 1.6845 → 3.3377 → 1.6845. Phase commutation is not simultaneous; command-referenced response includes it.

Table 3. Common numerical settings. Changed factors are identified with each test.

Quantity	Value
Voltage/rated-power/nominal-frequency bases	380 V line RMS/68 kW/50 Hz
DC source/PWM/electrical step	900 V/10 kHz/5 µs
Converter filter L_f/C_f	1 mH/30 µF per phase
External network/commands	0.1 Ω; 4 → 2 → 4 mH at 2/4 s
Default external P^*/Q^*	20 kW/300 var
Current PI/voltage PI gains	2.5/1000/0.5/200
Injection/NBCF/projection	525 Hz, 10 V peak command; $Q = Q_{\mathrm{bp}} = 25$; 800 points
Acquisition/estimator update	100 µs/100 µs
Selector/guard	2/3 thresholds; 5%/80 ms qualification; 0.5°/1%/0.1 Hz held 20 ms

Estimator settling is the first entry into a 5% complex-Z_{50} error band maintained for 50 ms; invalid samples interrupt the hold. Times start at the network command, with a 1.5-s search interval. Steady metrics use $[1, 1.9)$, $[3, 3.9)$, and $[5, 6]$ s for the six-second sequences. Reported relative errors use reference values as denominators; the SCR premise in (9) instead uses the estimate. Unestablished holds are retained. Window length, output update, change detection, and settling are reported separately.

With t_e denoting the logged actual mode execution time, the current-tracking integral absolute error (IAE) is $\mathrm{IAE}_i = \int_{t_e}^{t_e+0.5} \|\boldsymbol{i}_{dq} - \boldsymbol{i}^*_{dq,\mathrm{lim}}\|_2\, dt$. P/Q integrals use absolute native feedback errors against external targets over the same interval. Three-phase peaks use raw 5-µs samples over $[t_e - 20\ \mathrm{ms}, t_e + 100\ \mathrm{ms}]$, and can precede execution. Voltage deviation is the maximum phase trailing-cycle RMS deviation from $380/\sqrt{3}$ V. Recovery

requires a 100-ms hold within the final steady mean ± 2% of the rated quantity; zero denotes an established hold from the evaluation origin, whereas unexecuted or unrecovered events have no successful recovery time. Harmonic THD covers orders 2–50; the 525-Hz interharmonic is separate. Supplementary Sections S3 and S5 provide detector, window, and censoring details.

4.2. Shared-Input Estimator Comparison

Ten six-second trajectories fix GFM or GFL under 50/49.5/50.5 Hz, 50 Hz with 2% source unbalance, and 49.5 Hz with the same unbalance. All estimators receive identical PCC voltage/current samples, timestamps, and 525-Hz excitation, without true grid impedance or source frequency as online inputs. Comparators are an 80-ms one-sample sliding DFT, MCCF/RDFT based on [8,24], and variable forgetting factor recursive least squares (VFF-RLS) based on [25]. The latter two are 525-Hz/common platform adaptations, not reproductions of the original hardware. Their settings and known-impedance checks are given in Supplementary Section S3. The comparison results of the four methods are presented in Figure 3.

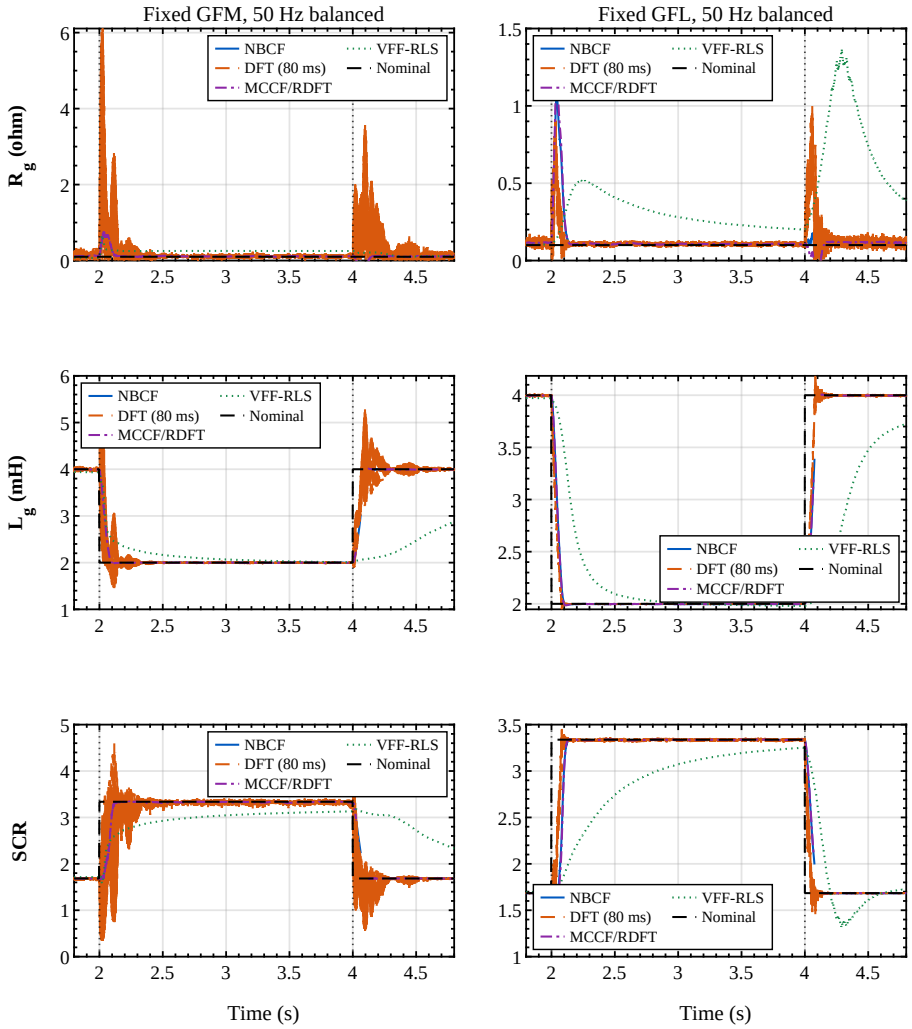


Figure 3. Shared-input estimation in fixed GFM (**left**) and GFL (**right**), 50 Hz balanced source. The same 525 Hz excitation and 100 µs samples feed every method. Dashed references denote the nominal balanced network after each command; phase commutation is not separately observed. Invalid outputs are gaps. The documented MCCF/RDFT and VFF-RLS curves are adaptations.

Each trajectory also receives 20 paired Gaussian phase-channel noise realizations, with standard deviations 0.219393 V and 0.103315 A. These 200 algorithm replays provide 400 event opportunities per method, not independent plant or hardware repetitions. Five separate training seeds and predeclared parameter grids are used for tuning; evaluation seeds are not reused for selection. NBCF defaults and the main DFT window are fixed beforehand.

The sliding-DFT 37.16% mean in Table 4 aggregates ten records; it is not the error at exactly 50 Hz. Balanced 50 Hz errors are 4.23/1.60% for GFM/GFL. An 80 ms window spans four 50 Hz and 42 injection cycles, but only 3.96/4.04 fundamental cycles at 49.5/50.5 Hz. The resulting fundamental leakage can contaminate the weak 525 Hz response, and need not cancel in its voltage/current ratio. The reconstruction in (7) retains resistance error relative to the smaller 50 Hz impedance. Supplementary Section S3.1 separates all conditions and reports direct-window and saved-waveform attribution checks. This comparison concerns the stated unprefiltered rectangular sliding DFT, not every DFT realization.

Table 4. Shared-input estimator results over all ten trajectories (five grid conditions in both fixed modes). Errors and valid coverage are equal-weight means of per-trajectory steady statistics; errors are conditional on each trajectory's valid outputs. Times are conditional event medians, with successful-event denominators. Superscript *a* denotes a disclosed adaptation.

Method	Noise	Valid (%)	Z_{50} (%)	SCR (%)	Holds	T_{50} (ms)
NBCF	No	100.00	1.48	0.11	20/20	130.85
NBCF	Yes	95.18	4.05	0.64	399/400	143.90
Sliding DFT	No	73.54	37.16	10.91	4/20	197.40
Sliding DFT	Yes	71.58	37.93	11.07	79/400	294.30
MCCF/RDFT [a]	No	100.00	1.48	0.11	20/20	132.15
MCCF/RDFT [a]	Yes	95.07	4.10	0.64	399/400	155.70
VFF-RLS [a]	No	57.56	11.82	5.77	3/20	115.40
VFF-RLS [a]	Yes	46.62	divergent	47.53	0/400	–

NBCF and the MCCF/RDFT adaptation both establish 20/20 clean holds, with 1.48% steady Z_{50} error and median 130.85/132.15 ms settling. With noise, both establish 399/400 holds while valid coverage is about 95%. Thus, the NBCF realization provides comparable estimation performance to this mature adapted baseline under the common protocol. Seed-paired timing intervals include zero, and one nominal GFL event favors sliding DFT; the evidence does not establish general speed superiority. The noisy RLS adaptation diverges, and remains an unsuccessful implementation under these settings rather than a performance characterization of published RLS. Supplementary Tables S3 and S4 and Figure S2 retain complete errors, unmatched change detector flags, failed event denominators, RLS diagnostics, and the speed–error tradeoff.

4.3. Final-Model Grid Strength and Parameter Coverage

The 86 three-second fixed-mode configurations comprise seven SCR values (1.5, 1.9, 2.1, 2.5, 2.9, 3.1, 4) in both modes; current/voltage PI multipliers 0.8/1.2, $P^* = 30/40$ kW, $Q^* = \pm 6.8$ kvar, and $R/X = 0.1/0.5/1$ at SCR 1.9/2.5/3.1 in both modes; and 49.5/50.5-Hz or 2% source-voltage unbalance cases at SCR 2.5. Changing R/X holds SCR constant. Each case is assessed over its last second. This is single-factor coverage, not a full-factorial experiment or continuous stability domain.

As shown in Figure 4, all 86 pass the stated final-interval observation gate: valid estimates, SCR error at most 5%, finite voltage/current and modulation magnitude at most unity. Maximum SCR/R/L errors are 2.32/51.04/0.503%, and maximum modulation is 0.816. Small SCR error does not ensure accurate resistance. A descriptive pairing of

the seven nominal SCR points gives maximum phase-RMS deviations of 1.28/1.93% for GFM/GFL and last-second converter peak ranges of 45.91–48.03/46.95–48.55 A. Both modes pass at every paired point; these observations identify neither an exclusive stability boundary nor an optimal threshold. Supplementary Table S7 reports the pairs. For the switched demonstration, nominal SCR endpoints 1.6845/3.3377 lie beyond the implemented 1.9048/3.1579 request levels, establishing consistency of the chosen policy with that sequence. At 49.5/50.5 Hz, fixed-GFM mean PCC active power is 33.47/6.01 kW despite the 20-kW reference, whereas fixed GFL gives about 20.06 kW.

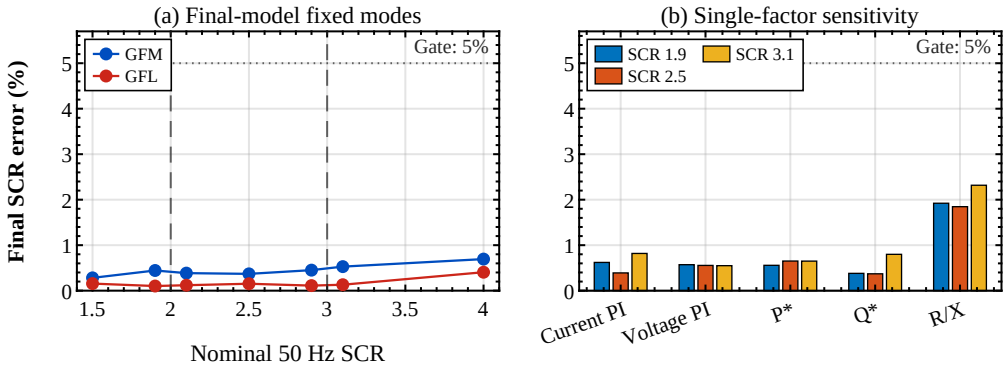


Figure 4. Final-model fixed-mode SCR observations: (**a**) seven SCR settings in both modes at base gains, the dashed lines represent the switching thresholds; (**b**) worst final-interval SCR errors across the specified single-factor variations and both modes at SCR $= 1.9, 2.5, 3.1$. Each record runs for 3 s and is assessed over its final 1 s. The 5% line is an observation gate, not a stability or uncertainty boundary; connecting lines are visual guides.

Eight further automatic sequences separately vary current/voltage PI multipliers, P or Q. All execute both transfers; final SCR errors are at most 0.54%. The 40-kW case reaches 179.31 A despite the 175.33 A reference limit. Full parameter and closed-loop results appear in Supplementary Tables S6 and S8.

4.4. Fair Transfer Comparison and Automatic Operation

At fixed SCR 2.5 and 50 Hz (direct transfer), the proposed preparation and a Gao-inspired adaptation share the plant, active controller gains, external references, and limits. Tests use both directions and 20/30/40 kW with 300 var. Preparation starts at 1.5 s and command is scheduled at 2 s; the proposed method is not forced through an unmet guard. The direct comparator omits standby synchronization and state/reference inheritance. The Gao adaptation retains angle inheritance, causal operating-point holding, and staged restoration without the proposed voltage-PI initialization or decaying PLL offset. Its structural substitutions and causal stationarity criterion can be found in Supplementary Section S5. The comparison results are shown in Table 5. The results do not establish a general ranking of the published methods.

At 40 kW, the common scheduled GFL-to-GFM case in Figure 5 gives converter window peaks of 89.97/100.28 A and maximum phase-RMS voltage deviations of 1.33/3.18% for the proposed and Gao-inspired implementations. The peak reduction is 10.3%; the proposed maximum occurs at 1.99131 s, before execution at 2.0001 s; it is not a post-transfer overshoot. The prepared strategies are comparable at 20 kW, while proposed reverse-direction peak and voltage deviation can exceed both comparators. Thus, the advantage is case- and direction-dependent. Supplementary Tables S12 and S17 retain the complete cases, integrals, recovery, limits, and spectra.

Table 5. Both transfer directions at fixed 20/40 kW and 300 var external targets.

Direction	P^* (kW)	Method	$I_{g,pk}$ (A)	$I_{c,pk}$ (A)	IAE (A s)	ΔU (%)	T_P (ms)
GFM → GFL	20	Proposed	47.30	48.29	1.170	2.55	0.00
GFM → GFL	20	Direct	45.91	46.88	1.242	2.43	0.00
GFM → GFL	20	Gao-adapted	45.61	46.73	1.237	2.43	0.00
GFL → GFM	20	Proposed	45.42	45.83	2.430	2.12	61.62
GFL → GFM	20	Direct	215.76	217.41	2.973	31.97	478.03
GFL → GFM	20	Gao-adapted	44.52	44.56	2.430	2.19	0.00
GFM → GFL	40	Proposed	94.29	94.77	1.198	2.64	70.85
GFM → GFL	40	Direct	87.21	89.06	1.425	1.59	0.00
GFM → GFL	40	Gao-adapted	87.41	90.89	1.444	1.54	0.00
GFL → GFM	40	Proposed	89.03	89.97	2.426	1.33	0.00
GFL → GFM	40	Direct	225.24	227.35	2.993	32.19	446.38
GFL → GFM	40	Gao-adapted	99.79	100.28	2.428	3.18	69.04

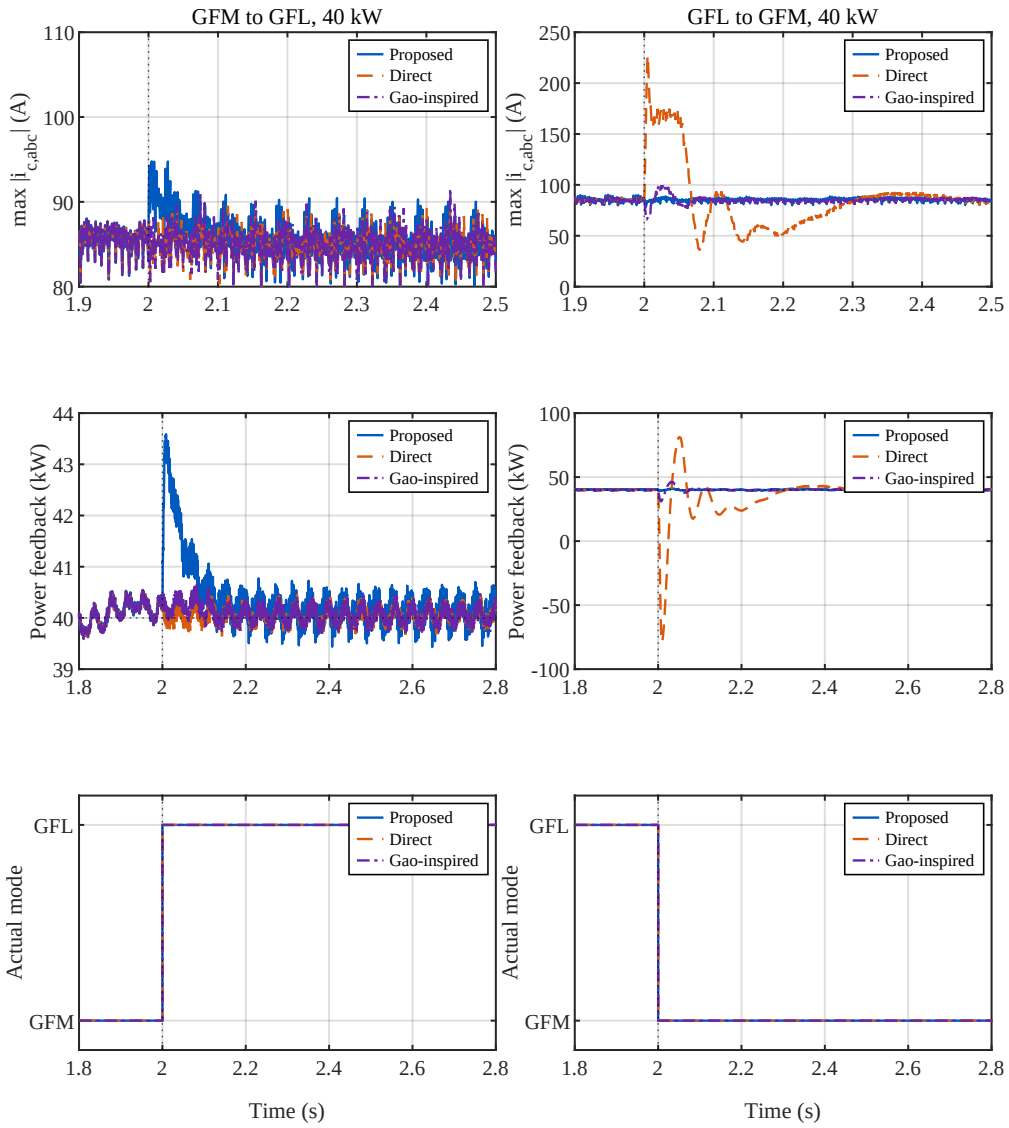


Figure 5. Common-platform scheduled 40 kW comparison: GFM-to-GFL (**left**) and GFL-to-GFM (**right**). Converter-current envelopes retain each one-millisecond bin maximum at its original 5 µs timestamp. Power and actual mode retain the original time axis; the vertical line marks the common planned command. The reverse direction is retained to show the direction-dependent tradeoff.

Figure 6 connects estimated grid strength to the request and actual handover. In the balanced sequence, proposed execution occurs at 2.2026/4.2535 s; second-transfer converter window peaks are 224.70/46.92/47.37 A for direct/proposed/Gao-adapted operation. With 2% source unbalance, the proposed chain completes both transfers at 2.2044/4.2500 s with a 49.54 A second-window peak; the Gao adaptation completes only the first, as its disclosed restoration stage is unfinished at 6 s. This case demonstrates repeated request-to-execution coordination within the observed horizon, not general superiority over Gao's original method; no second-event metric is assigned to its unexecuted event. The eight parameter variations and five frequency/unbalance sequences also execute both proposed transfers. Nevertheless, the combined 49.5 Hz/unbalanced case retains a transient valid SCR minimum of 0.2103 and a 175.73 A whole-run converter peak near the network change, before handover. Final-interval accuracy is not a transient guarantee.

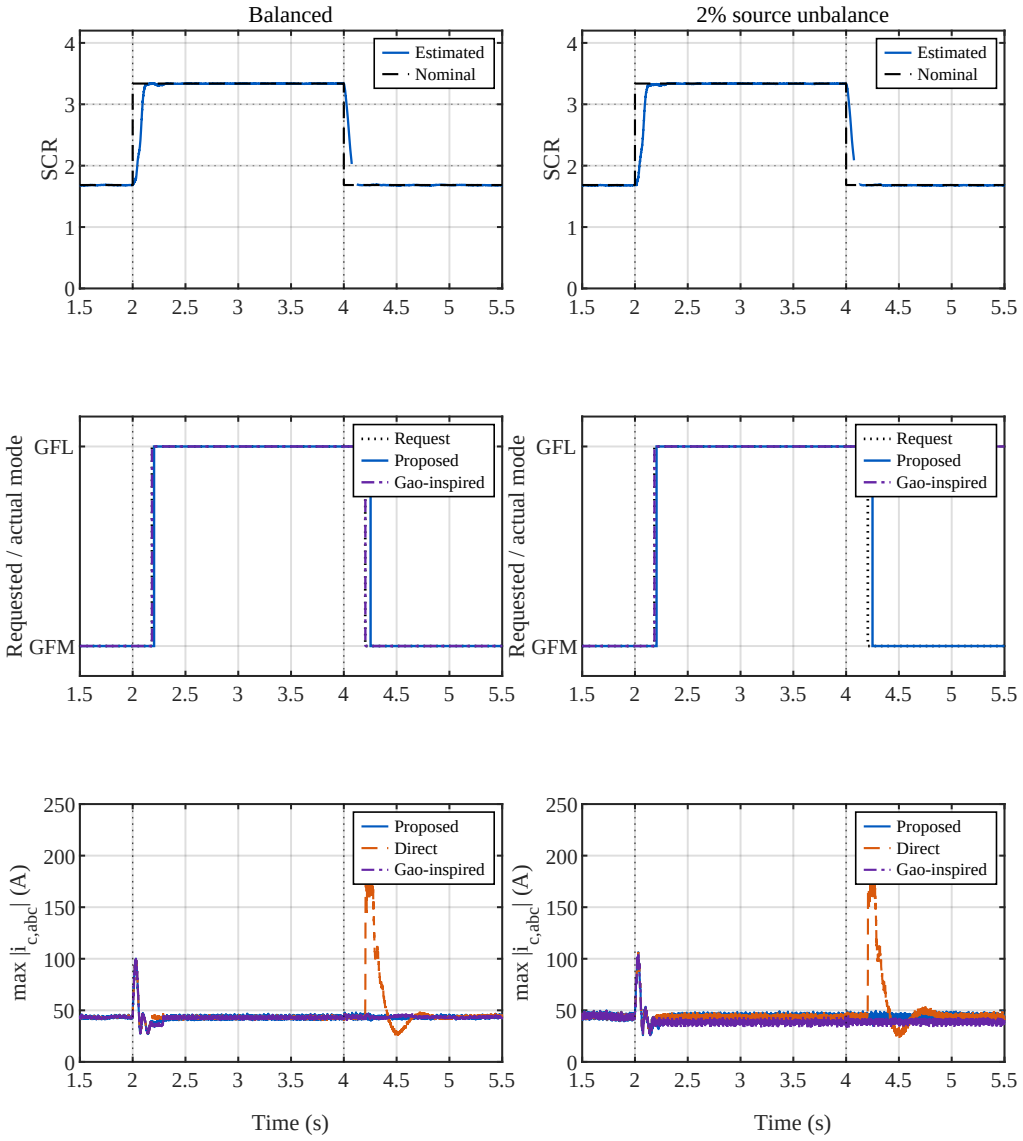


Figure 6. Automatic 4–2–4 mH sequences under balanced and 2% source-voltage unbalanced conditions. (**Top**): Reconstructed SCR and nominal-network reference, with invalid estimates shown as gaps and nominal 2/3 levels dotted. (**Middle**): Proposed request and actual modes of the proposed and Gao-inspired chains. (**Bottom**): Converter-current bin maxima at original timestamps, including direct transfer. Breaker commands at 2/4 s precede the guarded handovers; different execution times characterize the complete chains.

With three noise seeds per point, SCR 2.02/2.98 causes no final model false transfer; the 5% margin also defers nominal rule crossings at 1.98/3.02 in every record. Crossings at 1.8/3.2 execute in all three. Across the 18 noisy records, accepted final output coverage is 89.08–100%, with maximum reference-normalized accepted SCR error 6.83%; these observations do not establish the premise in (9). These counts do not estimate population error probabilities. Supplementary Section S4 retains all counts and causal margin/hold replays, including confirmations censored by the saved actual mode trajectory.

4.5. State Consistency and Synchronization Sensitivity

The same physical snapshot audit at 20/30/40 kW gives pre-/post-limit command residuals of 0.023261/0.003982/0.071366 V for GFM-to-GFL and numerical zero in reverse, using the declared 100-µs held reference age. Active equation reconstruction errors are below 10^{-7} V. These records evaluate the finite-residual distinction in (12); they do not demonstrate exact all-state resetting or hardware bumplessness.

The scheduled tolerance/delay sweep includes phase 0.25/1°, magnitude 0.5/2%, and additional actuation delays 100/300/500 µs in both directions plus a tight combined case. A prepared controller can give identical responses across tolerances. Targeted GFL-to-GFM cases in Figure 7 instead initialize the inactive state with +5°/+5% mismatch and allow command from 1.52 s following a 1.5-s request. Nominal guard readiness requires 236.7 ms, while phase tolerances 0.25/1° give 280.2/167.2 ms. Positive-mismatch variants reach 46.57–47.50 A window peaks. All twelve targeted records pass the last pre-reset joint guard; this does not guarantee preservation under arbitrary delay. Full bidirectional sweeps, opposite-sign control, and pre-/post-execution peaks can be found in Supplementary Section S5.

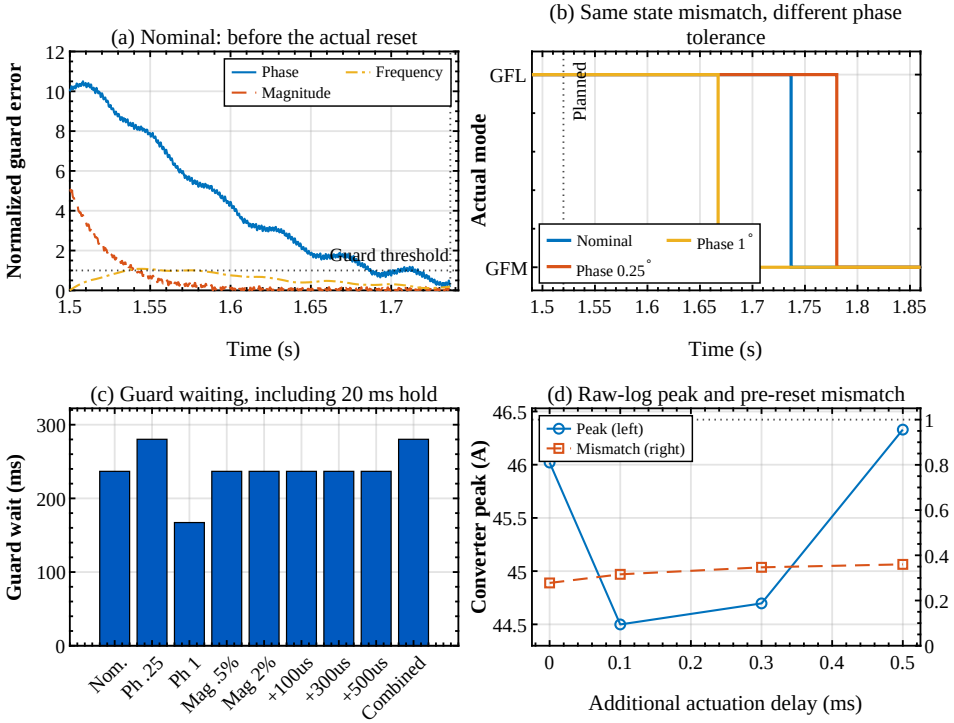


Figure 7. Targeted inactive-state mismatch assessment. (**a**) Nominal guard ratios before the actual reset; post-reset zeros are excluded. (**b**) Actual modes with the same initial mismatch and different phase tolerances. (**c**) First completed guard hold from the request for the nine positive-mismatch settings. (**d**) Post-transfer converter peaks from raw 5 µs logs and last pre-reset phase/magnitude ratios under additional execution delay. This stimulus changes the standby controller state, not the electrical-source phase or voltage.

Two guard bias diagnostics establish requests but execute no transfer: support loss cancels one, while the other remains pending at record end. Supervisor checks also cover invalid estimates and interrupted holds. The tests for additional delay alter only command-to-mode execution; they do not emulate complete acquisition, computation, and PWM latency or establish a hardware timeout policy.

4.6. Measurement, Network, and Injection Limits

The following tests separate common transport delay, relative-channel mismatch, coherent background, and network-model bias. Twenty-four relative gain/delay configurations on the two nominal trajectories, each clean and with the same 20 noise seeds, give 1008 paired replays. Delay is applied causally on raw 5-µs logs before acquisition; negative relative delay delays current. These perturb only the estimation branch. Figure 8 shows why accepted positive parameters must be assessed together with error and valid coverage.

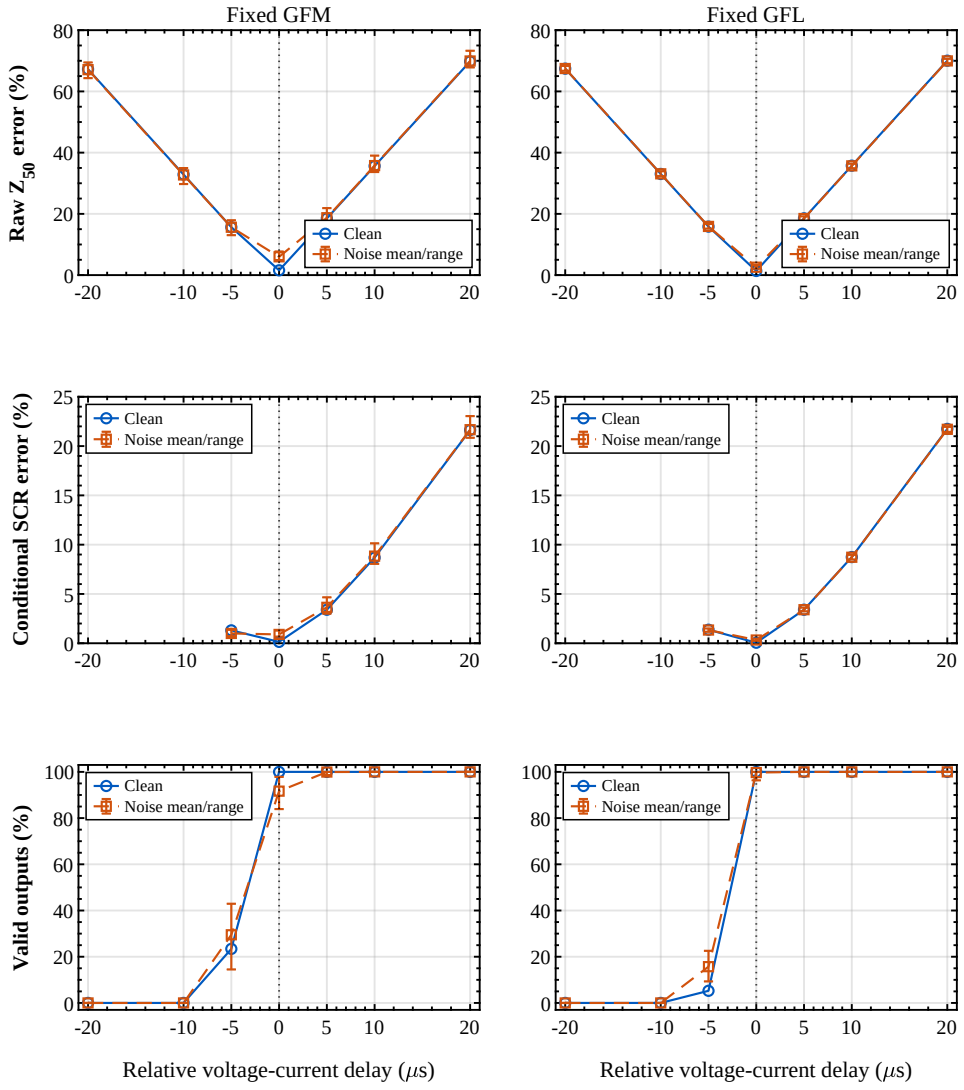


Figure 8. Relativechannel delay sensitivity on the two nominal step trajectories at unit gain. The display focuses on ±20 µs and includes the new ±5 µs settings; the full ±100 µs range and all gain combinations remain in the data archive. Positive delay means voltage lags current. The (**Top**) panels retain all finite reconstructed impedance errors, including nonphysical estimates; the (**middle**) panels report SCR error only on accepted outputs, with gaps where no output is accepted; finally, the (**Bottom**) panels disclose valid coverage. Noise bars show the range of per-record means across 20 paired seeds, not confidence or prediction bounds.

At unit gain and +5 µs, both clean modes retain 100% accepted outputs and about 3.40% mean SCR error, but mean Z_{50} errors are 18.51/18.54%. At +20 µs, SCR errors rise to 21.63/21.74%; at −20 µs, negative resistance leaves no accepted outputs. A matched 100-µs common delay instead retains approximately 0.140/0.053% mean SCR error. Ideal zero-residual 5% complex impedance delay regions at unit gain are only about ±1.46 µs for 2/4 mH; the raw-log integer delay tests do not resolve or calibrate those regions.

Thirty-six fixed-mode electrical runs apply actual source backgrounds, injection amplitude changes, and shunt RC networks. Six non-ideal automatic sequences separately test gain ±1%, relative delay ±20 µs, and 0.5% coherent backgrounds at 0/180°. The source fixture passes nominal waveform/SCR equivalence checks. Table 6 summarizes observed boundaries; full phase settings, network responses, posterior residual audits, and spectra are provided in Supplementary Section S6.

Table 6. Non-ideal results and their interpretation. Paired values denote GFM/GFL; detailed cases and failed outputs are in the Supplementary Materials.

Condition	Observed Result	Interpretation
525-Hz source background, 0.5%, 90°	Raw mean Z_{50} error 323.91/123.62%; no accepted steady outputs.	Coherent background is not rejected; three tested phases do not cover all phases.
RC shunt, 2-Ω damping; 475/525/575-Hz design points	Injection-on raw Z_{525} error 0.55–4.00%; RL-reconstructed Z_{50} error 2551.70–6599.10%.	Accurate injection frequency identification cannot validate the RL extrapolation.
Default 10-V injection command versus off	PCC 525-Hz ratios 1.52/3.94% versus 0.028/0.025%; voltage THD 2.03/2.68% versus 2.29/4.35%.	Command amplitude is not a fixed PCC percentage; harmonic THD excludes the interharmonic.
Six non-ideal automatic sequences	Only the two ±1% gain cases complete both transfers. Neither ±20 µs delay nor 0.5% background at 0/180° executes.	Validity and guard logic do not establish reliable estimation or a complete transfer sequence.
Recorded residual envelope audit	28 injection-on cases pass a posterior denominator/bound check; eight injection-off controls fail the denominator.	Record-specific consistency is not an a priori calibrated error bound.

The common-delay control and relative-delay failures distinguish transport latency from voltage–current phase rotation. The electrical tests separately expose background contamination and single-frequency RL extrapolation error. Together with the nominal results, they delimit the demonstrated chain: a suitable frequency-spanning network model, justified channel matching, and adequate response strength are required. The numerical validity screen and 5%/80-ms selector do not certify these conditions online. Record-specific posterior bounds provide consistency checks; harmonic THD and the injection frequency component remain separate power quality measures.

5. Prototype Experimental Results

5.1. Prototype and Evidence Scope

The laboratory platform in Figure 9 comprises a three-phase two-level converter, an LC filter, programmable dc supply, ITECH IT7900 grid simulator, sensors, and oscilloscopes. A Texas Instruments TMS320F28379D controlCARD operates at 10 kHz. The rated line voltage/power are 121 V RMS/1.2 kW, with a 300-V dc link, 50-Hz grid, 3-mH/100-µF

filter, and 3.3-Ω damping. These differ from the 380-V/68-kW simulation, and do not establish dynamic scaling equivalence.

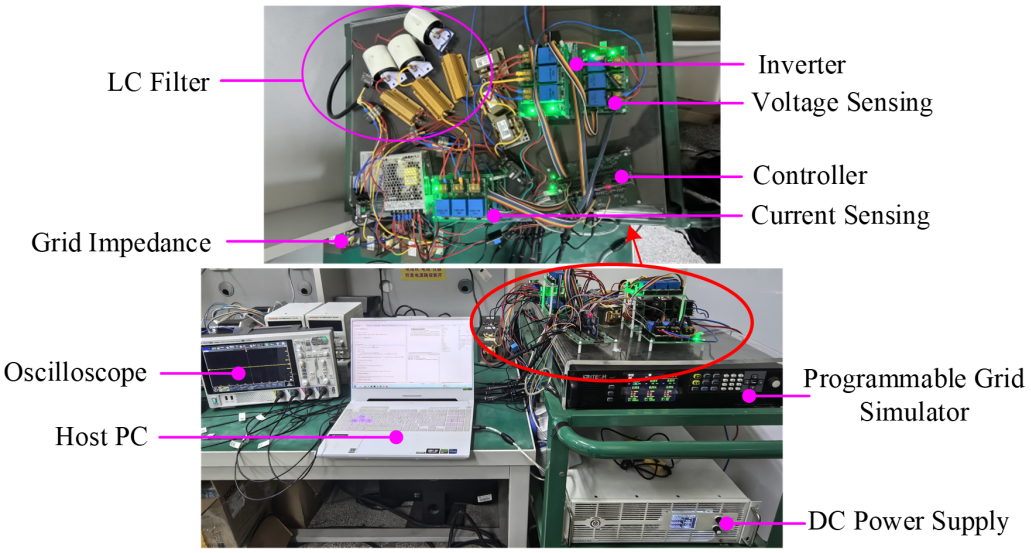


Figure 9. Laboratory prototype of the three-phase grid-connected converter.

The archived records below provide qualitative laboratory illustrations of impedance tracking and bidirectional transfer. The accuracy, timing, and comparative transient metrics reported in Section 4 are simulation results, not calibrated prototype measurements. The laboratory impedance tests use a nominal 525 Hz injection setting of 2% of rated voltage.

5.2. Qualitative Estimation and Transfer Records

Figure 10 shows the recorded response to a programmed grid-inductance change from 20 to 0 mH; zero programmed inductance does not mean zero total grid impedance. The displayed estimates qualitatively track the change.

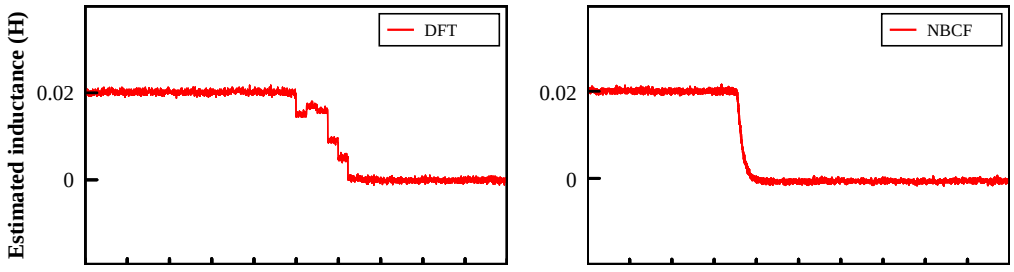
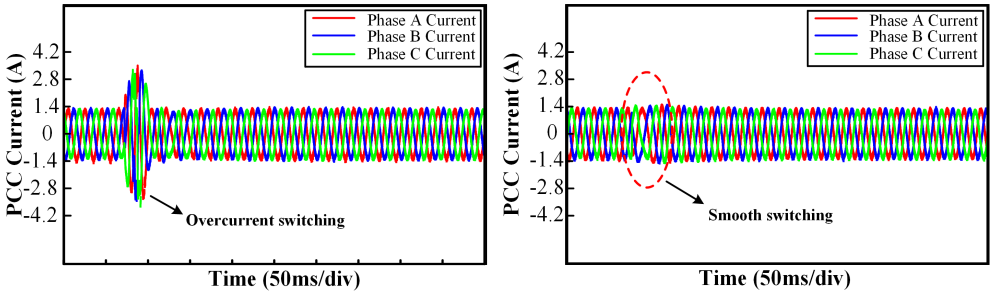


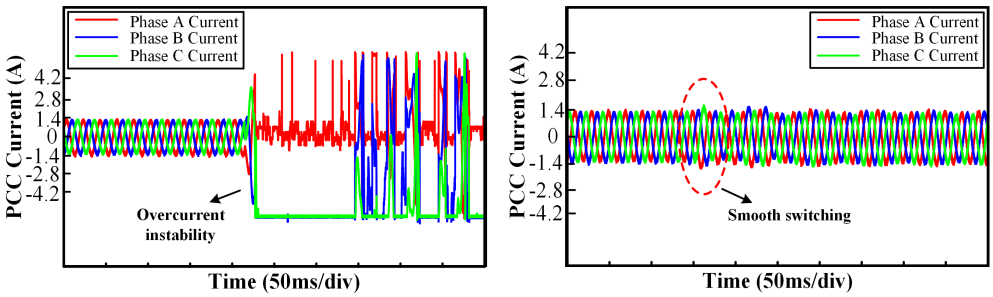
Figure 10. Experimental response to a programmed change in grid impedance. Archived traces retained for qualitative assessment; no common-criterion response time is assigned.

Figures 11 and 12 retain the bidirectional transfer records. Initial GFM operating power is 300 W, distinct from the 1.2-kW rating. With 121 V line RMS and 20 mH, neglecting resistance gives nominal SCR $\simeq$ 1.94, consistent with initial GFM operation but not a measured selector input. The displayed direct-transfer traces show larger visible excursions; this qualitative comparison does not isolate transfer strategy from operating-reference changes.



(a) Conventional switching (b) Proposed switching

Figure 11. Experimental GFM-to-GFL transfer under two switching strategies. Archived waveforms shown for qualitative comparison.



(a) Conventional switching (b) Proposed switching

Figure 12. Experimental GFL-to-GFM transfer under two switching strategies. Archived waveforms shown for qualitative comparison.

The exports do not establish calibrated channel conversions, synchronized references/event flags, or historical extraction settings. Consequently, no comparable hardware accuracy, identification time, peak, tracking integral, voltage deviation, recovery, or THD is assigned. Furthermore, the records do not verify automatic SCR triggering, multi-SCR/P/Q coverage, independent repetitions, or same-condition injection-on/off spectra. Quantitative comparisons in Section 4 are numerical evidence. Supplementary Section S7 summarizes the supported interpretation of these records.

The present validation concerns the reported single-converter configurations and operating conditions. Extension to other converter ratings requires reassessment of the voltage and rated-power bases, filter parameters, controller tuning, and digital delays; equal SCR values alone do not establish equivalent dynamic behavior. Application to multiple-converter systems requires evaluation of control interactions and possible interference between impedance identification signals. For grids with resonant or other frequency-dependent impedances, a single series-*RL* equivalent may not adequately represent both the injection and fundamental frequencies. In such cases, reconstruction of the fundamental-frequency impedance requires an appropriate network model or its separate identification. These extensions have not been validated in the present study.

6. Conclusions

This article developed a grid state-aware adaptive grid-following/grid-forming switching strategy that connects online impedance estimation, fundamental-frequency short-circuit ratio reconstruction and bidirectional controller state preparation. The method coordinates notch–band-pass extraction, hysteretic selection, synchronization and state initialization within a reproducible estimation–decision–handover chain. Conditional error

analysis, explicit state assignments, and common-frame command consistency conditions connect its estimation and transfer stages.

Across 86 matched-channel fixed-mode simulation configurations, the maximum final-interval short-circuit ratio error was 2.32%. Shared-input settling was comparable to the adapted mature estimator. The coordinated chain completed nominal and unbalanced automatic sequences. In the scheduled 40 kW grid-following to grid-forming case, converter window peak and phase-RMS voltage deviation were 89.97 A and 1.33%, versus 100.28 A and 3.18% for the Gao-inspired adaptation; benefits remained direction-dependent. These quantitative results are numerical; archived prototype waveforms provide qualitative estimation and transfer evidence.

Further work should extend calibrated hardware validation across grid strengths and operating points, should also and assess frequency-dependent networks and interacting converters.

Supplementary Materials: The following supporting information can be downloaded at https://www.mdpi.com/article/10.3390/pr14213552/s1, Supplementary file: Detailed filter and error derivations; synchronization and state analysis; complete estimator comparisons; parameter and margin scans; complete transfer comparisons and sensitivity; non-ideal network and injection results; interpretation of prototype records.

Author Contributions: Conceptualization, Y.C. and W.D.; methodology, W.D.; validation, T.G.; formal analysis, T.G. and J.L.; writing—original draft preparation, Y.C.; writing—review and editing, J.L. and W.W.; supervision, W.W. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: Authors Yonghua Chen, Wei Du, and Tian Gao were employed by the Nari Technology Co., Ltd. and State Grid Electric Power Research Institute (NARI Group Corporation). The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest. The Nari Technology Co., Ltd. and State Grid Electric Power Research Institute (NARI Group Corporation) had no role in the design of the study, in the collection, analysis, or interpretation of data, in the writing of the manuscript, or in the decision to publish the results.

Abbreviations

The following abbreviations are used in this manuscript:

DFT	Discrete Fourier Transform
DSP	Digital Signal Processor
IAE	Integral Absolute Error
MCCF	Multiple Complex-Coefficient Filter
PI	Proportional–Integral
PWM	Pulse Width Modulation
RDFT	Recursive Discrete Fourier Transform
RMS	Root Mean Square

THD	Total Harmonic Distortion
VFF-RLS	Variable Forgetting Factor Recursive Least Squares
VSC	Voltage Source Converter
VSG	Virtual Synchronous Generator
GFL	Grid-Following
GFM	Grid-Forming
NBCF	Notch–Bandpass Compound Filter
PCC	Point of Common Coupling
PLL	Phase-Locked Loop
SCR	Short-Circuit Ratio

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