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Hierarchical Control System for a Multi-Port, Bidirectional MMC-Based EV Charging Station: A Model-in-the-Loop Validation

Tomas Ravet [1], Cristobal Rodriguez [1], Matias Diaz [1,*], Daniel Velasquez [1], Roberto Cárdenas [2] and Pat Wheeler [3,4]

[1] Electrical Engineering Department, Universidad de Santiago de Chile, Santiago 9170020, Chile; tomas.ravet@usach.cl (T.R.); cristobal.rodriguez.c@usach.cl (C.R.); daniel.velasquez.v@usach.cl (D.V.)
[2] Electrical Engineering Department, University of Chile, Santiago 9170020, Chile; jesus.cardenas@uchile.cl
[3] School of Electrical and Electronic Engineering, University of Nottingham, Nottingham NG7 2RD, UK; pat.wheeler@nottingham.ac.uk
[4] Centro de Transformación Energética, Universidad Andrés Bello, Santiago 7501015, Chile
* Correspondence: matias.diazd@usach.cl

Abstract

The increasing demand for high-power electric vehicle charging systems with Vehicle-to-Grid (V2G) capability highlights the need for modular, scalable power converters. This paper proposes a hierarchical control strategy for a high-power, multi-port electric vehicle charging station. The system, based on a Series-Parallel Modular Multilevel Converter (SP-MMC) with isolated modules, is managed by a coordinated control strategy that integrates proportional-integral-resonant regulators, nearest-level control with voltage sorting, and single-phase-shifted modulation. The proposed system enables simultaneous, independent regulation of multiple bidirectional, isolated direct current ports while maintaining grid-side power quality and internal variables of the SP-MMC. The proposed control is validated using real-time Model-In-the-Loop (MIL) simulations that include sequential port activation, bidirectional power flow, and charging operation. MIL results demonstrate stable operation with controlled DC-link voltage ripple, accurate per-port current tracking, and near-unity grid power factor under multi-port operation.

Keywords: multi-port charger; Modular Multilevel Converter; hierarchical control; SP-MMC; V2G integration; isolated DC-DC converter; model-in-the-loop

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1. Introduction

The global transition to electromobility is a key element in decarbonization efforts worldwide. This transition has been highlighted by the rapid increase in sales of electric vehicles (EVs), which reached 40 million units by 2023 [1]. As a result, there is a growing need for a reliable charging network that can provide high power quickly and efficiently. Fast charging is essential for the widespread adoption of EVs, as it helps alleviate consumer concerns about long charging times and range anxiety. Moreover, as battery technology continues to advance and average capacities are expected to reach 100 kWh by 2030, the demand for fast and ultra-fast charging infrastructure will continue to rise.

Conventional fast chargers typically rely on multi-stage architectures, such as an Active Front End rectifier followed by an isolated Direct Current (DC) to DC converter [2]. While effective, these designs can be complex and face limitations in modularity and

scalability. As an alternative, Modular Multilevel Converters (MMCs) have emerged as a relatively new technology for high-power EV charging applications.

Modular Multilevel Converters (MMCs), originally developed for high-voltage direct current (HVDC) transmission [3,4], have recently been adapted for medium-voltage and high-power applications. Novel topologies, such as the Modular Multilevel Matrix Converter [5] and the Hexverter [6], demonstrate the versatility of the MMC concept for various applications [7,8]. MMCs are well recognized for their inherent fault tolerance and robust fault-ride-through capability. MMC clusters are composed of series-connected half-bridge or full-bridge submodules, which provide distributed energy storage through the Cluster Capacitor Voltage (CCV). The CCVs are defined as the sum of the individual capacitor voltages within a cluster and allow for the converter to accommodate unbalanced operating conditions and transient overvoltages [5,9].

Furthermore, in the event of a submodule or semiconductor failure, the affected unit can be bypassed, allowing for the converter to continue operating with reduced capacity but without loss of functionality [10]. As a result, MMCs have consistently demonstrated strong ride-through performance under grid faults, maintaining controllability and operational continuity during voltage sags and asymmetric fault conditions [11].

In the context of electromobility, recent studies have explored MMCs due to their inherent modularity, scalability, high efficiency, and superior output power quality, making them promising candidates for next-generation charging infrastructure [12]. Nevertheless, existing MMC-based multi-port charger designs often face limitations regarding the number of independently controlled charging outputs [13]. Most implementations use the power cells to provide galvanic isolation, which can cause power imbalance and restrict the number of unidirectional charging ports [14].

The initial concept of the Series-Parallel Modular Multilevel Converter (SP-MMC) was introduced as a multi-port architecture [15]. Early implementations used a single High-Frequency (HF) transformer to couple the parallel stages. This single-transformer arrangement restricts scalability and limits independent port regulation due to inherent magnetic coupling. In addition, all charging ports remain magnetically coupled, preventing independent regulation and fault isolation.

The topology presented in this paper resolves this constraint by adopting a modular DC-DC stage with per-port isolation. As shown in Figure 1, the SP-MMC is composed of a Series-MMC, a DC link, and parallel DC modules. Every parallel module features an HF transformer and a Back-to-Back (B2B) Full-Bridge (FB) cell, offering galvanic isolation to enable multi-port scalability.

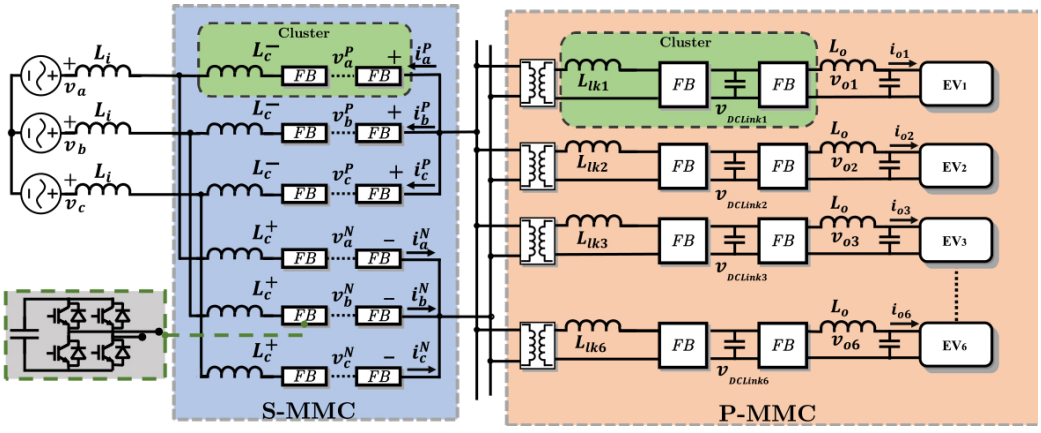


Figure 1. SP-MMC topology.

The architecture presented in this work is a variation of a Solid-State Transformer (SST), a core technology enabling isolated medium-voltage charging. To situate this contribution, it is necessary to compare it with recent SST topologies. Several existing designs concentrate on optimizing individual components, such as the magnetic elements or overall efficiency, or are limited to single-port operation. Architectures based on multi-winding high-frequency transformers introduce control complexity and increased fault propagation. Designs using per-cell Dual Active Bridges (DABs) face challenges related to balancing and modularity.

This work adopts a different approach based on port-level modularity using per-port HF-isolated DAB stages. Recent developments, such as the modular DAB converter in [16], achieve module-level high-voltage isolation and scale charging power by replicating single-output DC–DC modules. In contrast, the proposed SP-MMC targets a scalable multi-port architecture capable of simultaneously regulating multiple HF-isolated, bidirectional ports (demonstrated with six ports) by extending the parallel stage with additional isolated modules. To make this distinction explicit in terms of port scalability and the associated coordination/communication requirements, Table 1 provides a unified comparison of representative isolated charger or SST converter families.

Table 1. Benchmarking of SST converters.

Topology	Stages	HF Isolation Implementation	Modularity/Scaling Target	No. V2G Ports	Wide-Range Mechanism/Coordination Overhead
HF-Link SST [17–19]	3 (AC-DC, DC-DC, DC-AC)	Single HF-link (typically one DAB)	System-level; power scaling via larger/stacked modules	1 (or 4, dependent)	No dedicated multi-port scaling; overhead: Low
MMC with Cell-DAB [18,20]	2 (AC-DC, DC-DC)	Per-cell isolation (cell-level DABs)	Cell-level modularity; balancing-driven integration complexity	1	Balancing + many cell-level DAB loops; overhead: High
Multi-winding SST [19,21]	3	Multi-winding HF transformer (coupled ports)	Port-level via windings; limited by magnetic coupling/fault propagation	4	Port coupling increases control effort; overhead: High
Modular DAB [16]	1 (isolated DC-DC module)	Dual-secondary transformer; S-mode/P-mode output reconfiguration	Module-level; power scaling by paralleling modules (charging pole)	1 (per module)	Wide range via output series/parallel reconfiguration (S/P mode) + one main setpoint; overhead: Low
This Work (SP-MMC)	2 (S-MMC, P-MMC)	Per-port HF isolation (one DAB per port)	Port-level; port scaling by adding isolated parallel modules	n; demonstrate up to 6 (this work)	Multi-port coordination (one setpoint and one phase-shift per port) + shared MMC capacitor-energy balancing; overhead: High

Conversely, this paper proposes a hierarchical control strategy for the SP-MMC multi-port charger. The approach follows the general structure of classical multi-loop control. However, the resulting control problem differs from a standard power–voltage (e.g., $PQ - V_{dc}$) implementation. Instead, multiple HF-isolated bidirectional ports must be coordinated while enforcing capacitor-energy balancing in the SP-MMC under time-varying and asymmetric port demands. This requirement motivates the need for an explicit coordination layer. This layer dispatches port setpoints subject to shared energy balancing

constraints, improves port-to-port decoupling, and enables selective port blocking while preserving the operation of the remaining ports under time-varying and asymmetric port demands. This introduces an explicit coordination layer that dispatches port setpoints under shared balancing constraints, thereby strengthening port-to-port decoupling and enabling selective port blocking while maintaining the operation of the remaining ports.

The proposed system is validated using a Model-in-the-Loop (MIL) simulation executed in real time. The MIL setup includes the power stage, the control architecture, and a battery model. The converter is implemented as a 42-cell SP-MMC, composed of a 30-cell Series-MMC connected to the grid and a 12-cell Parallel-MMC stage supplying six isolated and independently regulated DC outputs. The simulation is executed using a PLECS RT Box 3 platform. Each output port is connected to a virtual battery bank model that emulates EV packs with different voltage levels. Simulation results confirm stable operation under bidirectional power flow and validate the proposed architecture for multi-port fast charging applications.

The main contributions of this work are as follows:

- A hierarchical control strategy is developed that combines PI and PR controllers, SPS modulation for DAB regulation, NLC with voltage sorting for capacitor voltage balancing in the S-MMC, and the systems-level integration for six simultaneous, bidirectional ports.
- Demonstration of simultaneous, decoupled control of six ports under dynamic charging and V2G scenarios using a real-time MIL simulation of a 42-cell SP-MMC with six independently controlled DC ports.

The structure of this paper is as follows. Section 2 details the proposed converter topology and its mathematical modeling. Section 3 describes the hierarchical control strategy for the series and parallel stages. Section 4 presents the MIL simulation results and performance evaluation. Section 5 summarizes the main conclusions of the study.

2. Proposed SP-MMC

Figure 1 shows the proposed EV charger based on the SP-MMC. This converter is composed of two stages: the Series-MMC (S-MMC) and the Parallel-MMC (P-MMC). On the one hand, the S-MMC consists of six clusters that connect the three phases of the electrical network to a high-frequency transformer. Each cluster comprises a series connection of an inductor and FB power cells. The S-MMC generates low-voltage (LV) and HF outputs, connected to the parallel HF transformers. On the other hand, the P-MMC offers multiple DC charging ports by connecting B2B-FB cells. The first FB converts the Alternating Current (AC) signal from HF to DC by regulating the voltage of the floating capacitor, whereas the second FB regulates the output current. As a result, the floating capacitor in each P-MMC cluster has some degree of freedom, enabling it to adapt to various voltage levels.

2.1. S-MMC Modeling

MMCs are usually represented by voltage-current and voltage-power models. The work by [22,23] presents an overview of the modeling strategies used in AC-AC MMC. Consequently, the following subsections present the model applied to the S-MMC, based on [24,25], and using the $\Sigma\Delta\alpha\beta 0$ transformation to decouple the electrical variables of the input, output, and S-MMC. This transformation is constructed from orthogonal vectors, which guarantees the decoupling between the sum (Σ) and difference (Δ) subspaces. As a result, the dynamics related to capacitor-energy balancing and those associated with grid-side power exchange can be treated separately.

2.1.1. S-MMC Voltage-Current Model

Each cluster of the S-MMC can be considered a controlled voltage source; thus, the following expression is derived:

$$L_c \frac{d}{dt} \underbrace{\begin{pmatrix} i_a^P & i_b^P & i_c^P \\ i_a^N & i_b^N & i_c^N \end{pmatrix}}_{\boldsymbol{I_{abc}^{PN}}} = \frac{v_0}{2} \begin{pmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \end{pmatrix} - \underbrace{\begin{pmatrix} v_a^P & v_b^P & v_c^P \\ v_a^N & v_b^N & v_c^N \end{pmatrix}}_{\boldsymbol{V_{abc}^{PN}}} - \begin{pmatrix} v_a & v_b & v_c \\ -v_a & -v_b & -v_c \end{pmatrix}. \tag{1}$$

The dynamics of the input and output ports are decoupled by applying $\Sigma\Delta\alpha\beta 0$ to (1). The transform $\Sigma\Delta\alpha\beta 0$ is used to transform a generic matrix $\boldsymbol{X_{abc}^{PN}}$ into a decoupled matrix $\boldsymbol{X_{\alpha\beta 0}^{\Sigma\Delta}}$ as follows:

$$\boldsymbol{X_{\alpha\beta 0}^{\Sigma\Delta}} = \boldsymbol{C^{\Sigma\Delta}} \cdot \boldsymbol{X_{abc}^{PN}} \cdot \boldsymbol{C_{\alpha\beta 0}^{T}}. \tag{2}$$

where the transforms $\boldsymbol{C^{\Sigma\Delta}}$ and $\boldsymbol{C_{\alpha\beta 0}}$ are defined below:

$$\boldsymbol{C^{\Sigma\Delta}} = \begin{pmatrix} \frac{1}{2} & \frac{1}{2} \\ 1 & -1 \end{pmatrix}. \tag{3}$$

$$\boldsymbol{C_{\alpha\beta 0}} = \begin{pmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{pmatrix}. \tag{4}$$

Equation (5) results from applying the $\Sigma\Delta\alpha\beta 0$ transform to (1).

$$L \frac{d}{dt} \underbrace{\begin{pmatrix} i_\alpha^\Sigma & i_\beta^\Sigma & \frac{i_0}{3} \\ i_\alpha & i_\beta & 0 \end{pmatrix}}_{\boldsymbol{I_{\alpha\beta 0}^{\Sigma\Delta}}} = - \underbrace{\begin{pmatrix} v_\alpha^\Sigma & v_\beta^\Sigma & v_0^\Sigma \\ v_\alpha^\Delta & v_\beta^\Delta & v_0^\Delta \end{pmatrix}}_{\boldsymbol{V_{\alpha\beta 0}^{\Sigma\Delta}}} - 2 \begin{pmatrix} 0 & 0 & \frac{-v_0}{4} \\ v_\alpha & v_\beta & v_0 \end{pmatrix}. \tag{5}$$

where i_α^Σ and i_β^Σ represent circulating currents that regulate currents for each port independently. Using (5), it is simpler to propose and analyze an appropriate control system to independently regulate each current.

2.1.2. S-MMC Voltage-Power Model

The voltage in each capacitor is floating, and their regulation is the main control challenge in MMCs. Usually, a voltage-energy and voltage-power relationship is derived to regulate the CCVs. For a generic cluster xy, the following relationships are given by

$$W^{PN} = \frac{1}{2} C \sum_{i=1}^{n} v_{c_i}^{PN^2} \tag{6}$$

$$\Delta W^{xy} = C \bar{v}_C \Delta v_c^{PN} \tag{7}$$

$$\Delta P^{PN} \approx C \bar{v}_C \frac{d\Delta v_c^{PN}}{dt} \tag{8}$$

where W^{PN} and v_C^{PN} are the energy and CCV in the cluster PN, $\bar{v}_C$ is the average voltage in the cluster. Additionally, the CCV is calculated as $v_C^{PN} = v_{C_1}^{PN} + ... + v_{C_n}^{PN}$ for a cluster with n cells. Applying this voltage–power relationship to the six clusters yields

$$\underbrace{\begin{pmatrix} v_{C_a}^P & v_{C_b}^P & v_{C_c}^P \\ v_{C_a}^N & v_{C_b}^N & v_{C_c}^N \end{pmatrix}}_{\boldsymbol{V_{Cabc}^{PN}}} \approx \frac{1}{C\bar{v}_C} \int \underbrace{\begin{pmatrix} p_a^P & p_b^P & p_c^P \\ p_a^N & p_b^N & p_c^N \end{pmatrix}}_{\boldsymbol{P_{abc}^{PN}}} dt + n\bar{v}_C \begin{pmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \end{pmatrix}. \tag{9}$$

The elements of $\boldsymbol{P_{abc}^{PN}}$ are calculated by multiplying the voltage and current of each cluster (e.g., $p_a^P = v_a^P i_a^P$), and $\boldsymbol{V_{Cabc}^{PN}}$ represents the CCV. As proposed in [25], the $\Sigma\Delta\alpha\beta0$ is applied to (9) to obtain a decoupled representation of the average and ripple components of the CCVs:

$$\underbrace{\begin{pmatrix} v_{C_\alpha}^{\Sigma} & v_{C_\beta}^{\Sigma} & v_{C_0}^{\Sigma} \\ v_{C_\alpha}^{\Delta} & v_{C_\beta}^{\Delta} & v_{C_0}^{\Delta} \end{pmatrix}}_{\boldsymbol{V_{C\alpha\beta0}^{\Sigma\Delta}}} \approx \frac{1}{C\bar{v}_C} \int \underbrace{\begin{pmatrix} p_\alpha^{\Sigma} & p_\beta^{\Sigma} & p_0^{\Sigma} \\ p_\alpha^{\Delta} & p_\beta^{\Delta} & p_0^{\Delta} \end{pmatrix}}_{\boldsymbol{P_{\alpha\beta0}^{\Sigma\Delta}}} dt + \begin{pmatrix} 0 & 0 & n\bar{v}_C \\ 0 & 0 & 0 \end{pmatrix}. \tag{10}$$

The relation of (10) represents the Power-CCV model of the S-MMC in $\Sigma\Delta\alpha\beta0$ coordinates. The voltage terms of the left side of (10) have the following physical meaning and control modes:

- The voltage terms $v_{C_\alpha}^{\Sigma}$, $v_{C_\beta}^{\Sigma}$,$v_{C_\alpha}^{\Delta}$, and $v_{C_\beta}^{\Delta}$ represent CCV imbalances in the clusters and can be controlled using negative sequence of the input frequency in $i_{\alpha\beta}$ and $i_{\alpha\beta}^{\Sigma}$.
- The voltage terms $v_{C_0}^{\Delta}$ represents CCV imbalances in the clusters and can be controlled using positive sequence of the input frequency in $i_{\alpha\beta}^{\Sigma}$.
- The voltage terms $v_{C_0}^{\Sigma}$ represents the average voltage of the CCV and can be controlled using positive sequence of the input frequency in $i_{\alpha\beta}$.

Furthermore, the circulating current can be manipulated to control the total capacitor voltages in the $\Sigma\Delta\alpha\beta0$ coordinates.

2.2. P-MMC Modeling

The P-MMC consists of parallel-connected B2B FB modules. Each module operates as an independent, isolated charging port, converting the high-frequency AC voltage from the S-MMC link into a regulated DC output acting like a power transfer stage operating in HF.

2.2.1. HF Power Transfer Model

The mechanism for power transfer relies on the phase-shift principle typical of a DAB [26,27]. Essentially, power flow can be likened to the exchange between two voltage sources linked by a choke [28], and it is influenced by the phase angle (φ) between these two voltages, as illustrated in Figure 2. Hence, bidirectional (V2G) operation can be controlled if one voltage source is out of phase with the other, as the power flow depends on both the sign and magnitude of the phase angle [29,30].

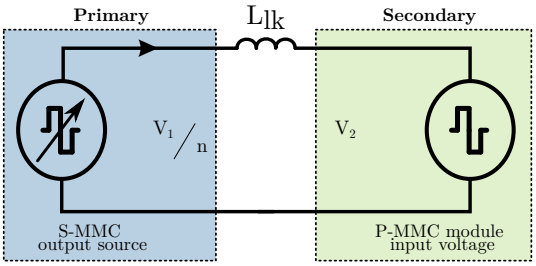


Figure 2. Equivalent circuit model for AC-DC power transference.

The S-MMC generates a high-frequency square wave voltage at the primary of the HF transformer, while the P-MMC synthesizes a phase-shifted square wave at the secondary. The phase-shift between the primary and secondary defines the current through the leakage inductance (L_{lk}):

$$p(t) = v_1(t) \cdot i_{lk}(t) \tag{11}$$

Using:

$$v_1(t) = V_1 \sum_{k=1,3,5,\ldots}^{\infty} \left(\frac{4}{k\pi}\right) \sin(k\pi D_1) \cos(k\omega t) \tag{12}$$

$$i_{lk}(t) = \frac{1}{L_{lk}} \int \left(v_1(t) - v_2(t)\right) dt \tag{13}$$

$$= \frac{4}{\pi\, \omega\, L_{lk}} \sum_{k=1,3,5,\ldots}^{\infty} \frac{1}{k^2} \left[V_1 \sin(k\pi D_1) \sin(k\omega t) - V_2 \sin(k\pi D_2) \sin(k\omega t + k\varphi)\right] \tag{14}$$

$$v_2(t) = V_2 \sum_{k=1,3,5,\ldots}^{\infty} \left(\frac{4}{k\pi}\right) \sin(k\pi D_2) \cos(k\omega t + k\varphi) \tag{15}$$

where V_1 and V_2 are the primary and secondary voltages, D_1 and D_2 are the duty cycles of each FB, φ is the phase-shift between both FBs, and f_{sw} is the switching frequency in $\omega = 2\pi f_{sw}$.

Then, the average HF power can be defined as follows:

$$\overline{P} = \frac{8\, V_1 V_2}{\pi^2\, \omega\, L_{lk}} \sum_{k=1,3,5,\ldots}^{\infty} \frac{1}{k^3} \sin(k\pi D_1) \sin(k\pi D_2) \sin(k\varphi) \tag{16}$$

The higher-order harmonics in (16) can be neglected, as indicated in [31,32], and the power is simplified to

$$\overline{P} = \frac{8 V_1 V_2}{\pi^2 \omega L_{lk}} \cdot sin(\varphi) \tag{17}$$

Equation (17) is a control-oriented simplification of (16) that adopts the fundamental approximation under an operating envelope with bounded phase shift and duty ratios close to 0.5, where the fundamental term dominates.

Magnetic components are a critical part of HF-link converters and impose practical constraints on performance and operating range, for instance, leakage dispersion, ZVS boundaries, core saturation, and thermal limits. These non-idealities can reduce the admissible phase-shift range and introduce gain variations in the HF power stage, affecting HF-link power dynamics and, consequently, DC-link regulation.

In this work, the MIL model assumes ideal magnetic components in order to isolate and validate the proposed control architecture and system-level integration. Accordingly, the leakage inductance is selected to provide a sufficiently wide operating margin so that the DAB power-transfer capability does not limit the control study [30]. Although practical hardware implementation activities would necessitate a dedicated stage for magnetics co-design and optimization, like in [27], these hardware-focused design tasks lie beyond the scope of this paper.

2.2.2. FB-Buck Model

EV charging is characterized by time intervals during which it operates at a constant current and voltage. Consequently, a dynamic model is needed to regulate these variables. Equations (18) and (19) refer to the dynamical model of the P-MMC.

$$v_{out} = L_{out} \frac{di_{out}}{dt}. \tag{18}$$

$$i_{out} = C_{out} \frac{dv_{out}}{dt}. \tag{19}$$

The proposed control strategy aims to regulate the output voltage and current of the P-MMC using Equations (18) and (19).

3. Proposed Control Strategy

The proposed control strategy for the SP-MMC coordinates the operation of the S-MMC and P-MMC stages to achieve the following key objectives: (i) regulation and balancing of the cluster capacitor voltages in the S-MMC, (ii) control of the high-frequency link voltage to manage power transfer between stages, and (iii) independent regulation of the output voltages and currents for multi-port EV battery charging [33]. Figure 3 presents an overview of the proposed control architecture, which is organized into three subsystems:

- S-MMC voltage–current control: Responsible for regulating the output voltage applied to the transformer primary and balancing the capacitor voltages of each cluster [34,35].
- HF power transfer control: Regulates power exchange between the S-MMC and the P-MMC by adjusting the phase shift between the primary and secondary voltages of the transformer [36–38].
- P-MMC voltage–current control: Manages the DC-link capacitor voltages and regulates the output voltage and current of each load port.

In addition to these control loops, specific modulation strategies are implemented at each stage. The S-MMC employs NLC, selected for its suitability for high-frequency synthesis without requiring high switching rates [39]. The P-MMC employs Pulse Width Modulation (PWM) as a simple and effective method to regulate the constant DC output [40].

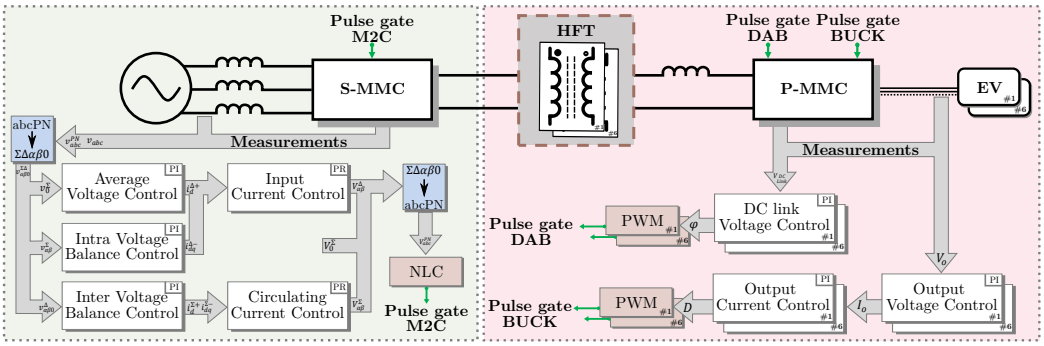


Figure 3. Control strategy for the SP-MMC system.

3.1. S-MMC Voltage–Current Control

The S-MMC control loop (left side in Figure 3) regulates the AC output voltage and balances the capacitor voltages in each cluster with a decoupled frame like [9]. First, the $\Sigma\Delta\alpha\beta0$ transform is applied to the voltages and currents of the cluster. Then, the derivative of the voltages $\boldsymbol{V}_{\boldsymbol{\alpha\beta0}}^{\boldsymbol{\Sigma\Delta}}$ in (10) is calculated using notch filters to obtain the average value of the total voltages of the cluster. The reference value for these components is obtained using the $\Sigma\Delta\alpha\beta0$ transformation, as described in (2), so the average value of the CCV is controlled with $v_{C_0}^{\Sigma}$ and the other terms control the balance, which, in steady-state, keeps the balance operation of the S-MMC, represented as follows:

$$\underbrace{\begin{pmatrix} \bar{v}_{C_\alpha}^{\Sigma *} & \bar{v}_{C_\beta}^{\Sigma *} & \bar{v}_{C_0}^{\Sigma *} \\ \bar{v}_{C_\alpha}^{\Delta *} & \bar{v}_{C_\beta}^{\Delta *} & \bar{v}_{C_0}^{\Delta *} \end{pmatrix}}_{\bar{V}_{C\alpha\beta0}^{\Sigma\Delta *}} = \begin{pmatrix} 0 & 0 & n\bar{v}_C^* \\ 0 & 0 & 0 \end{pmatrix}. \tag{20}$$

A PI controller on the average voltage defines the references for the circulating and input currents in $dq^{\pm}$ coordinates. PR controllers in the $\alpha\beta$ frame then shape these currents

to produce the desired cluster voltage references, as shown in Figure 3 and used in [3,41]. The term $v_0^{\Sigma*}$ is generated as a high-frequency square wave, while $v_0^{\Delta*} = 0$ avoids zero-sequence injection. Finally, the inverse $\Sigma\Delta\alpha\beta 0$ transform and NLC modulation synthesize each switching signal.

In practice, capacitor tolerances, precharge conditions, and load variations cause an initial spread of capacitor voltages and yield nonzero imbalance components around the mean operating point in (20). These deviations are regarded as disturbances and are compensated by the balancing control (using measured capacitor voltages, NLC voltage sorting, and outer average-energy/voltage control), following standard MMC formulations [9]. To further improve robustness against abrupt disturbances, sliding-mode approaches have been proposed as a promising enhancement [42].

3.2. P-MMC DC-Link Voltage Control

The HF link control, shown in Figure 4, uses the S-MMC square-wave output to feed a high-frequency transformer (right side in Figure 3). Power flow between series and parallel stages is adjusted using an SPS method: a PI controller on the parallel-stage DC-link voltage computes the phase shift φ^* between the primary and secondary waveforms. Changing φ^* alters the real power transferred, enabling tight DC-Link regulation during charging/discharging.

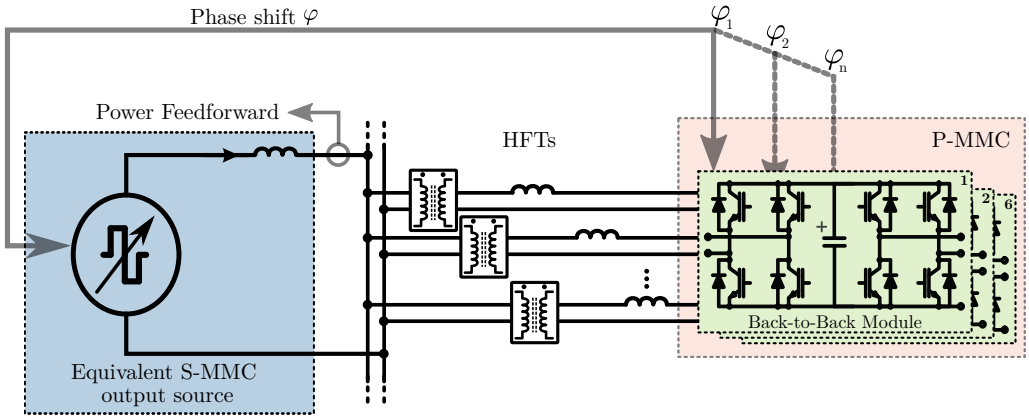


Figure 4. Secondary HF phase shift control of parallel modules with equivalent S-MMC output voltage.

In the parallel stage, FB power cells regulate the DC-Link voltage of each converter. As shown in the right side of Figure 3, PI controllers compare each $V_{\mathrm{DC-Link}}$ with its reference and generate the phase angle φ^* for each module in the SP-MMC link, like in Figure 4 [43]. The resulting voltage references for each FB are synthesized using PWM.

Finally, the P-MMC output stage regulates the DC load ports. A hierarchical PI structure is used: the outer loop controls each output voltage and sets the reference current; the inner loop regulates the output current. Both loops run in dq coordinates, with voltage references transformed back to $\alpha\beta$ for PWM. This ensures stable voltage and current at each DC port under varying load profiles.

By defining the operational parameters and constraining the operating margin, a first-order plant can be achieved without linearizing the previously derived expressions. This strategy allows for more flexible control variables while ensuring accurate reference tracking for each output module. When the system is operated within acceptable limits, precise overall system tracking can be maintained with zero steady-state error. Conversely, surpassing these limits results in increased control challenges and a loss of dynamics.

3.3. P-MMC Output Voltage Control

The nested voltage-current control loop that regulates the DC point of the system with the load parameters is controlled by a buck interleaved topology [40,44]. This FB cell allows for the current stress in each leg to be split, thereby decreasing current ripple [45]. In this way, the point of load is stabilized, enabling bidirectional charging and tracking of load voltage and current depending on the I–V curve required for the charging/discharging.

3.4. Modulation Strategies

The S-MMC employs an NLC strategy to synthesize the reference voltage waveforms. NLC is a modulation method that does not rely on a carrier signal. Instead, it directly selects the closest voltage level that a cluster can synthesize from its available discrete voltage states. This approach results in lower switching frequency and reduced switching losses compared to carrier-based PWM techniques. As shown in Figure 5a, the NLC algorithm determines the output voltage v_{out} as

$$v_{out} = \overline{v}_C \cdot round\left(\frac{v^*}{\overline{v}_C}\right). \tag{21}$$

where v^* is the instantaneous reference voltage, $\overline{v}_C$ is the average voltage of the cluster capacitors, and the round() function selects the nearest integer level. Given that each cluster consists of various FB cells, the number of available levels is 2n + 1. v^*, when decoupled into its low- and high-frequency terms, allows for greater correlation for the NLC algorithm.

A key advantage of NLC is its simplicity and scalability; however, voltage resolution and spectral quality depend on the number of levels. In the proposed system, S-MMC clusters synthesize multilevel voltages that combine a low-frequency component (for grid interaction) and a high-frequency square wave component (to drive the primary transformer), as illustrated in Figure 5b.

To mitigate capacitor voltage imbalance across power cells, the NLC algorithm integrates a cell-sorting strategy based on instantaneous capacitor voltage measurements and the direction of cluster current. Cells with higher voltages are selected when the current direction favors discharge, and vice versa. This method ensures capacitor voltage balancing over time without the need for dedicated circulating current controllers. Figure 5c illustrates the sorting process used for cell selection.

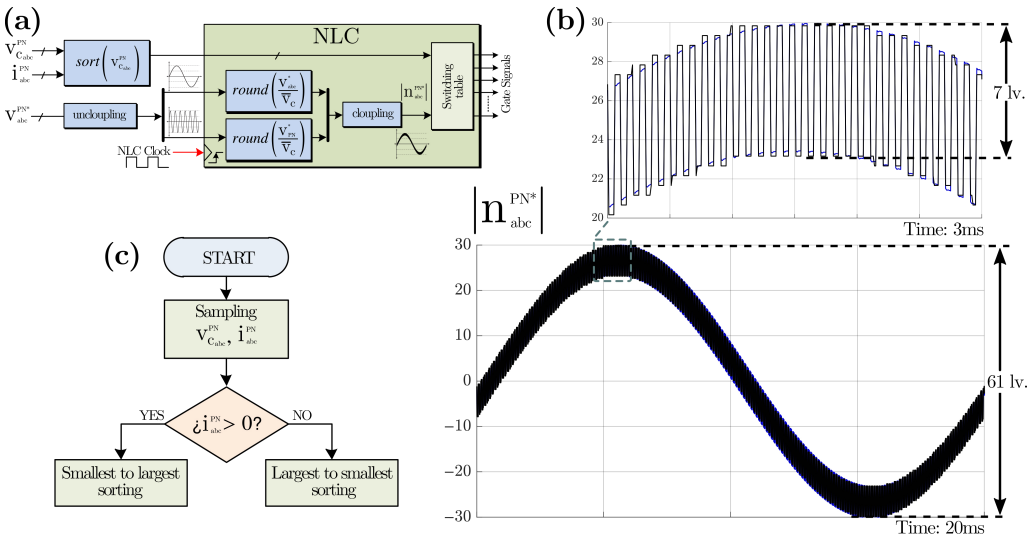


Figure 5. Modulation scheme. (**a**) NLC Algorithm. (**b**) Rounded levels synthesized. (**c**) Bubble sorting.

The P-MMC uses PWM-based modulation techniques for its DAB input and interleaved buck output. On the one hand, the phase shift φ control between the primary and secondary voltages is modulated at 10 kHz to generate the HF signal of the S-MMC. On the other hand, the modulation of the interleaved modules is performed at 40 kHz each, reducing the ripple of the controlled signals for constant voltage and/or current operation by half, depending on the load curve.

3.5. Control Loops Bandwidth Design

A critical aspect of a proposed control system is ensuring stability and preventing undesirable coupling between the multiple nested and parallel control loops. This is achieved by applying a standard bandwidth separation principle. While a detailed gain-tuning analysis is beyond the scope of this paper, the design hierarchy is detailed as follows:

- S-MMC voltage current control: The outer capacitor voltage balancing (Section 3.1), including average, inter, and intra balancing regulation, are tuned to 5 Hz. The inner control loops, including PR regulators, for input–output and circulating currents are designed at 200 Hz. Finally, the NLC and sorting are implemented with an equivalent switching frequency of 10 kHz.
- A frequency of 10 kHz is used in the HF link. The output control regulates the voltage transformer using a bandwidth of 30 Hz.
- P-MMC voltage–current control: The voltage loop provides the reference for the inner current loop and is designed to be slower, using 10 Hz. Additionally, the inner current control is the fastest loop, designed with 200 Hz to quickly track the current reference from the outer voltage loop.

The proposed hierarchy follows a time-scale separation principle to maintain the dynamics decoupled, enabling each nested control loop to be independently regulated without affecting one another. The capacitor-energy dynamics are slow and are therefore regulated with 5–10 Hz bandwidths to avoid interaction with the grid frequency. On the one hand, current controllers are designed at 200 Hz to ensure tracking and decoupling. On the other hand, the HF-link phase-shift control is slower than the switching frequency, but faster than the outer DC-port voltage loops. Finally, the discrete real-time implementation imposes sampling-related limits that prevent overly aggressive tuning. This selection minimizes cross-coupling among nested loops and preserves stability margins under multi-port operation.

4. MIL Results

This section presents the results obtained using a MIL real-time simulation of a SP-MMC charger with six independent DC charging ports. The MIL real-time simulation is implemented on an RT Box 3 platform, as shown in Figure 6.

The electrical plant and the control algorithms are executed on the same PLECS RT Box 3 platform. The plant is simulated using a fixed-step solver with a time step of 10 µs, and the control algorithms are executed with 100 µs for control, ensuring real-time execution. The S-MMC is composed of 60 cells with a voltage rating of 1500 V, while the P-MMC includes 12 cells to facilitate 6 DC charging ports. The proposed charger is designed to function with an input grid of 13.2 kV at 50 Hz. The HF link is regulated to 3.3 kV and 10 kHz, while the DC outputs are controlled at 825 V. The main electrical parameters of the MIL simulation are outlined in Table 2.

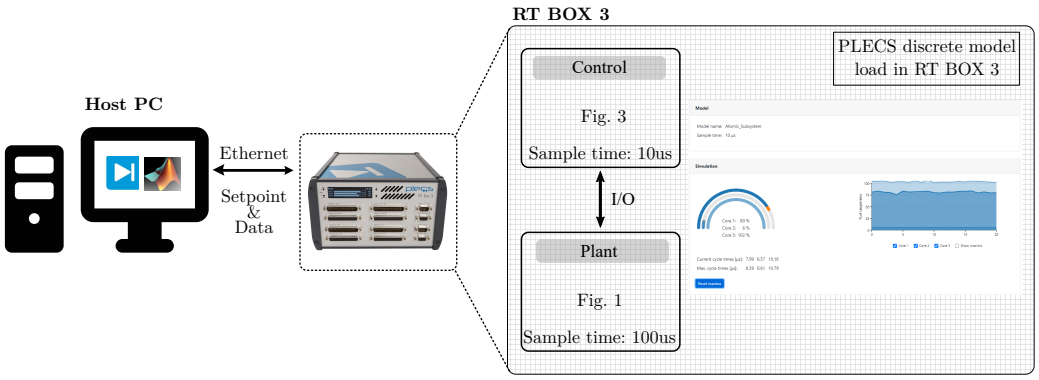


Figure 6. MIL-based implementation of the SP-MMC.

This implementation is developed taking into account the challenges of the control platforms used in this work, such as those indicated in [46].

Table 2. MIL real-time simulation main parameters.

Stage	Parameter	Symbol	Value
Grid	Power	P	1350 kW
	Voltage	V_s	13.2 kV
	Frequency	f_s	50 Hz
Transformer	Primary voltage	V_{prim}	3.3 kV
	Secondary voltage	V_{sec}	0.825 kV
	Frequency	f_{HF}	10 kHz
S-MMC	Cluster inductor	L_c	32.5 µH
	Cell capacitor	C_c	1 mF
	Capacitor voltage	$\bar{v}_C$	1500 V
	Number of cells per cluster	n	10
P-MMC	Input inductor	L_{lk}	3.25 µH
	Cell capacitor DC-Link	$C_{DC-Link}$	3 mF
	Capacitor DC-Link voltage	$\bar{v}_{DC-Link}$	825 V
	Inductor output	L_{out}	2 mH
	Cell capacitor output	V_{out}	220 uF

Three tests are introduced to confirm the correct operation of the SP-MMC and its control strategy: the operation of the S-MMC, the operation of the HF power transfer link, and a dynamic operation test involving multi-port charging and discharging.

4.1. MIL Limitations and Validation Scope

In the MIL framework, magnetic components such as transformers and inductors are represented as ideal linear elements. As a result, hardware-level physical phenomena—including core saturation, hysteresis effects, high-frequency core and eddy-current losses, thermal behavior, and parasitic inter-winding capacitances—are not captured. Consequently, the scope of this validation is limited to the evaluation of control performance, transient stability, and coordinated operation of the hierarchical control system, rather than detailed hardware or magnetic design verification.

The electrical plant and control algorithms are executed in real time on the RT Box 3 platform. The power stage is simulated using a fixed-step solver with a time step of 10 µs, selected to accurately represent the HF-link dynamics while ensuring real-time execution. The control tasks are implemented discretely with a sampling period of 100 µs, consistent with the targeted control bandwidths and the computational capabilities of the RT Box 3.

Due to the discrete-time implementation, the MIL results inherently include sampling and computational delays associated with digital control execution. These delays are considered in the tuning of the hierarchical control loops, whose bandwidths are deliberately selected to remain below the Nyquist frequency imposed by the control sampling rate. While switching-level dead-times and detailed PWM delays are not explicitly modeled, the proposed MIL framework provides a realistic assessment of the control-integration behavior at system level.

4.2. Test 1: S-MMC Operation

The S-MMC links the AC grid to the HF port, which operates at 3.3 kV and 10 kHz. The main control objective is the regulation of the floating capacitor voltages in each cell. The converter comprises ten cells per cluster (sixty in total), the capacitor dynamics can be represented by the six CCVs as shown in (9), and the average voltage of the entire converter as indicated in (10), which is denoted by $v_{C_0}^{\Delta}$.

Figure 7a shows the evolution of the six CCVs during a step change in the reference voltage. All CCVs exhibit a coordinated transient, reaching the new operating point with low ripple. The peak-to-peak ripple remains well regulated in a $\pm 2\%$ band, with less than 100 V of ripple. The reference tracking of $v_{C_0}^{\Delta}$ is illustrated in Figure 7b. The average voltage follows the reference step with a damped transient, with a setting time of 500 ms, an overshoot less than 2%. This coordinated response validates the ability of the controller to maintain the average converter voltage.

The cluster currents are presented in Figure 7c. As expected, the S-MMC produces square-wave HF currents imposed by the DAB-based energy transfer mechanism. The current waveforms remain phase-aligned with the HF port voltage to ensure efficient power transfer. The zoomed-in view highlights the symmetry and periodicity of the HF current.

Finally, Figure 7d shows the modulation levels generated by the top and bottom clusters of the S-MMC leg. Both signals display sinusoidal envelopes that are shifted in phase by 180°, along with the high-frequency switching components needed to produce the HF square-wave output. Since the two cluster voltages are in contraphase, their difference yields a clean HF square voltage at the port.

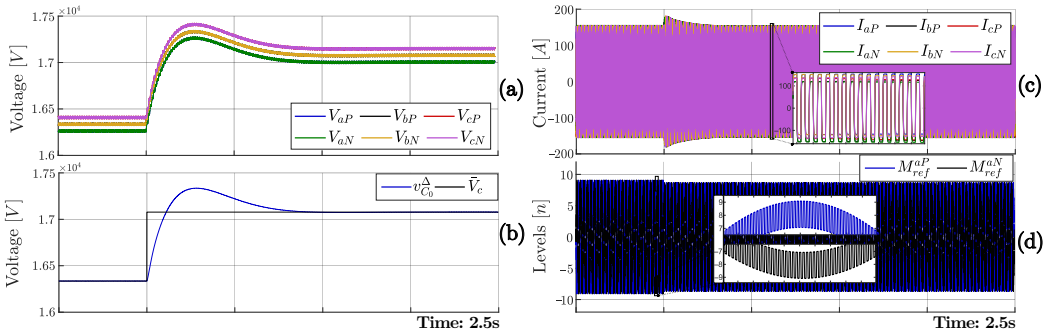


Figure 7. S-MMC balance variables: (**a**) CCVs. (**b**) Average voltage reference tracking. (**c**) Cluster Currents. (**d**) Voltage reference for a positive and negative cluster cells.

4.3. Test 2: Bidirectional HF Power Transfer Control

The first 100 ms shown in Figure 8a,b correspond to the steady-state operation of the system at rated power. The three-phase input voltages and currents remain balanced and sinusoidal during steady-state charging operation. The grid currents are in phase with the voltages, indicating unity power factor operation.

Figure 8c,d show a time-expanded view of the HF waveforms. The HF voltage exhibits a square-wave pattern from the S-MMC NLC sequence, and the HF current follows the trapezoidal waveform.

According to (17), the power transfer can be controlled by the phase shift between the input and output of the HF transformer. Figure 8e illustrates the phase shift, denoted as φ, between the input and output of the HF transformer for a single parallel DC port, first in charging with positive φ.

For V2G mode, the first 100 ms shown in Figure 8f,g corresponds to the steady-state operation of the system at rated inverse power. The three-phase input voltages and currents remain balanced and sinusoidal during steady-state charging operation. The grid currents are in antiphase with the voltages, indicating unity power factor operation for power injection to grid.

Similarly, Figure 8h,i shows the square-wave voltage in antiphase with the current, demonstrating the reverse flow defined by the negative φ, with energy from the batteries in the DC ports injected into the three-phase network. During this interval, the grid current leads the voltage, indicating reverse active power transfer.

Figure 8j illustrate the negative phase shift, between the input and output of the HF transformer for a single parallel DC port operating on V2G mode.

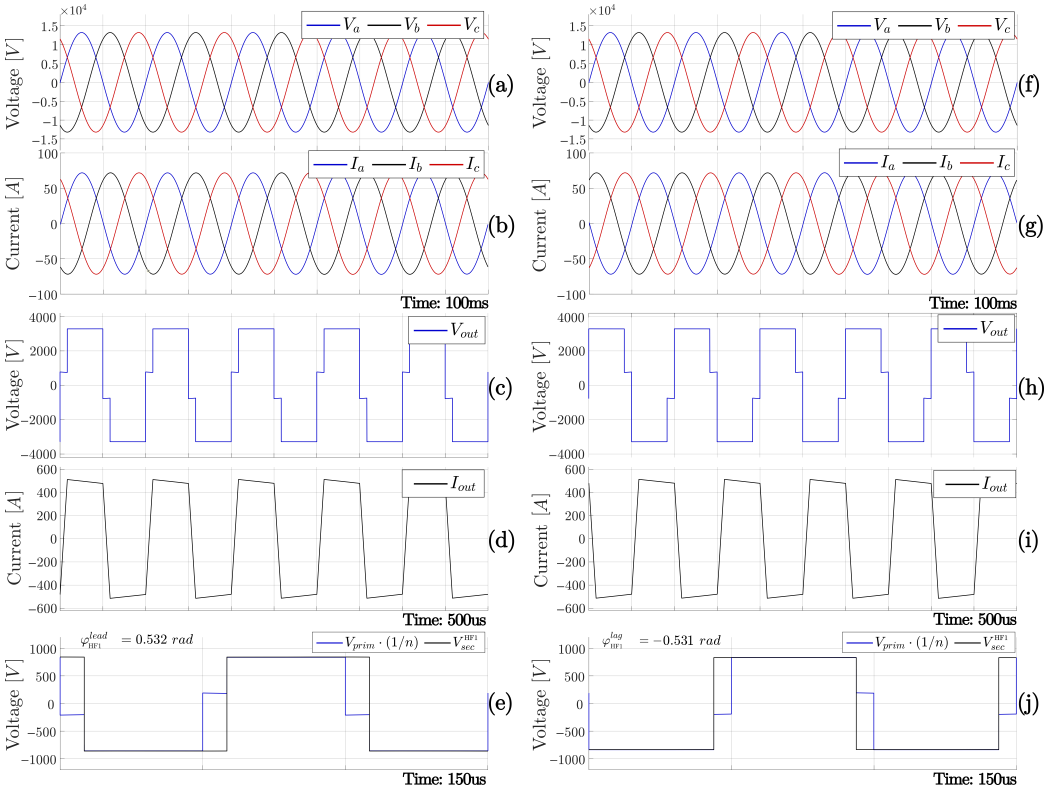


Figure 8. SP-MMC results of charging (**a**) input port AC voltages, (**b**) input port AC currents, (**c**) HF Voltage, (**d**) HF current, (**e**) HF_1 lead modulation reference with SPS for V2G power flow, and discharging (**f**) input port AC voltages, (**g**) input port AC currents, (**h**) HF Voltage, (**i**) HF current, (**j**) HF_1 lag modulation reference with SPS for discharging power flow.

4.4. Test 3: Multiple Charging and V2G Functionality

Figure 9 summarizes the behavior of the SP-MMC outputs during a multi-port charging sequence followed by a V2G multi-port discharging sequence operation. The test evaluates the capability of the control system to regulate six independent DC charging ports.

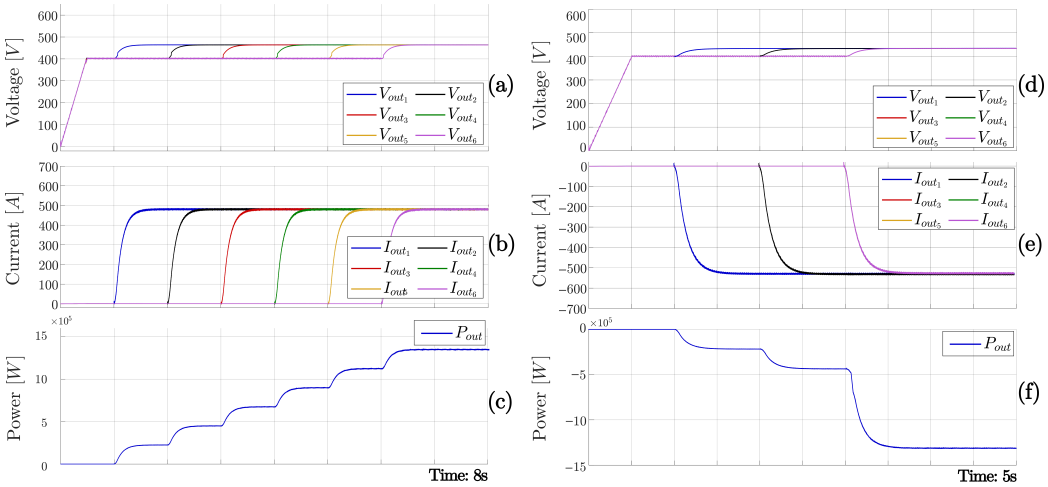


Figure 9. (**a**) DC charging port voltages. (**b**) DC charging port currents. (**c**) Output charging power. (**d**) DC V2G port voltages. (**e**) DC V2G port currents. (**f**) Output V2G power.

4.4.1. Charging Mode

The staircase power profile at the DC-side in Figure 9a reflects the sequential activation of the six DC ports, demonstrating the ability to operate with asymmetric loads, since as long as there is no power flow in a port, it remains preloaded without affecting system operation. Each port is regulated in voltage mode, considering 450 V vehicle batteries, increasing from an initial precharge level of 400 V to a charging target of 469 V. Then, the current is sequentially regulated to 479 A, as shown in Figure 9b. Each DC charging port is controlled to deliver ≈ 225 kW and is activated sequentially prior to its initial preload state, taking approximately 250 ms to stabilize to 90% of its nominal value. The SP-MMC operates under a progressive load until it reaches 1.350 MW, as shown in Figure 9c. Initially, φ is positive; therefore, six load steps of 225 kW are applied, as shown in Figure 9a,b, to the six DC ports operation in charging mode, with a DC port voltage that is higher than the batteries and positive current.

The 225 kW rating is selected as a representative operating point for a systems-level analysis. This value is used only as an illustrative example, as the same methodology applies to other charging power levels. In practical applications, DC fast-charging systems operate between 50 kW and 450 kW, consistent with the specifications defined for the Combined Charging System [47].

4.4.2. V2G Mode

Subsequently, the HF power transfer control modifies φ to reverse the power flow direction, starting in an initial preload state, taking approximately 350 ms to stabilize 90% of its nominal value. In this case, φ is negative; therefore the DC ports voltage are lower than the batteries regulated to 429 V and has negative current of 524 A as shown in Figure 9d,e, operating in V2G mode. This action reverses the DC-port current and establishes controlled power delivery to the grid. The active power then flows from the EV, shown in the negative staircase power profile in Figure 9f's output power. After a short stabilization interval, the voltage reference is decreased, and each port delivers its rated power back to the AC side.

During the V2G interval, the DC variables that are shown in Figure 9d,e remain well regulated and nearly constant for each power step, confirming correct control of the bidirectional power flow. The HF waveforms preserve the expected square-wave structure and the AC currents remain sinusoidal, demonstrating that the SP-MMC maintains grid-compliant operation in both charging and discharging modes.

As shown in the profiles of the charging and V2G modes, the system-controlled exhibits a damped response with no overshoot, preventing overvoltage at the battery

terminals. Likewise, the parameters are defined to reduce voltage oscillations and ripple currents.

4.5. Test 4: Low Voltage Ride Through Support

Figure 10 shows the result of a LVRT test applied at the AC input. An asymmetrical grid-voltage fault is imposed, after which the controller switches from normal operation to an LVRT mode that prioritizes reactive current support while limiting the power feed to the DC pots, following the codes studied in [48–50].

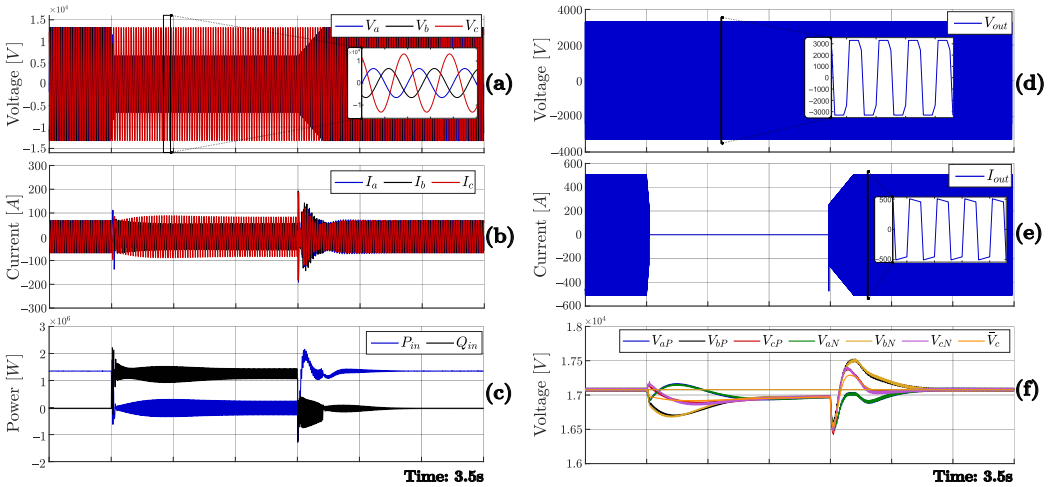


Figure 10. Variables of the LVRT test. (**a**) Input port AC voltages. (**b**) Input port AC currents. (**c**) Active and Reactive power. (**d**) HF port voltage. (**e**) HF current. (**f**) CCVs.

In Figure 10a, the three-phase input voltages show the programmed fault, with two phases reduced to half of their nominal magnitude for 1.5 s and then recovering to pre-fault conditions. Figure 10b shows the input currents regulated accordingly: once the fault is detected, the current transitions to the LVRT reference to provide reactive-current injection, while keeping the current magnitude bounded during the disturbance and the subsequent recovery transient. This behavior is reflected in Figure 10c, where the input active power is driven to zero during the fault, while the reactive power is increased to provide grid support. After fault clearance, both powers return to their nominal references.

The coordination between the S-MMC side and the P-MMC side by the HF link is shown in Figure 10d,e. In Figure 10d, the HF-port voltage remains properly synthesized throughout the event, indicating that the HF stage stays commutated even when power transfer is stopped. Consistently, Figure 10e shows the HF current being regulated to zero during the fault interval to prevent overcurrents. Following fault clearance, the HF current is re-established with a ramped profile to avoid power overshoot. Finally, Figure 10f illustrates the CCV behavior during LVRT. The average CCV magnitude decreases throughout the fault, since no active power is supplied to the converter to maintain voltage regulation. This temporary imbalance is resolved once the fault is cleared.

5. Conclusions

This paper presents a hierarchical control system and a systems-level integration scheme for a multi-port, bidirectional SP-MMC charging system. The SP-MMC topology provides modular, isolated, and multiple DC EV charging options. The demonstrated novelty lies in the integration of the control layers, which manage the dynamics of power conversion and the interaction of the six concurrent high-power ports.

The proposed topology and control system were evaluated using MIL simulations implemented in PLECS. The results verify the correct dynamic response during charging, V2G

operation, and LVRT operation. The grid, S-MMC, HF stage, and DC ports were regulated while floating capacitor voltages were maintained within the allowed range. Quantitative performance indicators include DC-link voltage ripple below 2% of the nominal value, settling times below 500 ms, accurate per-port current tracking, and near-unity power factor at the grid, even under grid-fault conditions.

While the MIL results assume ideal magnetic components, the results provide evidence of the operation of the proposed control architecture at a system level. Future work will focus on hardware implementation and experimental validation, including magnetic co-design, loss optimization, and compliance with grid-code requirements under extreme operating conditions. In addition, robust nonlinear controllers will be explored to benchmark and enhance the PI/PR loops under abrupt port/grid disturbances, while extending capacitor-voltage balancing robustness checks to initial dispersion and fault-tolerant modes. Overall, the proposed SP-MMC-based solution represents a promising and flexible platform for next-generation multi-port fast-charging and V2G-enabled applications.

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