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Multimodal Switching Control Strategy for Wide Voltage Range Operation of Three-Phase Dual Active Bridge Converters

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Abstract: In recent years, to achieve "dual carbon" goals, increasing the penetration of renewable energy has become a critical approach in China's power sector. Power electronic converters play a key role in integrating renewable energy into the power system. Among them, the Dual Active Bridge (DAB) DC-DC converter has gained widespread attention due to its merits, such as galvanic isolation, bidirectional power transfer, and soft switching. It has been extensively applied in microgrids, distributed generation, and electric vehicles. However, with the large-scale integration of stochastic renewable sources and uncertain loads into the grid, DAB converters are required to operate over a wider voltage regulation range and under more complex operating conditions. Conventional control strategies often fail to meet these demands due to their limited soft-switching range, restricted optimization capability, and slow dynamic response. To address these issues, this paper proposes a multi-mode switching optimized control strategy for the three-port DAB (3p-DAB) converter. The proposed method aims to broaden the soft-switching range and optimize the operation space, enabling high-power transfer capability while reducing switching and conduction losses. First, to address the issue of the narrow soft-switching range at medium and low power levels, a single-cycle interleaved phase-shift control mode is proposed. Under this control, the three-phase Dual Active Bridge can achieve zero-voltage switching and optimize the minimum current stress, thereby improving the operating efficiency of the converter. Then, in the face of the actual demand for wide voltage regulation of the converter, a standardized global unified minimum current stress optimization scheme based on the virtual phase-shift ratio is proposed. This scheme establishes a unified control structure and a standardized control table, reducing the complexity of the control structure design and the gain expression. Finally, both simulation and experimental results validate the effectiveness and superiority of the proposed multi-mode optimized control strategy.

Keywords: three-port dual active bridge (3p-DAB); multi-mode control strategy; soft switching; voltage regulation; renewable energy integration

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1. Introduction

In recent years, the global energy crisis has accelerated the search for clean and efficient alternatives to fossil fuels [1]. With the goal of achieving carbon neutrality and peak carbon emissions, countries worldwide are promoting the transition to low-carbon energy systems [2]. China, in particular, has proposed the "dual carbon" target, which

places increasing pressure on the power industry to integrate more renewable energy sources [3]. However, the shift towards renewable energy introduces challenges due to the intermittency and randomness of sources like wind and solar [4]. These challenges are especially significant for grid stability and efficient energy conversion [5], particularly in hybrid wind/solar systems where accurate current sharing and voltage regulation are critical [6]. As the International Energy Agency warns of continued pressure on global electricity demand, innovations in power electronic converters become essential [7].

The Dual Active Bridge (DAB) DC converter is often used in the energy exchange field due to its advantages such as electrical isolation, bidirectional energy flow, and easy realization of soft switching [8,9]. In practical applications, the three-phase DAB (3p-DAB) converter has become a key component in many energy systems, which typically require high power density and flexible voltage adaptation capabilities. For example, in the vehicle-to-vehicle energy sharing system [10], as an intermediate energy converter, DAB realizes fast bidirectional energy transmission between electric vehicles and needs to maintain soft-switching performance within a wide voltage range. Similarly, in microgrid and distributed generation systems [11,12], 3p-DAB is often used to connect distributed energy sources with DC buses, achieving efficient energy routing and enhanced system stability. In these scenarios, the operating conditions are complex and changeable, and frequent mode switching and voltage fluctuations place higher demands on control strategies. Therefore, the control method not only needs to optimize converters with specific rated power but also have good scalability and adaptability [13]. Although the multi-mode switching strategy proposed in this paper is verified based on a 15 kW prototype, it is essentially driven by a modular algorithm and has good versatility, making it applicable to a wider range of multi-port DC-DC converter systems.

At present, the mainstream control method for 3p-DAB is still single-phase-shift (PS) control. Although this control method is simple and reliable, when the voltage gain is not 1, especially under light load conditions, the operating range of zero voltage switching (ZVS) is greatly limited, thereby increasing switching losses [14–16]. In addition, since the degree of freedom of single-phase-shift control is only 1, it cannot optimize the generated conduction losses [17]. These transmission losses are very unfavorable for batteries with limited energy. To improve the operating efficiency of 3p-DAB, scholars have proposed some new control methods. Reference [18] proposes a numerical algorithm for a duty cycle control (DCC) composed of three degrees of freedom to obtain a modulation scheme with minimum conduction loss within the entire load range. However, the derivation process of this scheme is complex. Once the parameters change, it is necessary to recalculate the numerical table, which has a large calculation amount and lacks universality, making it difficult to further apply in practice. Reference [19] proposes an asymmetric phase-shift (APS) modulation scheme, which introduces a variable phase shift between the phase legs of the converter to achieve the minimum root mean square (RMS) current, but this results in different current magnitudes for each switch, leading to uneven losses and excessive current stress. Reference [20] proposes a synchronous parallel-phase operation method for 3p-DAB, but it does not elaborate on the specific operation steps. Moreover, simple parallel operation leads to the redundancy of switching devices and an uneven utilization rate, as well as reducing the power transmission upper limit.

In contrast, the control methods for 1p-DAB are more mature. The traditional control method is single-phase-shift (SPS) control, but the mismatch between the input voltage and output voltage makes it difficult for the converter to achieve ZVS [21]. The most mainstream approach is to expand the optimization space by increasing the degrees of freedom of control. Therefore, extended-phase-shift (EPS) control, dual-phase-shift (DPS) control, and three-phase-shift (TPS) control have been proposed successively [22–25]. Among them,

Reference [22] proposes a unified three-phase-shift (UTPS) scheme to achieve minimum current stress optimization and soft switching for 1p-DAB. Reference [24] proposes a minimum reactive power optimization scheme under TPS control. Reference [25] proposes a quasi-optimal RMS control strategy based on an inductor RMS current optimization algorithm to achieve full ZVS. These methods have been proven to effectively optimize the operating state of 1p-DAB, but they cannot be directly applied to 3p-DAB due to differences in circuit topologies.

Considering the actual needs of wide voltage and high-efficiency operation in practical applications of 3p-DAB in electric vehicle energy sharing, microgrids, and distributed generation systems, the main work of this paper is as follows:

1. Firstly, aiming at the problem that the traditional control of 3p-DAB is difficult to achieve soft switching and target optimization under wide voltage range and medium- to low-power conditions, the 3pSPCPS working mode is proposed to enable 3p-DAB to operate in a mode similar to 1p-DAB. In this mode, 3p-DAB adopts synchronous parallel operation, which can be equivalent to 1p-DAB, and then operates in a periodic cyclic rolling manner to ensure a consistent utilization rate of switching tubes. By invoking the TPS control scheme, ZVS and minimum current stress optimization are achieved, thereby improving the working efficiency in the medium–low power range.
2. Then, facing the actual demand for wide voltage regulation of 3p-DAB, a standardized, unified, minimum current stress optimization scheme based on a virtual phase-shift ratio is proposed. This scheme introduces a virtual phase-shift ratio to eliminate power aliasing and establishes a unified control structure and optimization control table as a standard quantity, which can reduce the complexity of controller design and gain expression.
3. Finally, through detailed theoretical modeling, simulation, and hardware-in-the-loop (HIL) experiment verification, improvement in efficiency and soft-switching performance is confirmed.

2. Three-Phase, Single-Cycle, Parallel-Cycling Phase-Shifting (3pSPCPS) Mode

2.1. Basic Working Principle of the 3pSPCPS Mode

Research on the control strategy for 1p-DAB is already relatively mature. Despite a slight increase in complexity with TPS control, it achieves the optimization of minimal electrical power stress within the power range and has proven capable of enabling soft switching. The analysis reveals a complementary advantage between these two types of converters, and organically integrating their strengths constitutes the primary research approach of this paper. To enable 3p-DAB to operate in a mode similar to 1p-DAB at medium to low power, this paper introduces a new operating mode based on the topology of 3p-DAB.

Figure 1 presents the schematic topology of 1p-DAB and 3p-DAB. In 3p-DAB controlled by traditional single-phase-shift, the three-phase bridge arms of each 3p-H bridge are shifted by 120°, with a phase-shift angle D between the corresponding bridge arms of the front and back 3p-H bridges. Thus, each pair of corresponding bridge arms can be considered consistent with the SPS modulation of 1p-DAB, allowing 3p-DAB to function as a parallel connection of three single-phase versions. Similarly, 3p-DAB can also be regarded as three 1p-DABs under TPS modulation that are shifted in phase and interconnected. Figure 2 presents a feasible scheme for transitioning from a 3-phase DAB to a 1-phase DAB operation, where the control method adopted is a parallel-phase operation scheme, that is, $S_B = S_C, S_b = S_c$, with a phase difference existing between S_C and S_B.

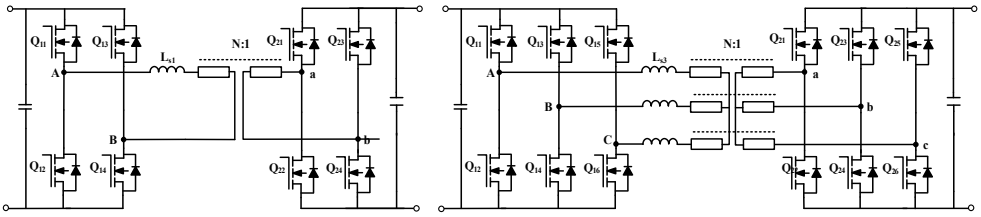


Figure 1. Topology diagram of 1p-DAB and 3p-DAB.

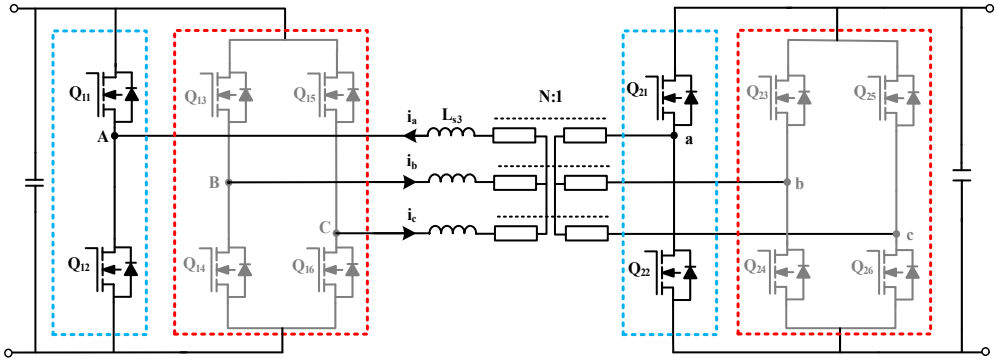


Figure 2. 3p-DAB parallel-phase operation diagram.

In fact, there are many ways to operate 3p-DAB in a mode similar to 1p-DAB, which can be divided from a timeline perspective into non-cyclic and cyclic modes. The non-cyclic mode means that the driving signal for each clock cycle remains unchanged, while the cyclic mode requires exchanging the driving signals of the bridge arms within a certain time period. The cyclic mode can further be divided into fixed-cycle and single-cycle modes. Moreover, based on the topological state of the circuit during single-cycle operation, it can be categorized into a parallel-phase operation and single-phase operation. Table 1 compares the advantages and disadvantages of several feasible schemes for operating 3p-DAB in a manner similar to 1p-DAB.

Table 1. Comparison of advantages and disadvantages of three feasible schemes of 3p-DAB and 1p-DAB.

	Non-Cyclic	Fixed Cycle	Single Cycle
Single phase	Advantages: Simple implementation, high reliability Disadvantages: Circuit redundancy	Advantages: Higher reliability Disadvantages: Inefficient circuit utilization	Advantages: Higher reliability Disadvantages: Inefficient circuit utilization
Parallel phase	Advantages: Efficient circuit utilization Disadvantages: Uneven heating, high requirements for parallel symmetry	Advantages: Efficient circuit utilization, uniform heating Disadvantages: Control requires additional costs, fluctuations in the cycling process, high requirements for parallel symmetry	Advantages: High circuit utilization, uniform heating, low thermal design difficulty Disadvantages: High requirements for parallel symmetry

Comparing the various schemes of operating 3p-DAB in a 1p-DAB mode as presented in Table 1, it is observed that while the single-phase approach is simple and reliable, it suffers from low circuit utilization. Moreover, differential heating due to operational phases can lead to uneven heating of the circuit board, increasing the difficulty of the thermal design in high-power applications. The advantage of the parallel-phase operation lies in the full utilization of the circuit, significantly reducing thermal design challenges. From a timeline perspective, the single-cycle cyclic operation ensures uniform heating across

the circuit, easing the design complexity in control. Additionally, influenced by modern switch tube technology, a high degree of symmetry in the parallel phase operation is more achievable. Therefore, this paper adopts a single-cycle cyclic operation with a parallel phase, termed in this study as Three-Phase, Single-Cycle, Parallel-Cycle Phase-Shifting (Three-phase, single-cycle, parallel-cycle, 3pSPCPS).

2.2. Detailed Analysis of 3pSPCPS Applied to DAB

Although the previous section introduced a basic concept for operating 3p-DAB in a manner similar to 1p-DAB, there are some issues in the actual design, including how and when to switch. This section primarily focuses on these specific details, analyzing and explaining them to address the challenges of 3pSPCPS in practical applications.

(1) The Concept of Switching

The control of the 1-phase DAB can be divided into four groups of PWM waves to control four bridge arms. For ease of explanation, the bridge arms are numbered 1, 2, 3, and 4 from the primary to the secondary side. It is defined that $PWM_{X,X\in\{1,2,3,4\}} = 1$ means the upper tube of the corresponding X bridge arm is turned on and the lower tube is turned off; $PWM_{X,X\in\{1,2,3,4\}} = 1$ means the upper tube of the corresponding X bridge arm is turned off and the lower tube is turned on. The control of the 3-phase DAB can be divided into six groups of PWM waves for controlling six bridge arms. The three-phase bridge arms of the front bridge are defined as A, B, and C, and those of the rear bridge as a, b, and c. It is defined that $S_{X,X\in\{A,B,C,a,b,c\}} = 1$ means the upper tube of the corresponding X bridge arm is turned on, and the lower tube is turned off; $S_{X,X\in\{A,B,C,a,b,c\}} = 0$ means the upper tube of the corresponding X bridge arm is turned off, and the lower tube is turned on. Since there is only a delay between the corresponding tubes of the front and rear bridges, the analysis can be limited to the state of the front bridge for switching purposes. The operations of the rear bridge corresponding to the front bridge arms are consistent, with only a certain delay.

The DAB operation in the 3pSPCPS mode requires providing two types of modulation waves for the front bridge, similar to the modulation waves under TPS control of the single-phase Dual Active Bridge DC converter. For 3p-DAB, the front bridge has three bridge arms requiring three types of modulation waves (i.e., S_A, S_B, S_C). For ease of analysis, PWM_1 and PWM_2 can be considered fixed, and the 3pSPCPS modulation can be seen as distributing the three modulation waves S_A, S_B, S_C to the two types PWM_1 and PWM_2 in a single-cycle, parallel-phase cycling manner.

(2) Switching State and Sequence

The 3pSPCPS control requires a switch at every clock cycle, with Figure 3 showing the operational state of the switch tubes at moments T_1 and T_2. At T_1, the driving signal for the first bridge arm is PWM_1, while the second and third bridge arms operate in parallel phase with a PWM_2 signal. At T_2, the first and second arms operate in parallel phase with a PWM_1 signal, and the third arm receives a PWM_2 signal, with only one phase-shift operation occurring between the two moments, that is, a phase shift of S_C. The post-switch state and sequence of states in 3pSPCPS are not arbitrary and require consideration of the following issues:

Switching State: It is necessary to ensure that within a large cycle period under steady state, the duration and state of each switch are the same. This uniformity allows for consistent utilization of all switches, thereby ensuring even heating.

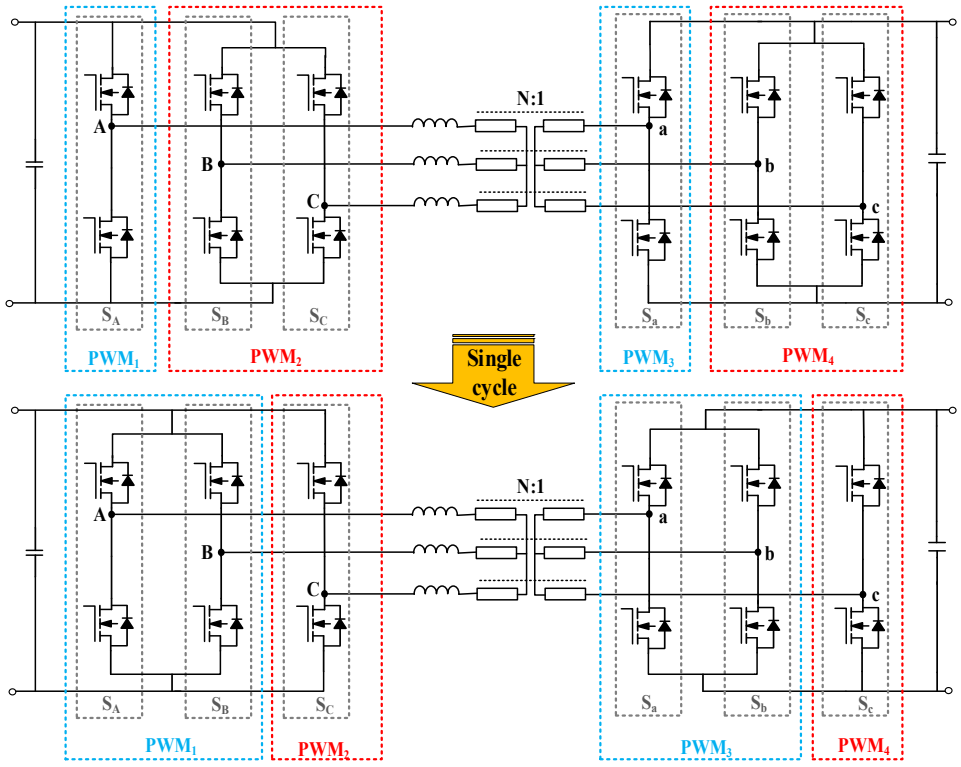


Figure 3. Operating status of switch tube at $Power_1$ and T_2.

Switching Sequence: Each switch state will involve a phase-shifting operation, with the requirement that the fewer phase-shifting operations during switching, the better. This helps to reduce the loss during commutation and the EMI generated during phase-shifting.

Taking into account the above two issues, this paper presents a reasonable and feasible switching state and sequence as shown in the Table 2. It can be seen that within a large clock cycle, there are six states, with only one phase-shifting operation occurring in each state transition (as indicated by the purple mark), and the operation of each switch, aside from a certain delay, is the same. This ensures uniform heating of all switches and effectively reduces the electromagnetic interference caused by phase-shifting during each clock cycle switch.

Table 2. Table of switching status and switching sequence.

	T_1	**T_2**	**T_3**	**T_4**	**T_5**	**T_6**	**T_7**
PWM_1	S_A	S_A, S_B	S_B	S_B, S_C	S_C	S_C, S_A	S_A
PWM_2	S_B, S_C	S_C	S_C, S_A	S_A	S_A, S_B	S_B	S_B, S_C

(3) Switching Time Points

After determining the switching state and sequence for each cycle, the specific switching moments within the cycle need to be identified. The analysis continues with the transition from parallel phases B, C to A, B as shown in Figure 4, presenting four typical switching time nodes. The impact of these four switching times on control is analyzed next:

A. Choosing time node t_1 for switching from phase PWM_2 to PWM_1 for B, even though no switch tube operation occurs, the duty cycle of B within T is not 50%, leading to a DC bias issue at the switching moment.

B. At time node t_2, switching from 6 back to PWM_1 instantly changes B's state from $S_B = 0$ to $S_B = 1$, resulting in additional switching losses. Similarly, the duty cycle of B within T not being 50% introduces a DC bias issue.

C. Selecting time node t_3 and switching from PWM_2 back to PWM_1 for B, B's state instantly remains at $S_B = 0$, avoiding additional switching losses. Moreover, with B's duty cycle within T remaining at 50%, DC bias issues are prevented.

D. By choosing time node t_4 for switching from PWM_2 back to PWM_1, both A and B's states instantly change from $S_A = 0$ to $S_A = 1$, causing extra switching losses. However, B's duty cycle within T still being 50% prevents DC bias issues.

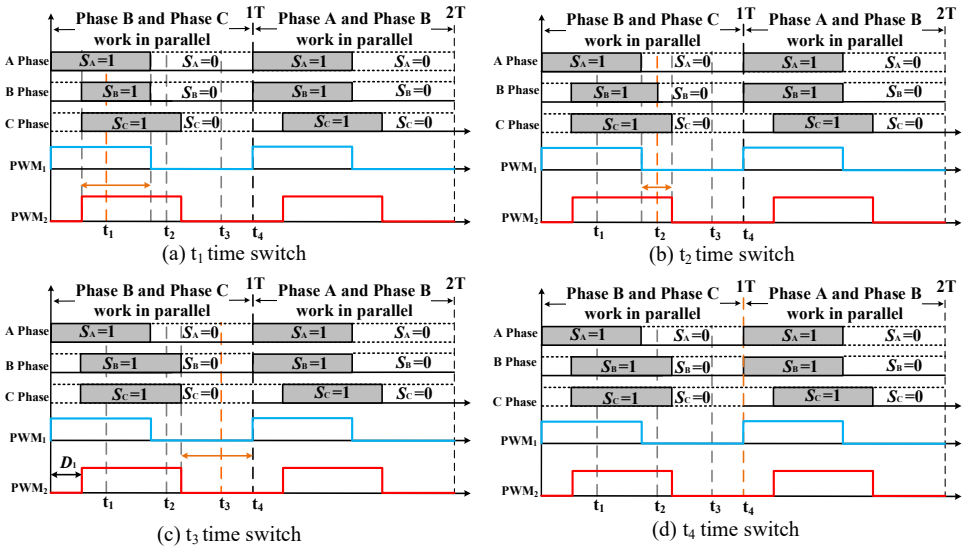


Figure 4. Four typical switching time node operations.

Upon comprehensive analysis of the circuit operational effects at the four typical switching times, employing interval t_3 for switching results in the circuit operating in an optimal state. This paper selects the midpoint of the interval t_3 as the switching moment, corresponding to

$$t_3 = (\frac{D_1}{4} + \frac{3}{4})T \quad (1)$$

In Equation (1), D_1 denotes the duty ratio of the switching signal during one cycle, and T represents the full duration of a switching cycle.

3. Standardized Global Unified Operation Strategy Under Wide Voltage Range

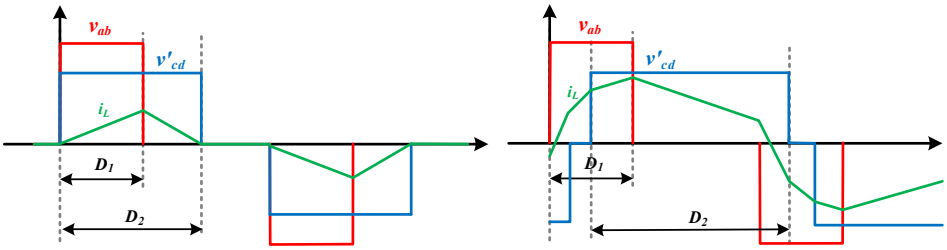
3.1. Wide Voltage Range Optimization Scheme at Low and Medium Power Levels

The 3pSPCPS mode is applied to 3p-DAB operating at medium and low transmission powers to optimize minimal reverse power and enable soft switching at medium and low powers, similar to the operating state of 1p-DAB under TPS modulation. Section 2.1 analyzes the operating characteristics and optimization of 1p-DAB under TPS modulation, presenting an optimized scheme for step-down 1p-DAB in forward transmission mode. To achieve minimal current stress optimization, the conclusion is to use Mode3A at low power and Mode4B at high power. Other modes will not be considered in this paper due to their inability to meet the optimization criteria. Following the analysis in this paper, DAB operating conditions are divided into four categories based on power range (defined as $P\text{ower}_1$, $P\text{ower}_2$, $P\text{ower}_3$, and $P\text{ower}_4$, respectively), with this section focusing on optimization schemes for medium and low power. Based on the analysis in Section 2, the optimization scheme for step-down power transmission is presented directly as shown in Table 3.

Table 3. Optimal buck scheme for forward power transmission at medium and low power.

Condition	Power Range	Operating Mode	Optimization
$Power_1$	$\left[0, \frac{(1-d)d^2\pi}{2}\right]$	$3pSPCPS_tri$	$D_{1\text{opt}} = \sqrt{\frac{2P_{on}}{(1-d)\pi}}, D_{2\text{opt}} = \frac{1}{d}\sqrt{\frac{2P_{on}}{(1-d)\pi}}, D_{fopt} = \frac{\sqrt{2(1-d)\pi P_{on}}}{2d\pi}$
$Power_2$	$\left(\frac{(1-d)d^2\pi}{2}, \frac{d\pi}{4}\right]$	$3pSPCPS_trape$	$D_{1\text{opt}} = 1-(1-d)\sqrt{\frac{d\pi-4P_{on}}{(1-2d+2d^2)d\pi}}, D_{2\text{opt}} = 1,$ $D_{fopt} = \frac{1}{2} - \frac{1}{2}\sqrt{\frac{d(d\pi-4P_{on})}{(1-2d+2d^2)\pi}}$

Figure 5 shows the circuit basic switch current waveforms under two working conditions, $P\text{ower}_1$ and $P\text{ower}_2$. It can be seen that the inductor current waveform is a triangular wave under the $P\text{ower}_1$ working condition and soft switching can be achieved. Therefore, the working mode at this time is defined as $3pSPCPS_tri$. Under the $P\text{ower}_2$ working condition, the inductor current waveform is a trapezoidal wave, and soft switching can also be achieved. The working mode at this time is defined as $3pSPCPS_trape$.



(a) 3pSPCPS_tri:Inductor Current Triangle Wave

(b) 3pSPCPS_trape:Inductive Current Trapezoidal Wave

Figure 5. Switch current waveform of a circuit under two working conditions of $P\text{ower}_1$ and $P\text{ower}_2$.

To satisfy the requirements for a wide voltage range, this section provides an optimization scheme for forward power transmission with a voltage gain greater than 1. Analyzing the waveforms in Figure 5, the voltage and inductor current are symmetrical during the step-up and step-down phases, with output power and cyclic power being identical. This allows for a similar transformation to propose an optimization scheme for boost operation in forward power transmission.

$$\begin{cases} \hat{d} = 1/d \\ \hat{v}_{ab} = v'_{cd} \\ \hat{v}'_{cd} = v_{ab} \\ \hat{D}_1 = D_2 \\ \hat{D}_2 = D_1 \\ \hat{D}_3 = D_2 + D_3 - D_1 \end{cases} \tag{2}$$

In Equation (2), $\hat{v}_{ab}$ and $\hat{v}'_{cd}$ denote the equivalent voltages on the primary and secondary sides of the transformer, respectively. d is the voltage gain, D_1 and D_2 are the primary- and secondary-side duty ratios under the current operating mode, and D_3 is introduced as an equivalent normalized duty ratio, providing a unified expression for power transfer analysis across the primary and secondary sides. Its equivalent transformation satisfies the Equation (2). The forward boost optimization scheme obtained after the transformation is shown in Table 4.

Table 4. Boost optimization scheme for forward power transmission at medium and low power.

Condition	Power Range	Operating Mode	Optimization
$Power_1$	$\left[0, \frac{(d-1)\pi}{2d^3}\right]$	$3pSPCPS_tri$	$D_{1\text{opt}} = \sqrt{\frac{2dP_{on}}{(d-1)\pi}}, D_{2\text{opt}} = d\sqrt{\frac{2dP_{on}}{(d-1)\pi}}, D_{fopt} = \frac{d\sqrt{2(1-1/d)\pi P_{on}}}{2\pi}$
$Power_2$	$\left(\frac{(d-1)\pi}{2d^3}, \frac{\pi}{4d}\right]$	$3pSPCPS_trape$	$D_{1\text{opt}} = 1 - \sqrt{\frac{d\pi - 4d^2P_{on}}{(d-1)\pi}}, D_{2\text{opt}} = 1,$ $D_{fopt} = \frac{1}{2} - \frac{1}{2}\sqrt{\frac{1/d(\pi/d - 4P_{on})}{(1-1/d)^2\pi}}$

The optimization control scheme can be further simplified by changing the per-unit value to Equation (3), resulting in a simplified optimization control scheme for forward medium and low power transmission over a wide voltage range, as shown in Table 5.

$$I_b = \frac{V_1}{4fL_{S1}}, P_b = \frac{V_1^2}{2fL_{S1}} \tag{3}$$

Table 5. Optimal control scheme of wide voltage in forward medium and low transmission power.

Voltage Gain	Condition	Power Range	Operating Mode	Optimization
$d < 1$	$Power_1$	$\left[0, \frac{d^2(1-d)}{2}\right]$	$3pSPCPS_tri$	$\begin{cases} D_1 = \sqrt{\frac{2dP_n}{1-d}} \\ D_2 = \frac{D_1}{d}, D_3 = 0 \end{cases}$
	$Power_2$	$\left[\frac{d^2(1-d)}{2}, \frac{d}{4}\right]$	$3pSPCPS_trape$	$\begin{cases} D_1 = 1 - (1-d)\sqrt{\frac{1-4P_n}{1-2d+2d^2}} \\ D_2 = 1, D_3 = \frac{D_1 - d}{2(1-d)} \end{cases}$
$d \geq 1$	$Power_1$	$\left[0, \frac{d-1}{2d^3}\right]$	$3pSPCPS_tri$	$\begin{cases} D_2 = \sqrt{\frac{2P_n}{d-1}} \\ D_1 = dD_2, D_3 = dD_2 - D_2 \end{cases}$
	$Power_2$	$\left[\frac{d-1}{2d^3}, \frac{1}{4d}\right]$	$3pSPCPS_trape$	$\begin{cases} D_2 = 1 - (d-1)\sqrt{\frac{1-4P_n}{d^2-2d+2}} \\ D_1 = 1, D_3 = \frac{(2-d)D_2 + 2d - 3}{2(d-1)} \end{cases}$

In Equation (3), the input voltage V_1, series inductance L_{S1}, and switching period f are used to define the power and current base values for the normalization process. The base current I_b and base power P_b are fundamental references for the per-unit control design.

3.2. Control Scheme for Wide Voltage Range Under High-Power Conditions

To facilitate standardized comparative analysis, the per-unit value is adopted as $I_b = V_1T_s/4L_{s3}$, $P_b = V_1^2T_s/2L_{s3}$, and the maximum value of the duty cycle D is constrained to 1/2. The per-unit normalized expression of the power transfer characteristic is thus given by Equation (4):

$$P_{3pSPS} = \begin{cases} 2dD_{3pSPS} - \frac{3dD_{3pSPS}^2}{2} & \forall 0 \leq D_{3pSPS} \leq \frac{1}{3} \\ 3d\left(D_{3pSPS} - D_{3pSPS}^2\right) - \frac{d}{6} & \forall \frac{1}{3} \leq D_{3pSPS} \leq 1/2 \end{cases} \tag{4}$$

By solving the above equation, the relationship between the phase-shift angle D_{3pSPS}, the transmitted power P_n, and the gain d under the forward high transmission power

condition for the 3p-DAB is obtained as Equation (5). The corresponding control table under this condition is shown in Table 6.

$$D_{3pSPS} = \begin{cases} \frac{2}{3} - \frac{1}{3}\sqrt{4 - \frac{6P_n}{d}} & \forall 0 \le P_n \le d/2 \\ \frac{1}{2} - \frac{1}{2}\sqrt{\frac{7}{9} - \frac{4P_n}{3d}} & \forall 0 \le d/2 \le P_n \le 7d/12 \end{cases} \quad (5)$$

Table 6. Lower control table of forward high transmission power.

Power Range	Operating Mode	Optimization Strategy
$\left[0, \frac{d}{2}\right]$	$3pSPS$	$D_{3pSPS} = \frac{2}{3} - \frac{1}{3}\sqrt{4 - \frac{6P_n}{d}}$
$\left[\frac{d}{2}, \frac{7d}{12}\right]$	$3pSPS$	$D_{3pSPS} = \frac{1}{2} - \frac{1}{2}\sqrt{\frac{7}{9} - \frac{4P_n}{3d}}$

3.3. Standardized Unification Based on Virtual Phase-Shift Ratio

(1) Correction of Operating Range under Medium- and Low-Power Conditions

The per-unit expressions for medium/low power and high power are structurally similar. However, it is evident that under medium- and low-power conditions, employing the 3pSPCPS control strategy alters the 3p-DAB topology, making it not entirely equivalent to a 1p-DAB. The most significant difference lies in the use of parallel phase operation, which changes the effective inductance of the circuit. Considering the symmetry of the leakage inductances in the three phases of the 3p-DAB, the leakage inductance for each phase is defined as $L_{s3} = L$. When the 3p-DAB operates under the 3pSPCPS mode, the effective leakage inductance satisfies the following relationship:

$$L_{s1} = 1.5L_{s3} = 1.5L \quad (6)$$

Therefore, it is necessary to correct the operating range under medium- and low-power conditions. After correction, the applicable power range is as specified in Table 7. It should be noted that the power correction affects only the boundary expressions of the operating conditions and does not impact the optimization strategies across different operating scenarios.

(2) Expanding the Meaning of the External Phase-Shift Ratio D_f

Table 7. Corrected low and medium power range table.

Voltage Gain	$Power_1$	$Power_2$
$d < 1$	$\left[0, \frac{d^2(1-d)}{3}\right]$	$\left[\frac{d^2(1-d)}{3}, \frac{d}{6}\right]$
$d \ge 1$	$\left[0, \frac{d-1}{3d^3}\right]$	$\left[\frac{d-1}{3d^3}, \frac{1}{6d}\right]$

Based on the above analysis, operating conditions are divided based on voltage gain and power range. Generally, the voltage gain is known, but the power range needs to be detected. Due to the effects of system output capacitor charging and discharging as well as detection delay, changes in detected power are lagging. Directly dividing operating conditions based on detected power presents the following disadvantages:

1. Slow dynamic response, with ringing occurring under input and load disturbances.
2. Mode switching under multiple conditions can oscillate due to the lagging effect of power.
3. It may affect system stability, requiring higher stability margins for the control system.

Therefore, directly using detected power for dividing operating conditions and optimizing control in the control system is not an optimal solution. In forward transmission mode, its value range is [0, 0.5], with a larger amplitude corresponding to a higher transmission power. For 3p-DAB under 3pSPS control, there are no D and F, nor is there the concept of the external phase-shift ratio. However, there is a phase-shift angle D_{3pSPS}, which is also related to the DAB's transmission power, with a value range of [0, 0.5] in forward transmission mode. Furthermore, the value ranges of D_f and D_{3pSPS} overlap, making them unsuitable as references for mode switching. To this end, this paper extends the traditional meaning of D_f in 1p-DAB to the full power range of 3p-DAB (defined as the virtual phase-shift ratio D_f). After the extension, the value range is [0, 1]. Through the virtual phase-shift ratio, the power aliasing between modes can be solved, which is beneficial for mode identification and reduces the complexity of the optimal control expression. In the 3pSPCPS mode, the D_f value range is [0, 0.5], while in the 3pSPS mode, the D_f value range is [0.5, 1]. Additionally, a virtual relationship is established, satisfying the equation:

$$\begin{cases} D_f = D_3 + D_2/2 - D_1/2 \\ D_1 = 0, D_2 = 0 \\ D_{3pSPS} = f(D_3) \\ D_f \in (0.5, 1] \end{cases} \tag{7}$$

Here, $f(D_3)$ represents the functional relationship between D_{3pSPS} and D_3 in the 3pSPS operating mode.

(3) Unification of Reference Quantities Across the Full Power Range

Based on the above analysis, this paper selects D_f as the control reference quantity within the full power range. The critical step towards unification is to establish the relationship between D_{3pSPS} and D_f, that is, to solve for $f(D_3)$. A pivotal issue addressed is the power overlap problem under the two operating modes.

Here, the analysis is conducted in step-down mode, while the step-up mode can be derived similarly. $P_{M_1p\text{-}DAB} = 0.25d$ represents the maximum transmission power under the condition $Power_2$, and it has been calculated that the power point falls within the quasi-high power range, satisfying the expression G.

$$\begin{cases} P_n = P_{M_1\text{p-DAB}} = \frac{d}{4} \\ D_{3pSPS} = \frac{2}{3} - \frac{1}{3}\sqrt{4 - \frac{6P_n}{d}} \end{cases} \tag{8}$$

Solving the above expression yields the boundary solutions for the two mode transitions as

$$D_{boundary_3pSPS} = \frac{2}{3} - \frac{\sqrt{10}}{6} \tag{9}$$

Due to the substantial overlap in the power range, the adjustable range of D_f within the high power range is less than 0.5. Therefore, transformation expression (10) is introduced to extend $D_f's$ range to 1, thus establishing the relationship between D_f and D_{3pSPS} under 3pSPS control.

$$D_f = \left(D_{3pSPS} - D_{boundary_3pSPS}\right)\frac{0.5}{0.5 - D_{boundary_3pSPS}} + 0.5 \tag{10}$$

The inverse function is obtained as follows:

$$D_{3pSPS} = \left(D_f - 0.5\right)\frac{0.5 - D_{boundary_3pSPS}}{0.5} + D_{boundary_3pSPS} \tag{11}$$

Under high-power operation, two additional operating modes exist. To partition the operating conditions, it is likewise necessary to determine their power boundary, which is defined by the following expression:

$$\begin{cases} P_n = P_{boundary_high-power-intermediate-state} = \frac{d}{2} \\ D_{3pSPS} = \frac{2}{3} - \frac{1}{3}\sqrt{4 - \frac{6P_n}{d}} \end{cases} \tag{12}$$

Solving for $D_{3pSPS} = 1/3$ and substituting into the transformation formula yields the power boundary:

$$D_f = 0.5 + \frac{\sqrt{10} - 2}{2(\sqrt{10} - 1)} \tag{13}$$

Therefore, based on the value of D_f, the full power range is divided into four operating conditions as shown in Table 8:

Table 8. Working condition division table of full power range.

Condition	$Power_1$ (Low Power)	$Power_2$ (Medium Power)	$Power_3$ (Quasi-High Power)	$Power_4$ (High Power)
D_f range	$[0, \frac{1-d}{2}]$	$(\frac{1-d}{2}, \frac{1}{2}]$	$(\frac{1}{2}, 0.5 + \frac{\sqrt{10}-2}{2(\sqrt{10}-1)}]$	$(0.5 + \frac{\sqrt{10}-2}{2(\sqrt{10}-1)}, 1]$
Operating mode	$3pSPCPS_tri$	$3pSPCPS_trape$	$3pSPS$	
Optimization	$D_1 = \frac{2d}{1-d} D_f$, $D_2 = \frac{2}{1-d} D_f$	$D_1 = 1 - \frac{(1-d)(1-2D_f)}{d}$ $D_2 = 1$	$D_{3pSPS} = (D_f - 0.5)\frac{0.5 - D_{boundary_3pSPS}}{0.5} + D_{boundary_3pSPS}$	

3.4. Global Operational Improvement Strategy to Suppress Switching Oscillations

In response to the demands of a wide voltage range, a mode-switching scheme is employed. Due to requirements or disturbances, the system may frequently switch modes across various conditions. To minimize the impact of mode-switching oscillations, the system's mode switches can be classified into three types, with the corresponding solutions as follows:

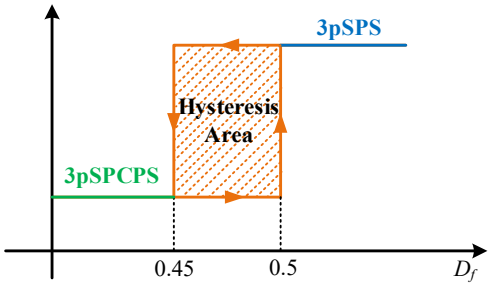
(1) Oscillations during switching between $Power_1$ and $Power_2$ as well as $Power_3$ and $Power_4$ are caused by changes in the mid-segment D_f of the control optimization algorithm. Since D_f is a continuous function during the switch, the impact of oscillations is minimal and can be largely ignored; thus, no further action is taken in this paper.

(2) Oscillations during the switch between medium and low power in $d < 1$ and $d \geq 1$ are caused by changes in the input d of the control optimization algorithm. The switching of d can result in discontinuous branch structures in the optimization algorithm, potentially leading to severe oscillations. At medium and low power, it has been found that soft switching can be achieved under any gain using SPS control when $d = 1$, and the system reliability is very high. Therefore, this paper designs a high-reliability buffer zone in the prone-to-oscillation area, with a specific scheme to operate under SPS control when $0.95 \leq d < 1.05$.

(3) Oscillations between $Power_2$ and $Power_3$ at medium to low power are caused, on the one hand, by the influence of D_f, leading to discontinuous branch structures in the optimization algorithm, and, on the other hand, by the mode switch altering the circuit's topology, thus causing severe oscillations. This paper employs hysteresis control to suppress such oscillations.

The previous analysis identified the power boundaries for 3pSPCPS and 3pSPS as $D_f = 0.5$. Given that the upper power limit of the converter under 3pSPCPS control corresponds to $D_f = 0.5$, the chosen hysteresis region should be less than 0.5. However, a

hysteresis region that is too large is detrimental to the optimized operation of the converter. This paper selects the hysteresis region as $[0.45, 0.5]$, and Figure 6 presents the schematic diagram of hysteresis control switching and its pseudocode for control. When the DAB operates in 3pSPCPS mode and $D_f \geq 0.50$ is detected, the system will switch to the 3pSPS working mode; when the DAB operates in 3pSPS mode and $D_f \leq 0.45$ is detected, the system will switch back to the 3pSPCPS working mode. The introduction of hysteresis control effectively suppresses oscillations caused by mode switching.



(a) Hysteresis Switching Strategy

Hysteresis control pseudocode

Function(Input:D_f **Output:***Mode*)
If *Mode*=0
    if $D_f \geqslant 0.50$ *Mode*=1
Else
    if $D_f \leqslant 0.45$ *Mode*=0
Switch *Mode*
    case 0: *Mode*=3pSPCPS
    case 1: *Mode*=3pSPS

(b) Hysteresis control pseudocode

Figure 6. Hysteresis control scheme.

Although the optimization scheme introduces a hysteresis zone, analysis has found that the power range corresponding to $D \in [0.45, 0.5]$ still falls within the adjustable interlaced power range of 1p-DAB and 3p-DAB, thus the formula does not require correction. After introducing strategies to suppress mode-switching oscillations, the improved control scheme under the requirement for wide boost is shown in Table 9. For cases where the gain under forward power transmission is greater than 1, the reader can derive the conclusion themselves using the analysis process mentioned above. This paper directly presents the conclusion.

Table 9. Wide voltage global unified optimal control scheme under forward transmission power.

Voltage Gain	D_f Range	Condition	Control Mode	Operation Plan
$d < 0.95$	$[0, \frac{1-d}{2}]$	$Power_1$	$3pSPCPS_tri$	$D_1 = \frac{2d}{1-d} D_f$, $D_2 = \frac{2}{1-d} D_f$
	$(\frac{1-d}{2}, 0.45]$	$Power_2$	$3pSPCPS_trape$	$D_1 = 1 - \frac{(1-d)(1-2D_f)}{d}$, $D_2 = 1$
	$(0.45, 0.5]$	hysteresis zone		
	$(\frac{1}{2}, \frac{2\sqrt{10}-3}{2(\sqrt{10}-1)}]$	$Power_3$	$3pSPS$	$D_{3pSPS} = (D_f - 0.5) \frac{0.5 - D_{boundary_3pSPS}}{0.5} + D_{boundary_3pSPS}$
	$(\frac{2\sqrt{10}-3}{2(\sqrt{10}-1)}, 1]$	$Power_4$		
$d \in [0.95, 1.05]$	$(0, 0.45]$	medium and low power level	$1pSPS$	$D_1 = 1, D_2 = 1$
	$(0.45, 0.5]$	hysteresis zone		
	$(\frac{1}{2}, \frac{2\sqrt{10}-3}{2(\sqrt{10}-1)}]$	$Power_3$	$3pSPS$	$D_{3pSPS} = (D_f - 0.5) \frac{0.5 - D_{boundary_3pSPS}}{0.5} + D_{boundary_3pSPS}$
	$(\frac{2\sqrt{10}-3}{2(\sqrt{10}-1)}, 1]$	$Power_4$		
$d > 1.05$	$\left[0, \frac{d-1}{2d}\right]$	$Power_1$	$3pSPCPS_tri$	$D_1 = \frac{2d}{d-1} D_f$, $D_2 = \frac{2}{d-1} D_f$
	$\left(\frac{d-1}{2d}, 0.45\right]$	$Power_2$	$3pSPCPS_trape$	$D_1 = 1$, $D_2 = 2 - d + 2(d-1) D_f$
	$(0.45, 0.5]$	hysteresis zone		
	$(\frac{1}{2}, \frac{2\sqrt{10}-3}{2(\sqrt{10}-1)}]$	$Power_3$	$3pSPS$	$D_{3pSPS} = (D_f - 0.5) \frac{0.5 - D_{boundary_3pSPS}}{0.5} + D_{boundary_3pSPS}$
	$(\frac{2\sqrt{10}-3}{2(\sqrt{10}-1)}, 1]$	$Power_4$		

4. Analysis of DAB Operational Characteristics Under Multiple Working Modes

The previous section presented a standardized, unified operational strategy. This section focuses on analyzing the operational characteristics of said strategy. Considering the need for a wide voltage and power range, this paper categorizes the operational states of the 3p-DAB into low power range, medium power range, quasi-high power range, and high power range (corresponding to $Power_1$, $Power_2$, $Power_3$, and $Power_4$, respectively), with operational control modes divided into 3pSPCPS and 3pSPS. The following analysis will primarily address power characteristics and soft-switching features.

(1) Power Characteristics Analysis

Figure 7 presents the division of the full power range into four operating conditions ($Power_1$ to $Power_4$), along with the corresponding control modes ($3pSPCPS_tri$, $3pSPCPS_trape$, and 3pSPS) and their mapping to different regions of the normalized power index D_f, where the per-unit value P_n satisfies Equation (3). The power coverage range of the traditional 1p-DAB includes $Power_1$ and $Power_2$, while that of the traditional 3p-DAB encompasses $Power_1$, $Power_2$, $Power_3$, and $Power_4$. However, optimization is not achievable due to limitations in control flexibility. This paper utilizes two hybrid control strategies, 3pSPCPS and 3pSPS, with $Power_1$ adopting $3pSPCPS_tri$ control to primarily achieve the optimization objective of minimal current stress and, secondarily, the optimization objectives of minimal reverse power and minimal RMS; $Power_2$ employs $3pSPCPS_trape$ control to achieve the optimization objective of minimal current stress; $Power_3$ and $Power_4$ are controlled by 3pSPS to maintain high power operation. Thus, the operational scheme proposed in this paper not only retains the high-power transmission characteristics of the 3p-DAB under wide voltage conditions, but it also achieves optimization objectives at medium and low power levels.

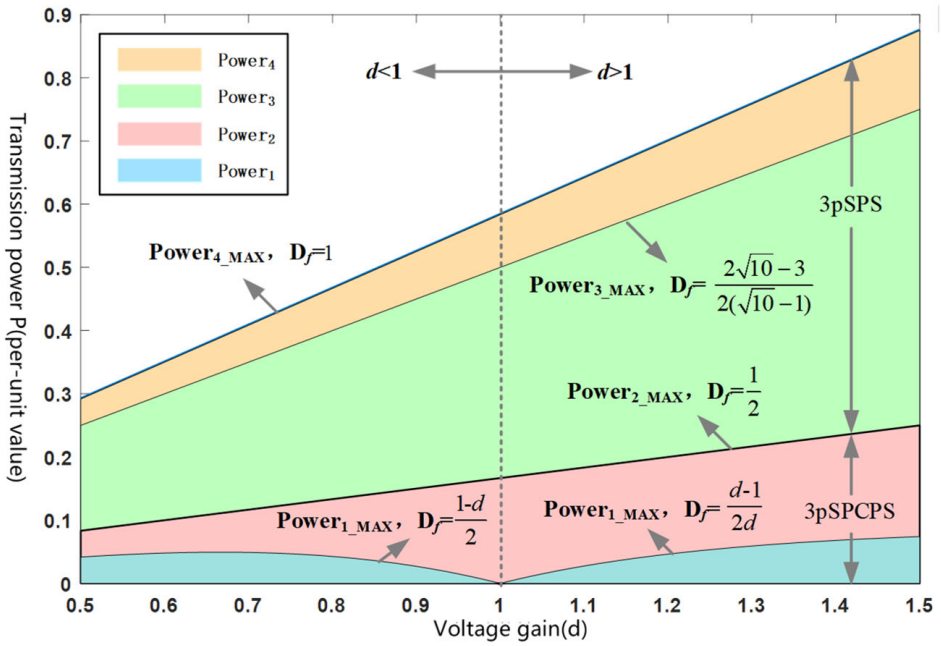


Figure 7. Multi-mode control strategy with power range partitioning under wide voltage conditions.

(2) Soft-Switching Characteristics Analysis

Figure 8 displays the soft-switching region diagram across the global power range under wide voltage conditions, where the per-unit value P_n satisfies Equation (3). As shown in the figure, the blue region represents the ZVS range achievable by conventional 3p-DAB control, which is mainly concentrated in the high-power region. Under conventional control,

the soft-switching range of the 3p-DAB is very narrow at medium and low transmission power levels, and it becomes even more limited as the voltage gain deviates from 1. Full-range ZVS can only be achieved when $d = 1$. The yellow region denotes the ZVS coverage typically realized by TPS-optimized, single-phase DAB (1p-DAB) within its operating power range. The green region indicates the extended ZVS region enabled by the proposed multi-mode control strategy. With the implementation of our strategy, the ZVS capability of the 3p-DAB is significantly expanded into the medium- and low-power regions under a wide voltage range, while the soft-switching characteristics in the quasi-high-power and high-power regions are well preserved. To support the soft-switching design of the converter, the key operating points A, B, C, and D in the ZVS region are further analyzed. Note that point D is not shown in the figure due to scale limitations.

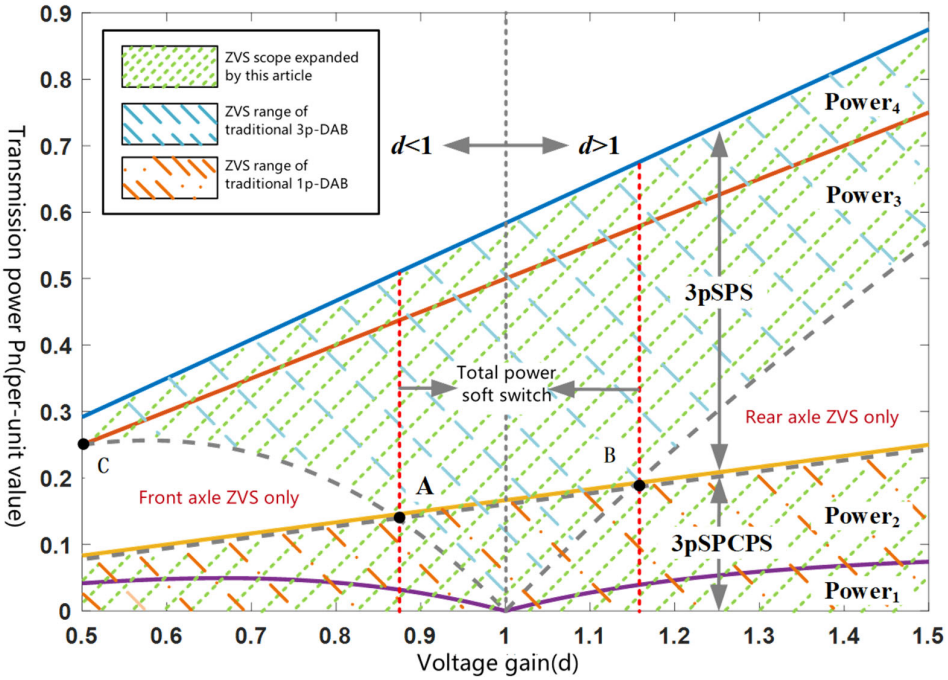


Figure 8. Global power range of a soft-switching area diagram with wide voltage range.

Points A and B: As shown in the figure, the operating region between points A and B can achieve soft switching across the full power range. In the soft-switching design, the voltage gain should overlap with this range as much as possible to reduce the switching losses of the converter. The expression for point A is as follows:

$$\begin{cases} \frac{2-3D_{3pSPS}}{2} = d \\ 2dD_{3pSPS} - \frac{3dD_{3pSPS}^2}{2} = \frac{d}{6} \end{cases} \tag{14}$$

The solution yields that the duty ratio (d) corresponding to point A is $\sqrt{3}/2$.

The expression for point B is as follows:

$$\begin{cases} \left(\frac{2-3D_{3pSPS}}{2}\right) - 1 = d \\ 2dD_{3pSPS} - \frac{3dD_{3pSPS}^2}{2} = \frac{d}{6} \end{cases} \tag{15}$$

The solution yields that the duty ratio (d) corresponding to point B is $2\sqrt{3}/3$.

Therefore, it is recommended to design the voltage gain in the range of $\left[\sqrt{3}/2 \quad 2\sqrt{3}/3\right]$ to meet the soft-switching characteristics across the full power range.

(3) Points C and D: As shown in the figure, points C and D are the intersections of the upper power limit of Y and the soft-switching boundary. When the duty ratio (d) is less than the gain corresponding to point C or greater than the gain corresponding to point D, all soft-switching characteristics are lost below Y, with an extremely narrow range of soft-switching across the full power range. Unless specifically required by the design, it is not recommended to set the voltage gain within this range. The expression for point C is as follows:

$$\begin{cases} \frac{2-3D_{3pSPS}}{2} = d \\ 2dD_{3pSPS} - \frac{3dD_{3pSPS}^2}{2} = \frac{d}{2} \end{cases} \tag{16}$$

The solution yields that the duty ratio (d) corresponding to point C is 1/2.
The expression for point D is as follows:

$$\begin{cases} \left(\frac{2-3D_{3pSPS}}{2}\right)^{-1} = d \\ 2dD_{3pSPS} - \frac{3dD_{3pSPS}^2}{2} = \frac{d}{2} \end{cases} \tag{17}$$

The solution yields that the duty ratio (d) corresponding to point D is 2, but due to scale limitations, this point is not shown in Figure 8.

Therefore, it is not recommended to set the voltage gain in a range less than 0.5 or greater than 2.

In summary, when $d \in [0.5, 2]$, the converter can achieve zero-voltage switching (ZVS) and minimum current stress optimization under the $Power_1$ and $Power_1$ conditions, and ZVS can still be achieved under the $Power_3$ condition. Moreover, when $d \in \left[3/2, 2\sqrt{3}/3\right]$, ZVS remains achievable under the $Power_4$ condition. Compared with traditional PS control, which achieves full-range ZVS only when $d = 1$, the proposed multi-mode control strategy significantly expands the ZVS region and optimization space toward the medium and low power range.

5. Simulation Verification

To verify the correctness of the multimodal switching operation management scheme of the 3p-DAB proposed under a wide voltage range, this paper constructs a simulation model of a three-phase Dual Active Bridge converter on the Matlab/Simulink platform (https://www.mathworks.com/products/simulink.html accessed on 15 May 2025), as shown in Figure 9. The simulation model employs an open-loop control scheme, facilitating the analysis of the 3p-DAB's operation. The overall model comprises five parts: the 3p-DAB circuit's main topological unit, optimization control unit, loop control unit, measurement module unit, and modulation wave generation module unit, with the simulation circuit parameters shown in Table 10.

Table 10. Simulation model system parameter table.

Parameters	Numerical Value
Input voltage U	350 V
Input capacitor C1	2200 μF
Output capacitor C2	2200 μF
High-frequency transformer ration	1.1
3p-DAB leakage inductance La/Lb/Lc	0.25 mH
Switching frequency fs	5.6 kHz

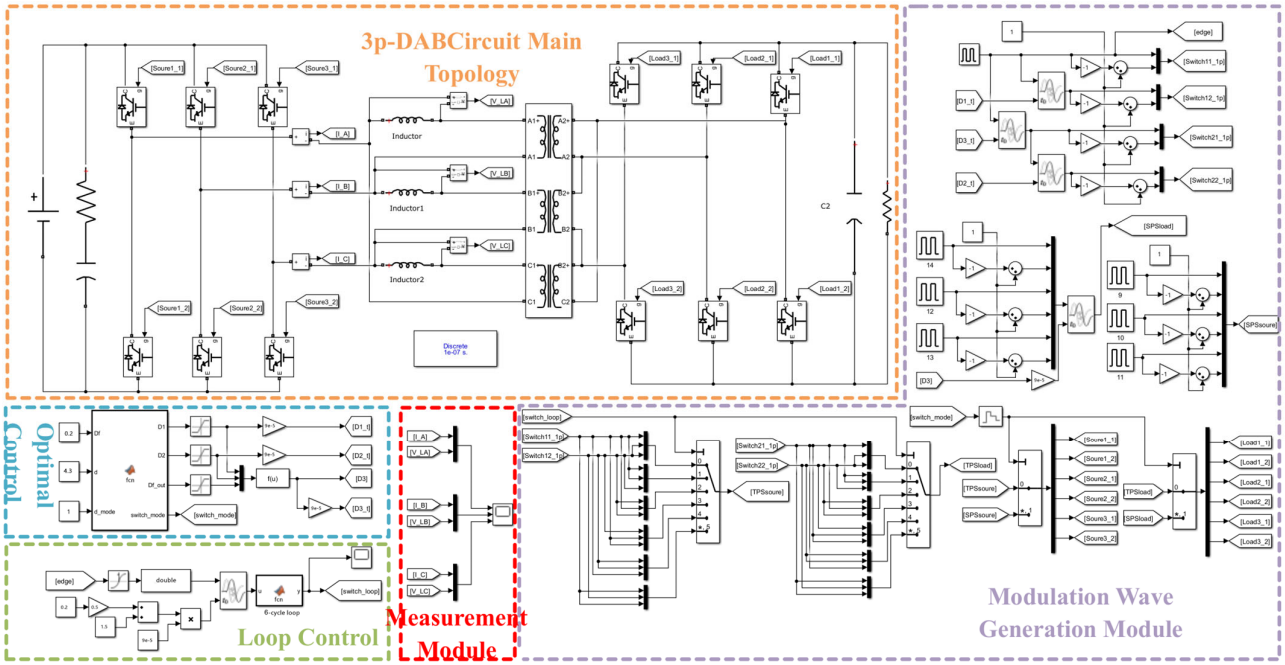


Figure 9. Simulation model of 3p-DAB operation management control based on Simulink.

The proposed control strategy is not limited to a specific converter configuration. It is applicable to various three-phase DAB systems used in practical scenarios, such as vehicle-to-vehicle energy sharing and microgrid interfacing. To reflect real-world application needs, the converter parameters in the experiment are selected based on typical engineering requirements rather than theoretical constraints.

For the 3p-DAB designed for a wide voltage range, this section initially proposes the 3pSPCPS operating mode at medium to low power to achieve similar operational effects to the 1p-DAB. Therefore, this section will first verify the operational effects of the 3p-DAB under this mode and the feasibility of the implementation method. Additionally, the 3p-DAB employs a multimodal operation management approach under four different conditions, so this section will also verify the operational effects of the circuit under multiple modes. The following will detail the simulation situations for these two aspects.

(1) Simulation Verification of the Implementation Effectiveness and Feasibility of the 3pSPCPS Operating Mode

This simulation employs an open-loop verification method, setting the voltage transfer ratio d to 1, the shift ratio D_f to 0.1, and the output load power to 10 kW. Figure 10 displays the output results of the 3p-DAB under the 3pSPCPS operating mode. From the output results, it can be observed that the output voltage is stable at 350 V, and the output current is stable at 28.6 A, consistent with the theoretical analysis of the 3pSPCPS operating mode.

The implementation of the 3pSPCPS operating mode relies on the generation of the correct modulation wave. A critical step is the production of a time cycle control state signal (generated by the cycle control unit shown in Figure 9), as depicted in Figure 11a, where the state information $Mode \in \{0, 1, 2, 3, 4, 5\}$ of a modulation wave changes with each clock cycle. The switching information corresponding to the control in Figure 11a is consistent with the design presented in Table 2. The value corresponding to this mode is then transmitted as a switching control quantity to the modulation wave generation module unit, thereby generating the gate drive signal shown in Figure 11b, and the waveform of this drive signal is consistent with the theoretical design of the 3pSPCPS operating mode.

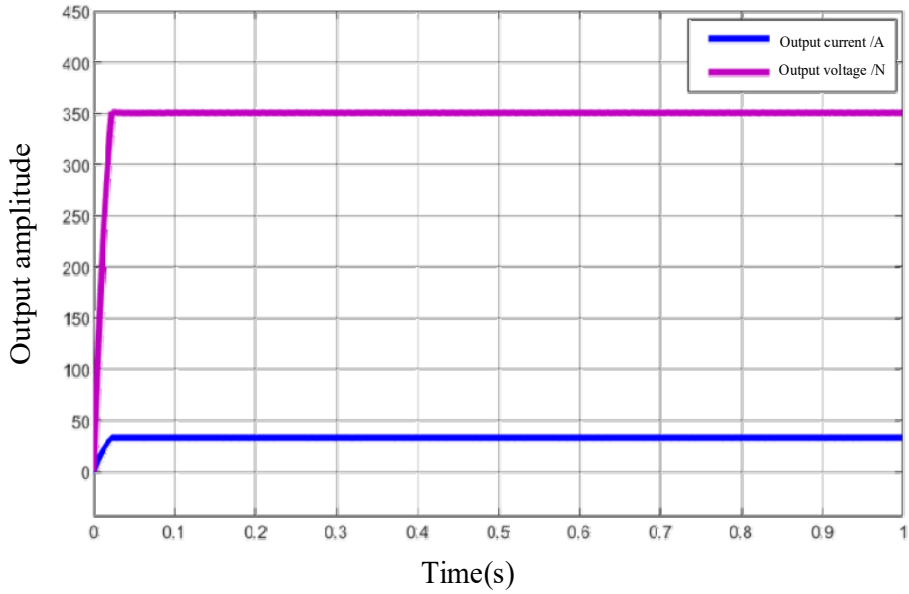
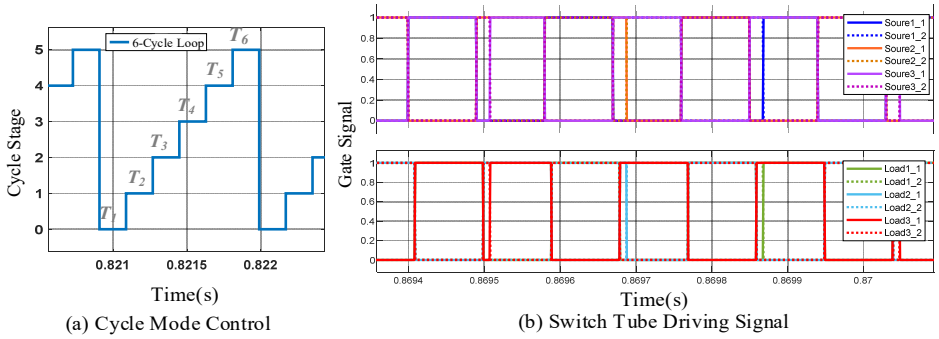


Figure 10. 3p-DAB output results in the 3pSPCPS operating mode.



(a) Cycle Mode Control (b) Switch Tube Driving Signal

Figure 11. Simulation of switching tube drive signal control under 3pSPCPS.

Based on the standardized global unified operation scheme shown in Table 9, with $d \in [0.95, 1]$, this precisely corresponds to the 3pSPCPS operating mode under medium to low power (where the 3p-DAB operates in a manner similar to 1p-DAB controlled by SPS). The voltages across the three-phase leakage inductances and the currents flowing through them, as shown in Figure 12, are highly symmetrical across the three phases, with only a 120° phase-shift present. Furthermore, according to the close-up view, the waveform of the voltage across the inductance and the current, as well as their relationship, conform to the theoretical analysis of DAB operation.

The operational effect of the 3pSPCPS mode can be directly analyzed from the waveform of the three-phase current, with the simulated waveform of the current flowing through the three-phase leakage inductance provided in Figure 13. For each single-phase current, 6T constitutes a cycle. According to the simulation results, i_b lags i_a by 120°, and i_c lags i_b by 120°, which conforms to the relationship of the three-phase current in 3p-DAB. During the T_1 cycle, the current relationship satisfies $i_b = i_C$, $i_a = -(i_b + i_C)$, thus aligning with the analysis of the BC phase parallel operation within the T_1 cycle as per Table 2. A similar analysis can be applied to other cycles. The simulation results show that the three-phase current under the 3pSPCPS operating mode is consistent with theoretical analysis.

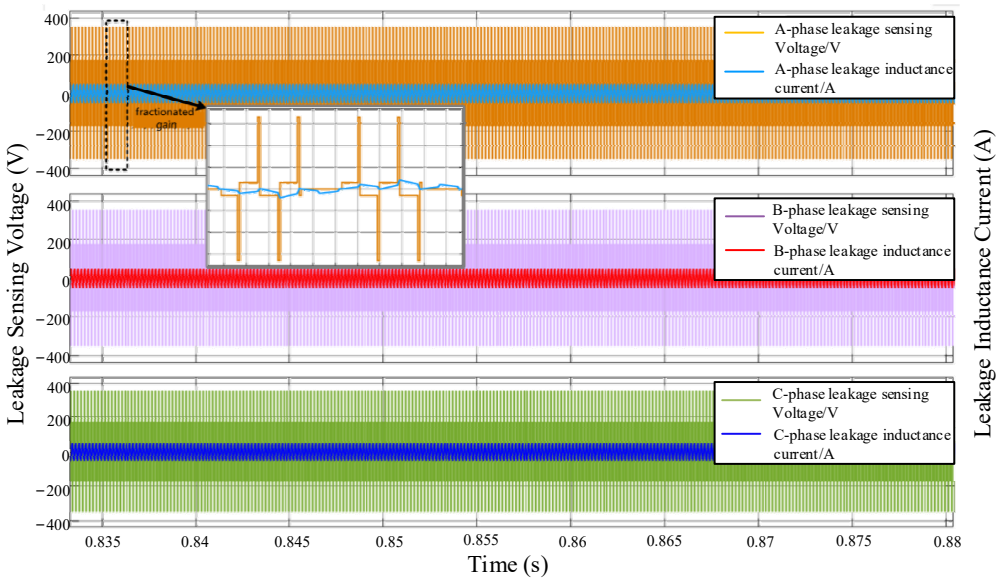


Figure 12. Voltage and leakage current at both ends of the three-phase leakage inductance.

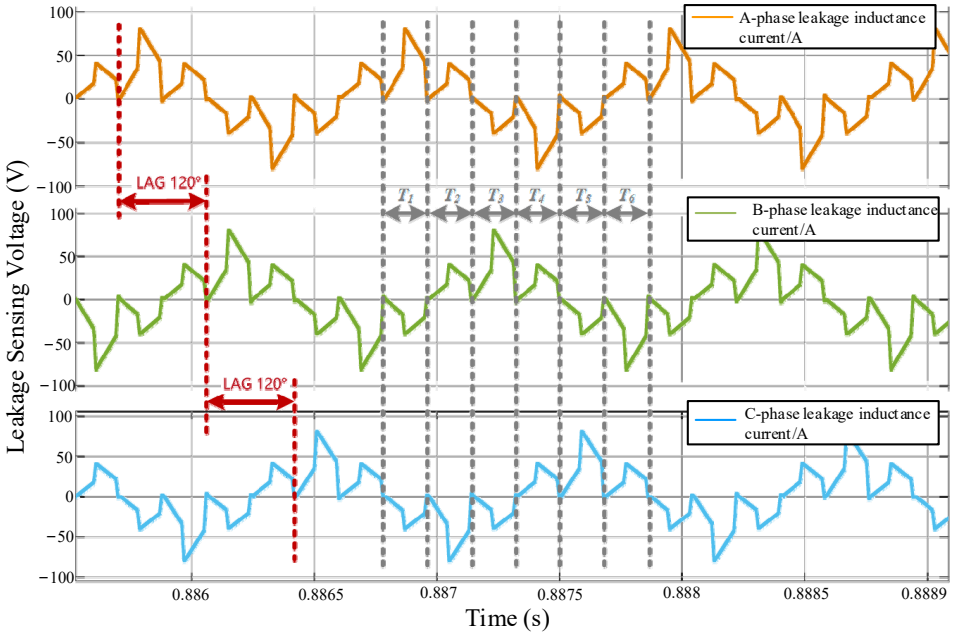


Figure 13. Simulation results of three-phase leakage current.

(2) Simulation Verification of Multimodal Working Effects under Unified Global Operation

When the voltage transfer ratio $d = 0.5$ and $D_f = 0.15$ with an output power of 1500 W, according to the operational conditions outlined in Table 9, the 3p-DAB operates under the Power1 condition in the $3pSPCPS_tri$ mode. Figure 14 shows the circuit operation in the $3pSPCPS_tri$ mode under the Power1 condition, revealing that the inductor current forms a triangular wave, consistent with the theoretical analysis in Figure 5a.

When $d = 0.5$ and $D_f = 0.4$ with an output power of 6000 W, the 3p-DAB operates under the $Power_2$ condition in the $3pSPCPS_trape$ mode, as shown in Figure 15. The inductor current forms a trapezoidal wave, aligning with the theoretical analysis in Figure 5b.

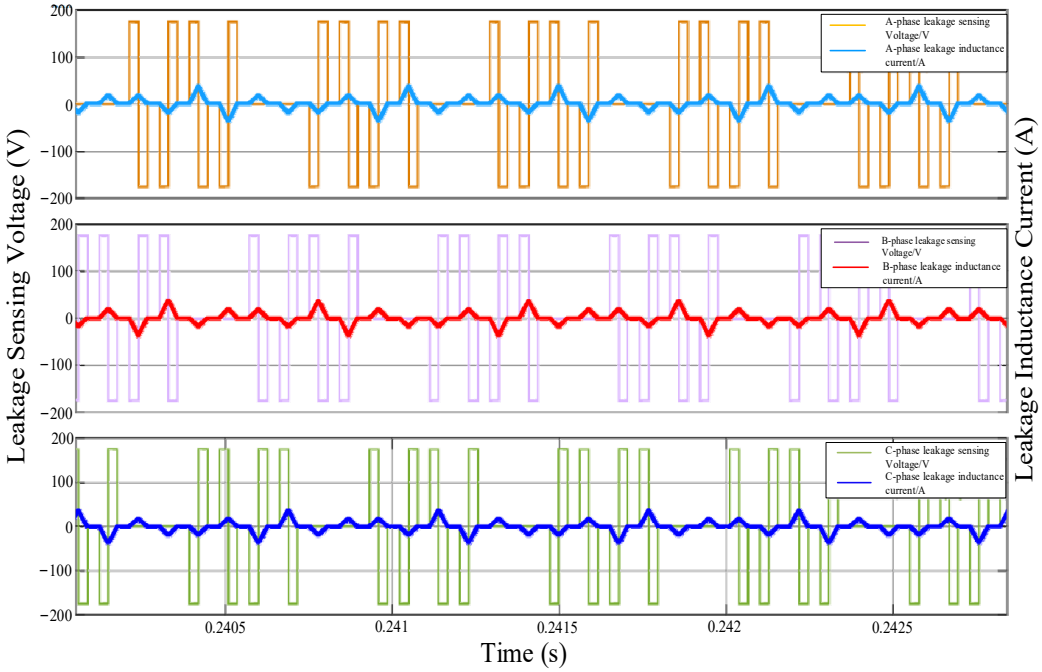


Figure 14. Circuit operation of the 3*pSPCPS_tri* operating mode under the $Power_1$ working condition.

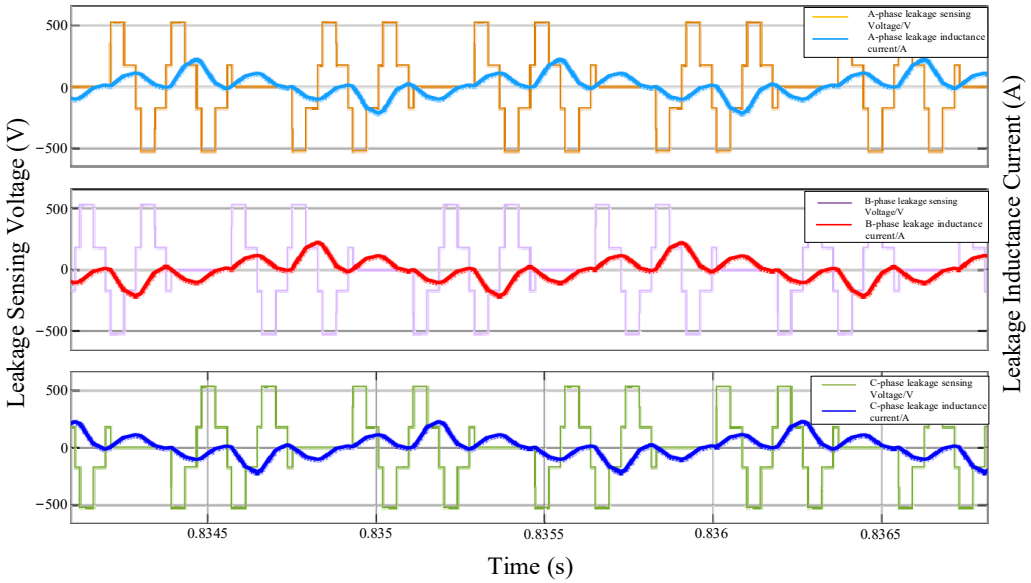


Figure 15. Circuit operation of the 3*pSPCPS_trape* operating mode under the $Power_2$ working condition.

With $d = 0.5$ and $D_f = 0.65$ for an output power of 10,000 W, according to Table 9, the 3p-DAB operates under the $Power_3$ condition in the 3pSPS mode. Figure 16 shows the circuit operation of the 3pSPS mode under the $Power_3$ condition, with the three-phase current waveforms being uniform and a 120° phase delay between adjacent phases.

When the voltage transfer ratio $d = 0.5$ and D_f = 0.85, with an output power of 15,000 W, according to the operational conditions outlined in Table 9, the 3p-DAB operates under the $Power_4$ condition in the 3pSPS mode. Figure 17 shows the circuit operation in the 3pSPS mode under the $Power_4$ condition, with uniform three-phase current waveforms and a 120° phase delay between adjacent phases.

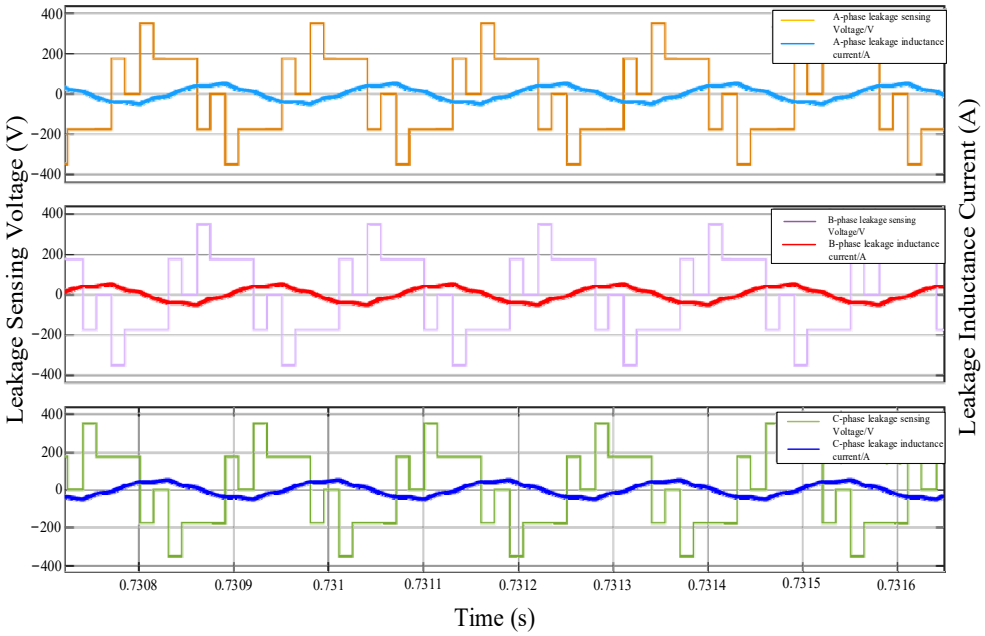


Figure 16. Circuit operation of the 3pSPS operating mode under the $Power_3$ working condition.

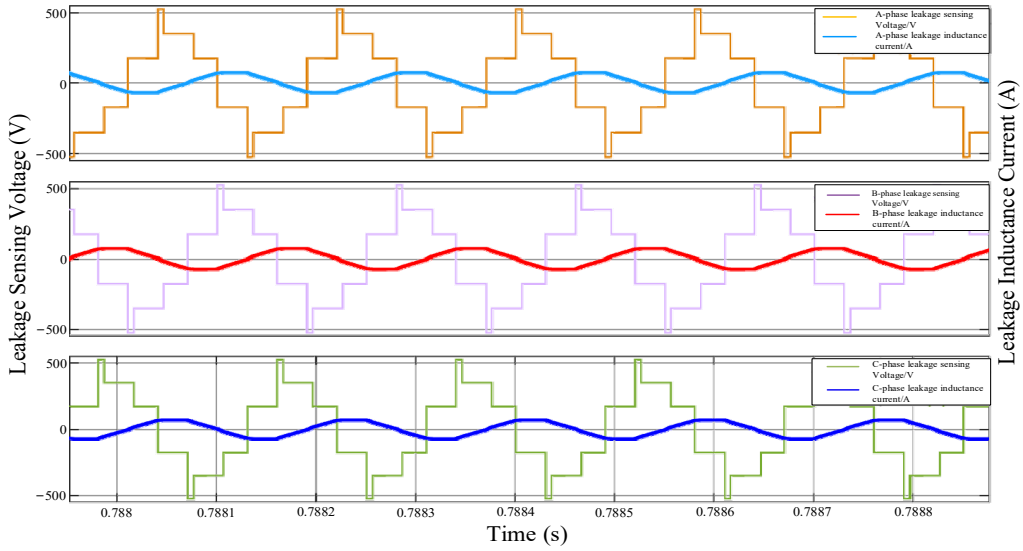


Figure 17. Circuit operation of the 3pSPS operating mode under the $Power_4$ working condition.

The simulation results demonstrate that the 3pSPCPS operating mode proposed in this section enables the 3p-DAB to operate in a manner similar to the 1p-DAB at medium to low power levels, and the circuit's operational conditions are consistent with the theoretical analysis in Section 3.1. Moreover, across a wide voltage range, the simulation results from the four operational conditions for the multimodal operation of the 3p-DAB show that the circuit's operational conditions are consistent with the theoretical analysis in Section 3.2.

6. Experimental Verification

To demonstrate the practical feasibility of the proposed hybrid control scheme for the 3p-DAB, this section first conducts experimental validation based on a HIL (hardware-in-the-loop) simulation platform. The circuit design requirements and parameters refer to Tables 11 and 12, while the platform setup is shown in Figure 18, and the specific laboratory hardware platform is illustrated in Figure 19. The experimental focus of this section is to

verify the effectiveness of the proposed multimodal switching and optimized operation control. Finally, the experimental results are analyzed in detail.

Table 11. Electrical parameter design requirements.

Technical Indicators	Parameters	Technical Indicators	Parameters
System Rated Power:	5 kW	Switching Frequency:	10 kHz
Maximum Transmission Power:	10 kW	Input Voltage:	300 *V*
Input Voltage Overshoot:	<10%	Output Voltage:	150 V–400 V
Input Voltage Droop:	<10%	Output Voltage Ripple Ratio:	<5%

Table 12. Circuit design parameters.

Electrical Parameters	Parameters
Switching frequency:	10 kHz
Number of MOSFETs:	12
Input capacitor C1:	1000 μF
Input capacitor C2:	1500 μF
Leakage inductance L:	140 μH

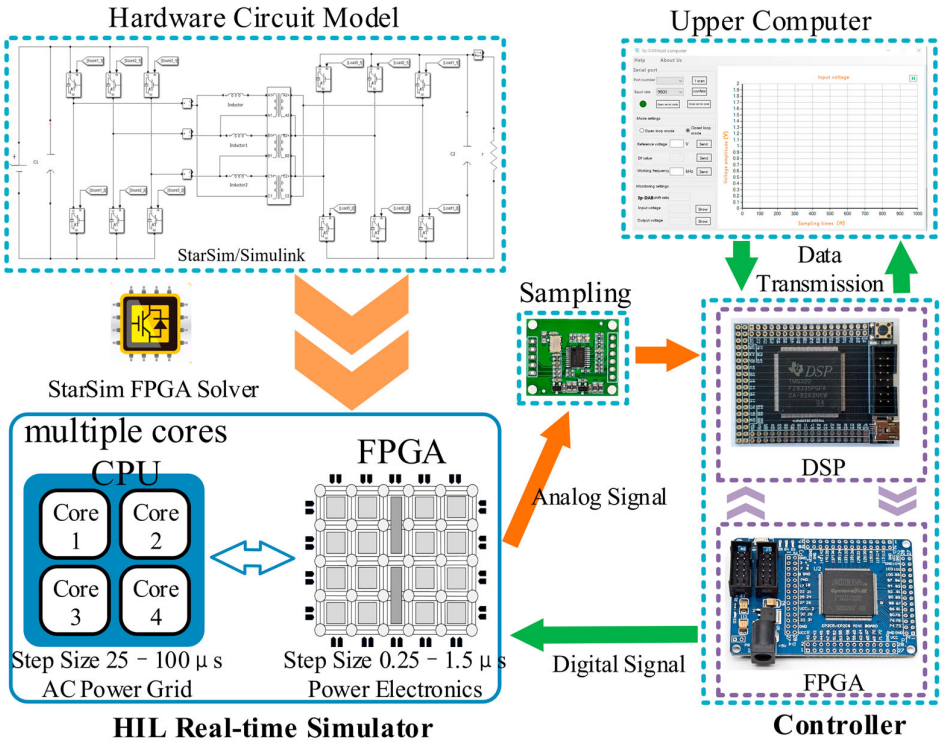


Figure 18. Schematic diagram of a HIL-based experiment.

HIL simulation connects simulated hardware components with real ones, enabling the use of digital models to replace actual system operations. The experimental results obtained through this technique closely resemble those of actual system operations. Moreover, HIL allows for real-time modification of hardware parameters and monitoring, which helps improve the development efficiency of control algorithms. It has been widely used in the development and design verification of circuits [26]. Considering circuit design costs and control algorithm development efficiency, and based on available laboratory resources, a schematic diagram of the experimental platform based on StarSim HIL (ModelingTech Energy Technology Co., Ltd., Nanjing, China) is shown in Figure 18.

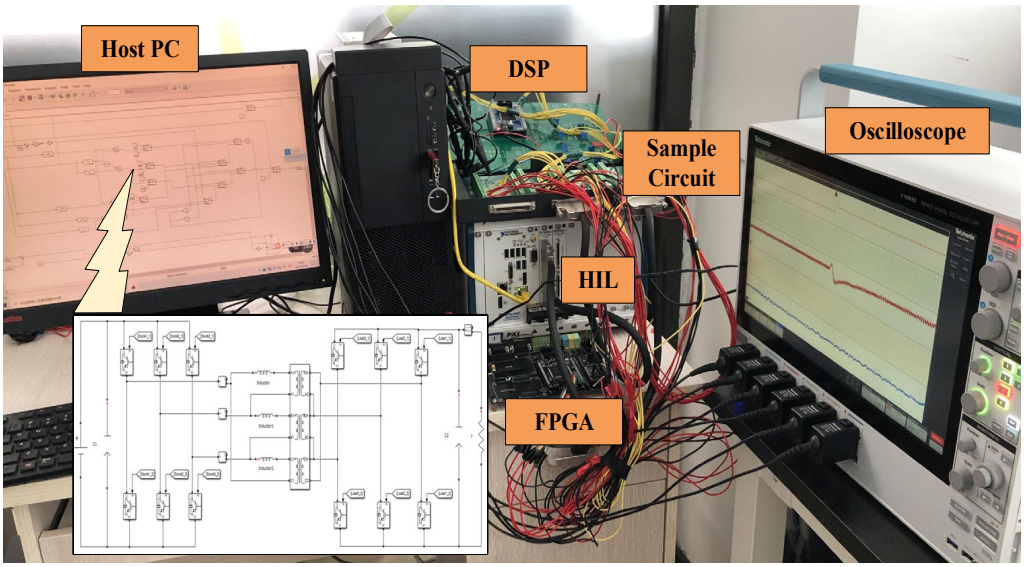


Figure 19. Experimental platform.

The HIL experimental platform is constructed according to the schematic diagram shown in Figure 19. This platform consists of a simulator running the main circuit model and a combined controller composed of a DSP (TMS320F28335) (Texas Instruments Inc., Dallas, TX, USA) and an FPGA (EP4CE10F17C8N) (Intel Corporation (formerly Altera), San Jose, CA, USA). The host configuration parameters are transmitted via the simulator to the sampling circuit, where they are filtered. The DSP then executes the control algorithm, while the FPGA simultaneously performs optimized scheme table lookup, storage, and modulation wave generation. Finally, the drive signals are fed back to the simulator to form a closed loop, and an oscilloscope monitors waveform dynamics in real time.

Next, we conduct a detailed analysis of the experimental results under four operating conditions:

(1) Operating performance of the $3pSPCPS_tri$ mode under Power1 condition:

In this scenario, the open-loop controlled hardware circuit is set with parameters $D_f = 0.15$ and $d = 0.5$, corresponding to the Power1 operating condition. As shown in Figure 20, the experimental waveforms of the three-phase currents and the voltages at the leakage inductance ends are presented. According to the analysis in Section 3.2, the circuit is expected to operate in the $3pSPCPS_tri$ mode. The experimental results show that the three-phase current waveforms exhibit a triangular shape, and the relationship among the three-phase currents aligns with the analysis of the 3pSPCPS mode. The experimental results are very close to the simulation results shown in Figure 14.

(2) Operating performance of the $3pSPCPS_trape$ mode under the $Power_2$ condition:

In this scenario, the open-loop controlled hardware circuit is configured with parameters $D_f = 0.40$ and $d = 0.5$, corresponding to the $Power_2$ operating condition. As shown in Figure 21, the experimental waveforms of the three-phase currents and the voltages at the leakage inductance ends are presented. At this point, the circuit is expected to operate in the $3pSPCPS_trape$ mode. The three-phase current waveforms exhibit a trapezoidal shape, and the relationship among the three-phase currents conforms to the analysis of the 3pSPCPS mode. The experimental results are very close to the simulation results shown in Figure 15.

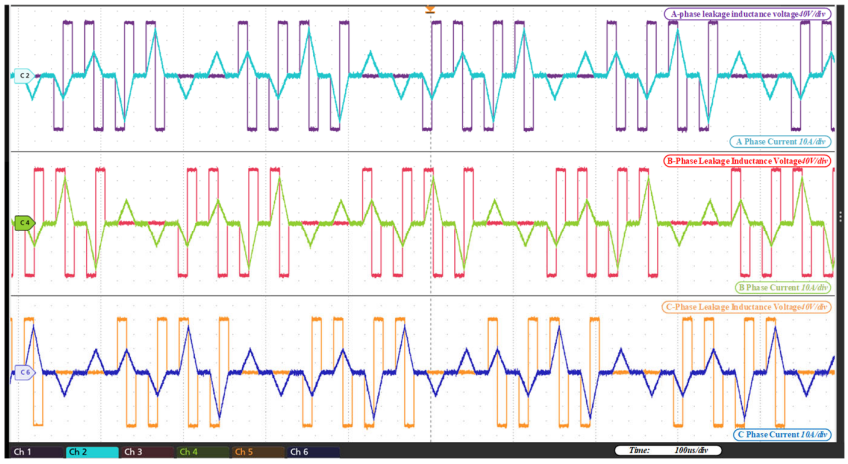


Figure 20. Experimental results of three-phase current and leakage inductance terminal voltage under the $Power_1$ working condition.

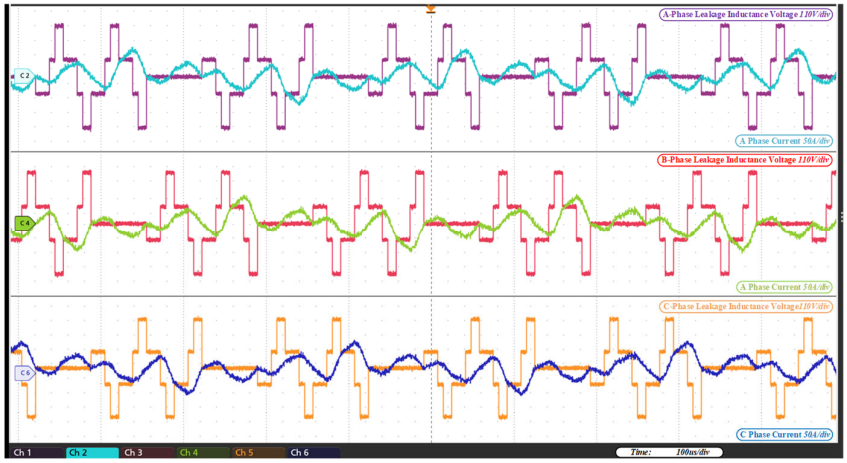


Figure 21. Experimental results of three-phase current and leakage inductance terminal voltage under the $Power_2$ working condition.

(3) Operating performance of the 3pSPCPS mode under $Power_3$ condition:

In this scenario, the open-loop controlled hardware circuit is configured with parameters $D_f = 0.65$ and $d = 0.5$, corresponding to the $Power_3$ operating condition. As shown in Figure 22, the experimental waveforms of the three-phase currents and the voltages at the leakage inductance ends are presented. According to the analysis in Section 3.2, the circuit is expected to operate in the 3pSPCPS mode. The experimental results indicate that the relationship between the three-phase currents conforms to the mode analysis of the conventional SPS control under the condition of $0 \leq D_{3pSPS} \leq 1/3$. The experimental results closely match the simulation results shown in Figure 16.

(4) Operating performance of the 3pSPCPS mode under $Power_4$ condition:

In this scenario, the open-loop controlled hardware circuit is configured with parameters $D_f = 0.85$ and $d = 0.5$, corresponding to the Power$_4$ operating condition. As shown in Figure 23, the experimental waveforms of the three-phase currents and the voltages at the leakage inductance ends are presented. According to the analysis in Section 3.2, the circuit is expected to operate in the 3pSPCPS mode. The experimental results show that the relationship among the three-phase currents conforms to the mode analysis under the conventional SPS control with $1/3 \leq D_{3pSPS} \leq 1/2$. The experimental results are very close to the simulation results shown in Figure 17.

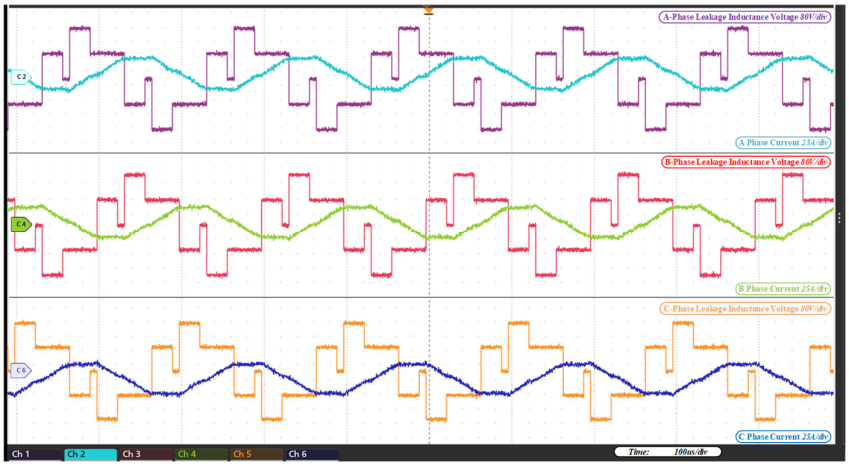


Figure 22. Experimental results of three-phase current and leakage inductance terminal voltage under the $Power_3$ working condition.

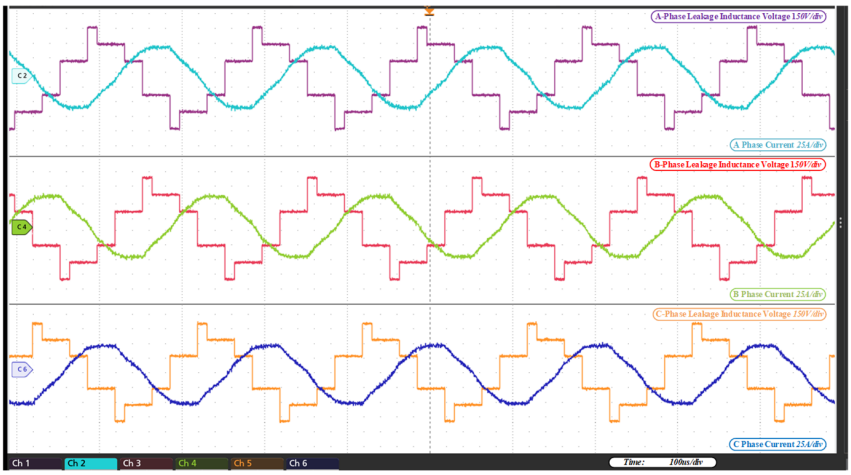


Figure 23. Experimental results of three-phase current and leakage inductance terminal voltage under the $Power_4$ working condition.

As shown above, both the simulation and the experiment have verified the operating characteristics of the proposed control strategy at different power intervals of the 3p-DAB. The two show a high degree of consistency in terms of the output voltage, inductor current waveforms, and the zero-voltage turn-on characteristics under soft-switching conditions. Although there are certain fluctuations and ripples in the experiment, the overall trend is consistent with the simulation analysis, which further verifies the practicality and accuracy of the theoretical model.

7. Conclusions

Firstly, in response to the challenge of achieving soft-switching and targeted optimization under traditional control for the 3p-DAB across a wide voltage range and under medium to low-power conditions, the 3pSPCPS operating mode was introduced to enable the 3p-DAB to function in a manner similar to the 1p-DAB. Subsequently, a standardized global operational strategy was proposed for various conditions within wide voltage applications. This strategy allows the 3p-DAB to operate in the 3pSPCPS mode under medium to low-power conditions to extend the range of soft-switching and minimize current stress, and in the 3pSPS mode under high-power conditions to increase the power transmission limit. Following that, the operational characteristics of this multimodal switching management scheme were analyzed. This optimized operational control not only preserves

the high-power transmission features of the 3p-DAB but also expands the soft-switching range. Finally, through the simulation verification of the 3p-DAB and hardware-in-the-loop simulation, the feasibility of implementing the 3pSPCPS mode and the rationality of the working effects of mode switching under various conditions were demonstrated.

Although the proposed control strategy achieves soft-switching and optimization across wide voltage and power ranges, the current work still has several limitations. First, the analysis is based on idealized component models and assumes a perfectly symmetrical 3-phase DAB topology. Second, the experimental validation is conducted on a fixed-rated 5kW setup, limiting generalization. In future works, the proposed method can be extended to systems with non-idealities such as parasitic capacitance, component mismatches, and thermal variations. Additionally, adaptation to multi-port or modular DAB topologies and implementation on real-time embedded platforms will be pursued to further evaluate the control robustness and practical applicability.

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Nomenclature

Abbreviations Sets and Indices

DAB	Dual Active Bridge
3p-DAB	Three-Phase Dual Ac-tive Bridge
1p-DAB	Single-Phase Dual Ac-tive Bridge
3pSPCPS	Three-Phase Single-Cycle Parallel-Cycle Phase-Shifting
3pSPS	Three-Phase Single-Phase-Shift
TPS	Three-Phase-Shift
SPS	Single-Phase-Shift
EPS	Extended Phase-Shift
APS	Asymmetric Phase-Shift
DCC	Duty Cycle Control
RMS	Root Mean Square
ZVS	Zero Voltage Switching
HIL	Hardware-in-the-Loop
DSP	Digital Signal Processor
FPGA	Field Programmable Gate Array

f	Switching frequency
v'_{cd}, v_{ab}	Reflected secondary-side voltage, Primary-side voltage between nodes a and b
D_1, D_2, D_3	Duty ratios
V_1	Input voltage
L_{S1}	Series leakage inductance
$Mode$	Operating mode selection variable
P_{3pSPS}	Power under 3-phase Single-Phase-Shift control
D_{3pSPS}	Phase-shift ratio in 3-phase SPS mode
$f(D_3)$	A function of the normalized duty ratio D_3
$3pSPS$	3-phase Single-Phase-Shift control
i_a, i_b, i_c	Phase A, B, C current
Decision Variables	
t_3	Switching time instants within a clock cycle
$D_{1\text{opt}}$	On-state duty ratio of switch 1
$D_{2\text{opt}}$	On-state duty ratio of switch 2
D_{fopt}	Optimized virtual phase-shift ratio

Parameters and constants			
T	Switching period	$\hat{d}$	The reciprocal of the voltage gain
D_1, D_2	Primary and secondary duty ratios	$\hat{v}_{ab}$, $\hat{v}'_{cd}$	Primary voltage equals the reflected secondary voltage, Reflected secondary voltage equals the primary voltage
$3pSPC$ PS_tri	Three-Phase Single-Cycle Parallel-Cycling Phase-Shift Control (Triangular Mode)	$\hat{D}_1$, $\hat{D}_2$, $\hat{D}_3$	Mapped duty ratios
$3pSPC$ PS_trape	Three-Phase Single-Cycle ratio Parallel-Cycling Phase- Shift Control (Trapezoidal Mode)	I_b, P_b	Base current for normalization, Base power for normalization
P_{on}	Power delivered during switch-on interval	D_f	Virtual phase-shift (used for mode switching and global unification)
d	Voltage gain	$P_{M_1p\text{-}DAB}$	Maximum power of 1-phase DAB in mode M
$Power_1$, $Power_2$ $Power_3$ and $Power_4$	Low-power region, Medium-power region, Quasi-high-power region, High-power region	$D_{boundary_3pSPS}$	Boundary duty ratio for switching from 3pSPCPS to 3pSPS
		$P_{boundary_high-power-\mathrm{intermediate}-state}$	Power at the boundary of high-power intermediate state

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