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DC/AC/RF Characteristic Fluctuation of N-Type Bulk FinFETs Induced by Random Interface Traps

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Abstract

Three-dimensional bulk fin-type field-effect transistors (FinFETs) have been the dominant devices since the sub-22 nm technology node. Electrical characteristics of scaled devices suffer from different process variation effects. Owing to the trapping and de-trapping of charge carriers, random interface traps (RITs) degrade device characteristics, and, to study this effect, this work investigates the impact of RITs on the DC/AC/RF characteristic fluctuations of FinFETs. Under high gate bias, the device screening effect suppresses large fluctuations induced by RITs. In relation to different densities of interface traps (D_{it}), fluctuations of short-channel effects, including potential barriers and current densities, are analyzed. Bulk FinFETs exhibit entirely different variability, despite having the same number of RITs. Potential barriers are significantly altered when devices with RITs are located near the source end. An analysis and a discussion of RIT-fluctuated gate capacitances, transconductances, cut-off, and 3-dB frequencies are provided. Under high D_{it} conditions, we observe ~146% variation in off-state current, ~26% in threshold voltage, and large fluctuations of ~107% and ~131% in gain and cut-off frequency, respectively. The effects of the random position of RITs on both AC and RF characteristic fluctuations are also discussed and designed in three different scenarios. Across all densities of interface traps, the device with RITs near the drain end exhibits relatively minimal fluctuations in gate capacitance, voltage gain, cut-off, and 3-dB frequencies.

Keywords: bulk FinFETs; characteristic fluctuations; random interface traps; random positions; random numbers; density of interface traps; potential barriers; current densities; short-channel effects; gate capacitances; transconductance; cut-off frequency; 3-dB frequency; 3D statistical device simulation



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1. Introduction

Nowadays, bulk fin field-effect transistors (FinFETs) have become a key technology due to their electrostatic controllability, improved short-channel effect (SCE), and greater

manufacturability compatible with complementary metal-oxide-semiconductor devices (CMOS) [1–3]. Comparing bulk FinFETs with gate-all-around stacked nanosheets and nanowires, bulk FinFETs have the advantage of being low-cost and easy to fabricate due to existing mass-production technology [4,5]. Based on the IRDS roadmap prediction [6], with FinFETs, the trend of CMOS devices will continue to be scaled down to technology nodes less than 5 nm and beyond [7]. For example, they will be used in nodes of 3-nm and 2-nm [8]. Therefore, FinFET will continue to be a viable solution for 3-/2-nm nodes [5,9]. A study of FinFET performance was conducted based on the geometry and size of the fins [8,10–15]. Through the scaling down of device dimensions, comparable improvements can be achieved in terms of power efficiency, variability, reliability, and performance [16,17].

Various randomness sources and process variations [18], such as random discrete dopant (RDD) [19], line edge roughness (LER) [20], and work function fluctuation (WKF) [21–25] of silicon-on-insulator (SOI) and bulk FinFETs have been of great interest. Emerging CMOS technologies have also been critically impacted by the statistical variability caused by random interface traps (RIT) [17,26,27]. It has been known that the single interface trap has a severe impact on the random telegraph noise in the static random access memory (SRAM) with N-/P-type bulk FinFETs [28,29], the bias temperature instability of P-type bulk FinFETs [30], and the radio frequency (RF) of FinFETs [7,31]. In recent research, it was demonstrated that the RITs-induced threshold voltage (V_{th}) and leakage current of JL-FinFETs are larger than those of FinFETs [32]. Further, the position of RITs causes a rather different effect depending on their number and position [33]. Notably, it is important to consider not only DC characteristic fluctuation induced by RITs [34–38] for diverse applications, it is also important to consider the fluctuation of the AC and RF characteristics. It should be noted, however, that recent studies have primarily focused on DC characteristic fluctuation induced by RITs and single-charge traps [32,36,39–41]. There have been many studies on the impact of RITs and single-charge traps on random telegraph noise [42,43] that have found that DC characteristics including threshold voltage, sub-threshold swing (SS), and drain induced the barrier lowering (DIBL) of bulk FinFETs [39,44,45]. This is, however, not the case for the DC characteristics of bulk FinFETs, nor three-dimensional (3D) architectures. In this study, we, for the first time, investigate the impact of RITs on AC and RF characteristics fluctuations under the three different densities of interface traps (D_{it}). Based on a unified statistical 3D device simulation, it will be interesting for us to examine the impact of RITs with differing D_{it} on the DC/AC/RF characteristic fluctuation of bulk FinFETs [16,23,27,36,46].

RIT-induced DC/AC/RF characteristic fluctuations for N-type bulk FinFETs are studied here. In this paper, we investigate the effects of the random position and number of RITs on V_{th} , on-state current (I_{on}), and off-state current (I_{off}) using experimentally calibrated device simulations. A study is then conducted to examine the variations in gate capacitance (C_G) caused by RITs with respect to different D_{it} values. Further discussion will be given to the RIT-fluctuated cut-off frequency (f_T), which is larger than that of the 3-dB frequency (f_{3dB}). As a result of the presence of RITs at the source end, middle end, and drain end of a channel surface, the fluctuations in f_T , f_{3dB} , and C_G are quite different. The following is the organization of this paper. In Section 2, we provide a brief overview of device simulation settings, statistical RIT generation, and device simulation. The results of the study are discussed in Section 3. Lastly, we conclude this study and suggest some future directions.

2. The Statistical Device Simulation

We first brief the simulation settings and accuracy validation prior to the statistical generation of RITs in the large-scale statistical 3D device simulation. To validate our

device simulation by examining the conduction band energy and electron density along the channel during on-/off states, we have numerically solved the three-dimensional density gradient equation along with drift-diffusion (DG + DD) and nonequilibrium Green's functions (NEGF) models. Though not shown here, by adjusting the electron effective mass the DG + DD model's simulation results are in good agreement with those of the NEGF model [46]. In order to achieve the best accuracy of the 3D device simulation, we further calibrated the adopted simulation model with the experimental approach for the bulk FinFET at linear and saturation regimes by adjusting the mobility model and doping level, as shown in Figure 1 [9]. This is calibrated by considering the fourth-generation 16-nm-gate-high- κ metal gate (HKMG) bulk FinFETs.

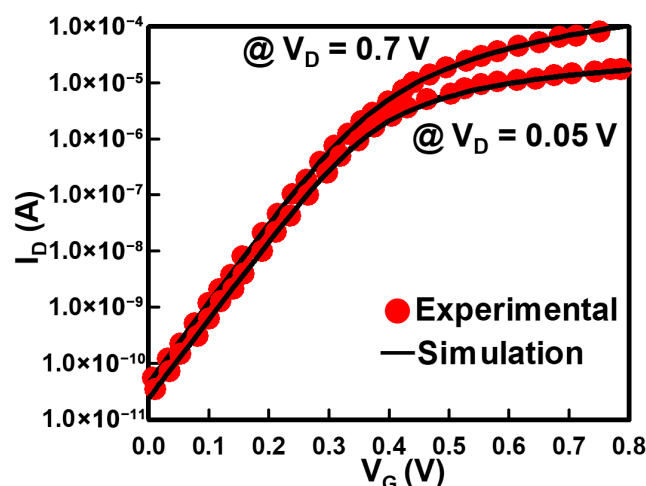


Figure 1. The affirmation of simulated (line) and experimental (symbol) I_D - V_G curves of the 16-nm-gate, $W_{\text{FIN}} = 6$ nm, and $H_{\text{FIN}} = 52$ nm N-type bulk FinFET with tsmc[®] experimental data [9].

Figure 2a illustrates the I_D - V_G characteristics as a function of the channel length (L_G), according to the device parameters listed in Table 1. The inset lists the achieved parameters of SCE, including V_{th} , $I_{\text{on}}/I_{\text{off}}$ ratio, SS, and DIBL, respectively. The V_{th} was extracted using the constant current method, defined at $I_D = W_{\text{FIN}} \times 10^{-7}$ A, ensuring consistency across device geometries. SS and DIBL were also derived based on this criterion under matched bias conditions. The V_{th} roll-off for L_G varying from 16 to 10 nm as shown in Figure 2b. Based on the IRDS projections, $L_G = 16$ nm corresponds to technological nodes below 5 nm (Figure 2b inset) [6]. As shown in Figure 2, there is a serious SCE with regard to device characteristics when L_G decreases [47].

Table 1. List of the adopted parameters of N-type fresh bulk FinFET device and the achieved nominal DC/AC/RF characteristics.

Device Parameter	Value
Channel length (nm) (L_G)	16
Channel doping (cm^{-3})	5×10^{17}
S/D extension (nm)	5
S/D length	12
Fin height (nm) (H_{FIN})	32
Fin width (nm) (W_{FIN})	8
Aspect ratio ($H_{\text{FIN}}/W_{\text{FIN}}$)	4
Work function (eV)	4.52

Table 1. Cont.

Device Parameter	Value
S/D doping (cm^{-3})	1×10^{20}
Density of RITs (cm^{-2})	1.5×10^{12}
Interface trap energy (eV)	0.35–0.55
S/D extension doping (cm^{-3})	4.8×10^{18}
The achieved characteristics of the fresh device and intrinsic RF parameters of a common source amplifier	
Threshold voltage (V_{th}) (mV)	250
Off-state current (I_{off}) (A)	2.86×10^{-12}
On-state current (I_{on}) (A)	6.43×10^{-6}
Gate capacitance (C_G) (aF)	33.37
Voltage gain (dB)	11.82
3-dB frequency (f_{3dB}) (GHz)	35.5
Cut-off frequency (f_T) (GHz)	168

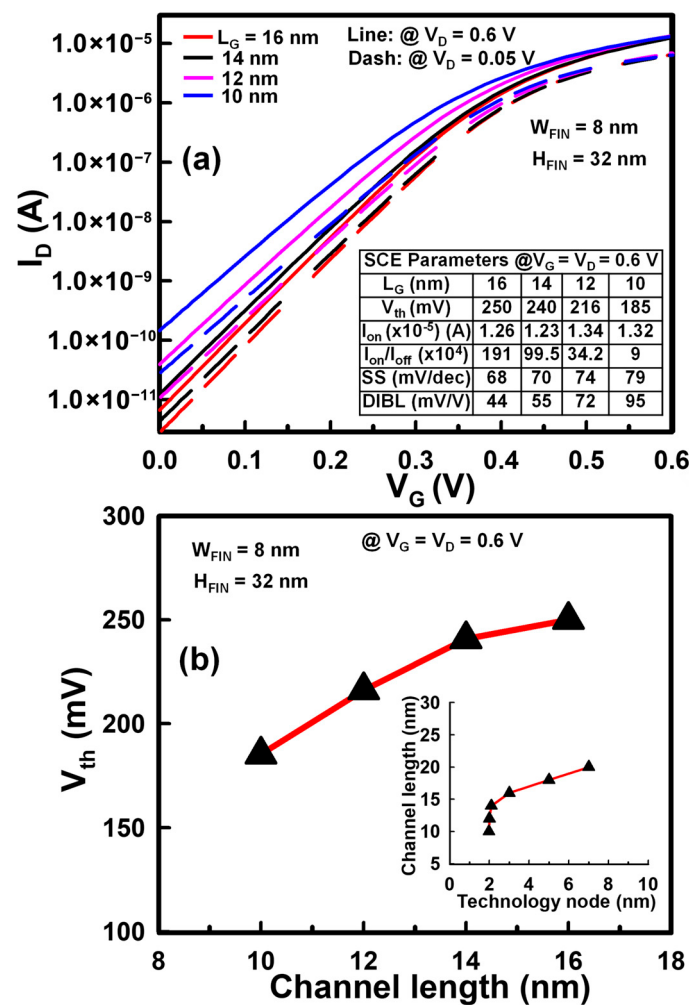


Figure 2. (a) The I_D - V_G characteristics of the explored fresh bulk FinFET device with the channel-length scaling from 16 to 10 nm, where the inset table summarizes the effect of L_G scaling on SCE parameters. (b) A plot of the V_{th} roll-off in bulk FinFETs. The inset in (b) indicates the scaling of gate length across the technology node.

As shown in Figure 3, the explored device has a $\text{SiO}_2/\text{HfO}_2$ stack with an effective oxide thickness (EOT) of 0.963 nm [36] for sub-5-nm technology nodes which are estimated by the formula $\text{EOT} = T_{\text{SiO}_2} + T_{\text{HfO}_2} \times \epsilon_{\text{SiO}_2} / \epsilon_{\text{HfO}_2}$, where $T_{\text{SiO}_2} = 0.6$ nm and $T_{\text{HfO}_2} = 2$ nm are the thickness of gate insulators. Both $\epsilon_{\text{SiO}_2} = 3.9$ and $\epsilon_{\text{HfO}_2} = 22.0$ are the dielectric constants of SiO_2 and HfO_2 . Listed in Table 1 are the parameters of the adopted device, detailed simulation settings, and the characteristics that have been achieved. We have properly incorporated doping dependence, high-field saturation, and impurity scattering mobility models into our device simulation [48]. A non-uniform 3D mesh was employed, with fine discretization (≤ 0.1 nm) near the high- κ/SiO_2 -Si interface to resolve potential fluctuations and trap effects. Boundary conditions included Dirichlet at gate electrodes and Neumann at insulating surfaces, with self-consistent treatment of thermionic emission and tunneling at contacts. Convergence was ensured by solving the coupled Poisson–drift-diffusion–DG equations until relative changes in carrier density and potential fell below 10^{-6} . Mesh refinement studies confirmed that local potential features, including ~ 65 meV peaks, are physical and not artifacts, with variations remaining below 2 meV across refinements. The device has an aspect ratio of 4, 12-nm source/drain (S/D), 5-nm S/D extension, 32-nm H_{FIN} , and 8-nm W_{FIN} [12], as shown in Figure 3a. The device is with a Si-based $\langle 100 \rangle$ surface orientation along the top channel direction and lateral channels are with the $\langle 110 \rangle$ directions [49]. The electron mobility may be enhanced by this orientation [50–52].

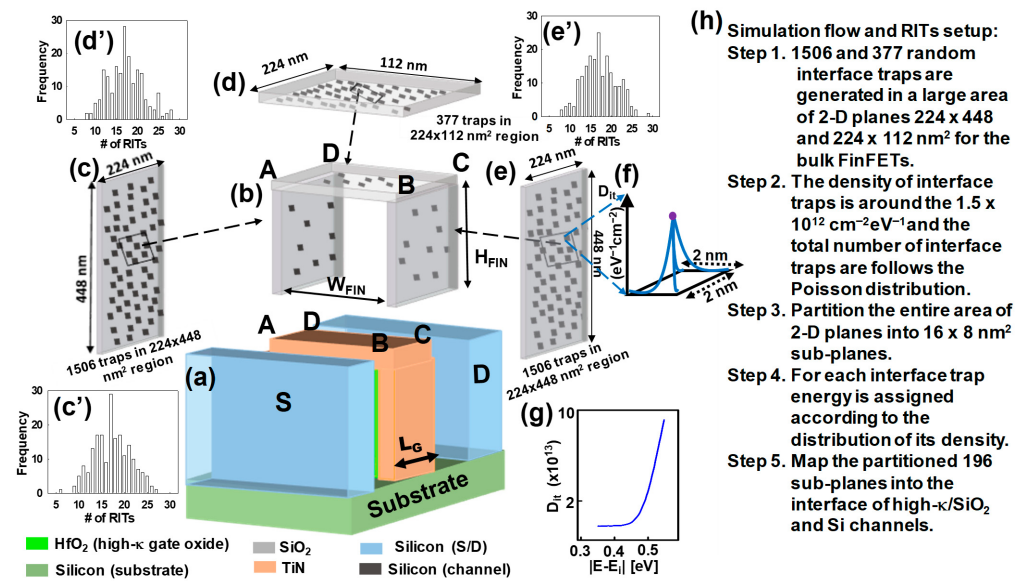


Figure 3. (a) A 3D schematic plot of the bulk FinFET with the gate stack of TiN/high- κ/SiO_2 and Si. (b) The RITs appear at the interface of the gate insulator and channel. (c–e) The three sources of interface traps are generated by using the random process of 1506 and 377 traps in large planes for the bulk FinFETs. The concentration of RITs is around 1.5×10^{12} cm⁻² of all planes and the generated total number of traps and its concentration is driven by the Poisson distribution. (c'–e') The Poisson distribution of the statistically generated RITs for the bulk FinFETs according to each plane. (f) The D_{it} in each plane. (g) The density of trap (denoted as D_{it}) on the plane is assigned according to the distribution of the trap's energy. (h) The stepwise simulation flow of RITs generation and assignment of 196 samples.

As a result of the experimentally validated simulation, we perform a statistical device simulation to explore the DC/AC/RF characteristics of RIT-fluctuated devices. A fresh device is assumed to be free of RITs. In the case of interface trap fluctuation (ITF), all cases of acceptor-like RITs are generated statistically. A total of 1506 traps are generated initially in two large areas of 224×448 nm² for two sides of the bulk FinFET [36], which

is depicted in Figure 3c,e. In all the 2D planes the corresponding concentration of RITs is around $1.5 \times 10^{12} \text{ cm}^{-2}$. Similarly, as shown in Figure 3d, for the top fin, 377 traps are generated in an area of $224 \times 112 \text{ nm}^2$ [53]. All traps are randomly assigned on the interface of the $\text{HfO}_2/\text{SiO}_2$ and Si channel. These interface traps were modeled as surface states defined by D_{it} , and their total number was obtained by integrating D_{it} over the relevant energy range. For numerical implementation, each trap was mapped to a thin volumetric element ($2 \times 2 \times 0.5 \text{ nm}^3$) at the Si/high- κ boundary, serving only as a discretization convenience without altering the physical interpretation of D_{it} . The volume of each trap is $2 \times 2 \times 0.5 \text{ nm}^3$ and there is a range of high, medium, and low levels of D_{it} [54] varying from 5.5×10^{12} to $4 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$, 1×10^{12} to $8 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, and 5.5×10^{11} to $4 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ [44,55–59]; the total number of traps follows the Poisson distribution. The statistically generated RITs standard deviations for three planes are 4.0681, 4.4327 for both side fins, and 2.0241 for the top fin, as shown in Figure 3c',d',e', respectively. Trap energy levels were assigned using a uniform distribution across the mid-gap region, consistent with physical expectations for HKMG interfaces. The selected D_{it} levels—categorized as high ($\sim 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$), medium ($\sim 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$), and low ($\sim 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$)—span the range reported in experimental studies of advanced CMOS processes [55]. This range enables the exploration of both nominal and degraded interface conditions without anchoring the analysis to a specific process corner. The chosen values are representative of typical HKMG process data, and support generalizable insights into trap-induced variability. A step-by-step simulation flow is shown in Figure 3h for the generation and assignment of RITs. The top fin is partitioned into $16 \times 8 \text{ nm}^2$ sub-planes, while the side fins are divided into $32 \times 8 \text{ nm}^2$ sub-planes, as shown in Figure 3c,d,e, respectively. Based on the distribution of trap density, the RITs energy is designated [36,60,61], as shown in Figure 3f,g. It is necessary to continue this process until all sub-planes have been designated. As a result, the 196 devices are generated for statistical 3D device simulations so that we can examine how RITs affect the characteristics of DC devices. Mesh settings and convergence criteria were chosen to ensure numerical stability and physical accuracy, with adaptive refinement applied near the channel and junction regions. A variability sample size of 196 devices was used to achieve statistically meaningful results while maintaining computational efficiency. We use acceptor-type faster traps to detect fluctuations in the AC and RF characteristics of the investigated devices. We have determined that the trap capture and emission cross-sections range from 10^{-14} cm^2 . This is within the acceptable range for silicon devices [55,60]. Statistical 3D device simulations are carried out utilizing the numerical solutions derived from the validated DG + DD model [39,48,62].

3. Results and Discussion

3.1. RITs Impact on DC Characteristics

Figure 4a–a'',b–b'' show the fluctuated I_D - V_G characteristics induced by RITs in semi-log, as well as in linear y -axes under high, medium, and low levels of D_{it} , where the device is operated in both linear ($V_D = 0.05 \text{ V}$) and saturation ($V_D = 0.6 \text{ V}$) regimes, respectively. As shown in Figure 4, the fresh device is indicated by the red lines. In proportion to the level of D_{it} , the magnitude of ITF increases. It is observed that RITs have a severe effect at low gate bias. By raising the gate bias, electrons in the channel can depart from the trap, thereby reducing fluctuations. With the gate bias increased, however, the RIT-induced fluctuations are diminished for all levels of D_{it} , since the inversion charge fills the interface states and reduces their impact. Accordingly, the high gate voltage reduces the characteristic fluctuation for all devices. Thus, significant characteristic fluctuations are observed at the off-state current under high D_{it} levels. Due to the random location and density of RITs, the energy barrier is vigorously stirred, resulting in relatively expanded

fluctuations below the threshold voltage. Consequently, the high level of D_{it} RITs located in the middle of the channel and near the S side has a significant impact on the energy barrier. The number of RITs increases, and the penetration of the electric field from D to S decreases, thereby decreasing the SCE of the device. The I_D - V_D characteristic fluctuation under three levels of D_{it} and its major derivatives of the bulk FinFETs induced by RITs have been carried out, as depicted in Figure 4c–c'' under the different gate bias. In addition, we observe that the output characteristic fluctuates significantly at high gate voltages ($V_G = 0.6$ V). Nevertheless, the ITF I_D fluctuation is governed by the high level of D_{it} . Accordingly, a significant variation in I_D was observed (>50%) for the high-level D_{it} under $V_D = V_G = 0.6$ V. The fluctuated g_d - V_D characteristics with varied gate voltage induced by RITs under three levels of D_{it} are shown in Figure 5a–a''. Figure 5b–b'' illustrate the fluctuated g_m - V_G characteristics associated with RITs under the three levels of D_{it} . The g_m of semiconductor devices is an important parameter, which alters the gain of an amplifier. However, under high levels of D_{it} , there are severe g_m fluctuations. Figure 6a illustrates the relationship between $g_{m,max}$ and RITs under the different levels of D_{it} . The $g_{m,max}$ decreases as the number of RITs increases. In the presence of a high level of D_{it} , it is evident that there is more scattering of $g_{m,max}$. A reduction in drain current caused by the increase in RITs results in a reduction in $g_{m,max}$. Figure 6b depicts the fluctuating $g_{d,max}$ for the number of RITs and the three levels of D_{it} ; a reduction in $g_{d,max}$ is associated with the number of RITs. Therefore, as expected, the $g_{d,max}$ is much more scattered under the conditions of level of high D_{it} . It has been realized that multiple traps can cause enormous fluctuations, owing to their multiple conduction carrier captures and emission events. As a result, the performance of the device will be adversely affected.

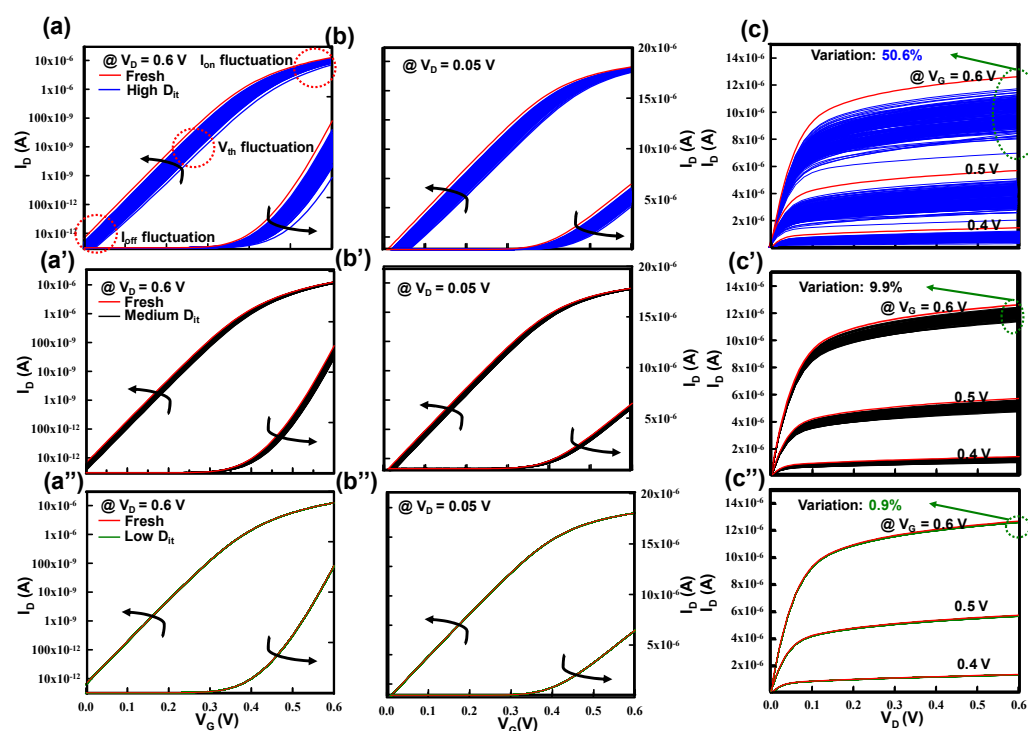


Figure 4. (a–a'') The RITs fluctuated I_D - V_G curves of the device at $V_D = 0.6$ V with respect to the high, medium, and low levels of D_{it} , respectively, where the red line indicates the I_D - V_G curve of fresh device. Similarly, (b–b'') the RITs fluctuated I_D - V_G curves of the device at $V_D = 0.05$ V. (c–c'') The RITs fluctuated I_D - V_D characteristics. The variation percentage is calculated by $(6\sigma/\mu) \times 100\%$, where σ is the standard deviation, and μ is the average value.

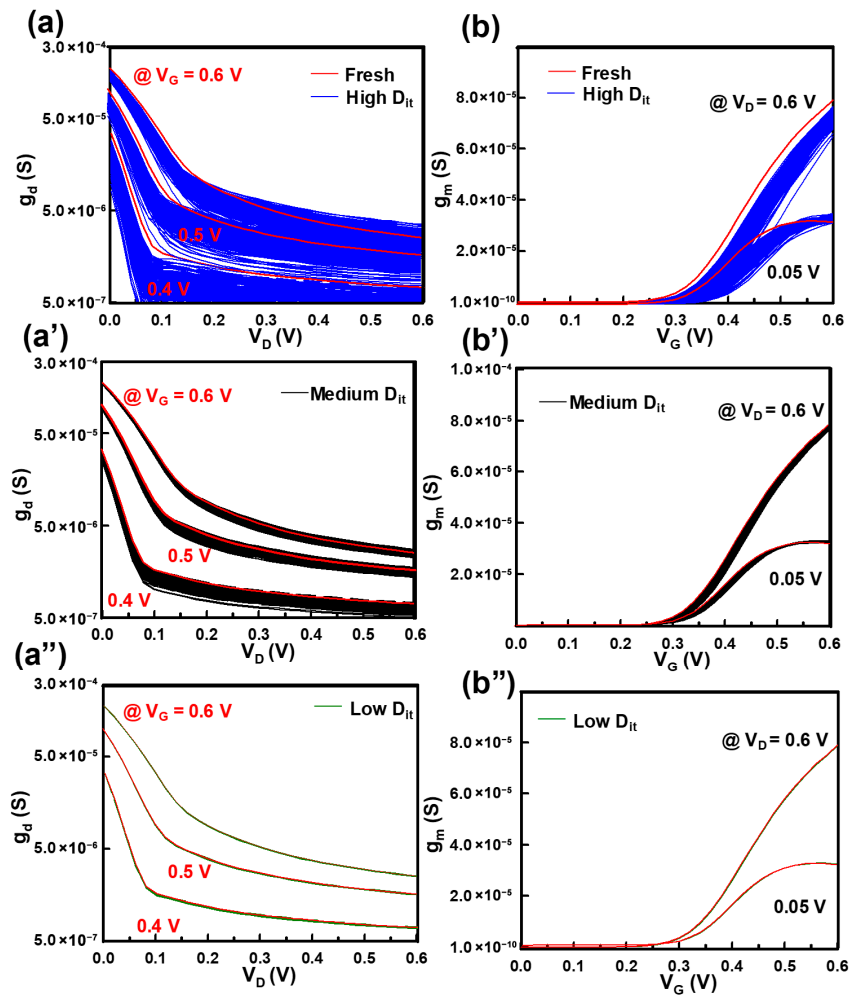


Figure 5. (a–a'') The fluctuated g_d - V_D characteristics of high, medium, and low levels of D_{it} under the various gate biasing conditions. (b–b'') The fluctuated g_m - V_G characteristics under the linear and saturation regimes for three varieties of D_{it} .

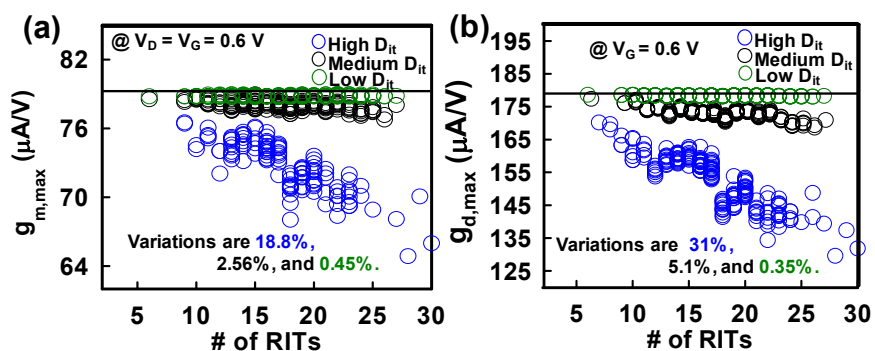


Figure 6. (a) The $g_{m,max}$ fluctuation versus the number of RITs at the $V_D = V_G = 0.6$ V for the three levels of D_{it} , where the black line indicates the $g_{m,max}$ of the fresh device. (b) The $g_{d,max}$ fluctuation versus the number of RITs at the $V_D = V_G = 0.6$ V for the three levels of D_{it} , where the black line represents the $g_{d,max}$ of the fresh device.

3.2. Significance of Interface Trap Random Position

Figure 7a'–a''' show the fluctuating V_{th} versus the number of RITs under $V_D = V_G = 0.6$ V at three levels of D_{it} , with the black line indicating the fresh device with $V_{th} = 250$ mV. A significant fluctuation in V_{th} is observed as a result of an increased number of RITs occurring under a high level of D_{it} . In addition, we investigate the effect of the random

position and number of RITs on the variability of V_{th} of bulk FinFETs at high level of D_{it} [63]. This is in agreement with the result reported in [33], where Wang et al. argued that the RIT-induced V_{th} is larger than our work under the medium D_{it} . Based on the high level of D_{it} , we have shown in Figure 7a' that both Cases A and B represent similar numbers of RITs but different V_{th} , and both Cases B and C represent similar V_{th} but different numbers of RITs. To explore this phenomenon, we extracted electrostatic potentials corresponding to Cases A, B, and C, respectively, on the channel surface from S to D, as illustrated in Figure 7a–c. Due to the position of the RITs, distinct characteristic fluctuation was observed, despite the same number of RITs. Our results in Figure 7a,b demonstrate that Case A has a significant V_{th} compared to Case B when a similar number of RITs were analyzed with different random positions. Thus, Case A shows a greater number of RITs, as more RITs are positioned near the middle and S of the channel, as shown in Figure 7a₁. The devices with RITs near the S and middle of the channel are, however, confirmed to have reduced immunity. In comparison with other locations, these RITs can be enhanced to address more potential barriers. In addition, Figure 7b illustrates the electrostatic potential with a similar number of RITs but a lower V_{th} . The effect of RIT position is estimated in terms of electrostatic potential along the channel, which shows that the RIT-induced potential barriers are reduced in Case B when fewer RITs are located near S and at the middle of the channel. Therefore, it has a lower V_{th} than Case A. Furthermore, both Cases B and C have the same value of V_{th} and different numbers of RITs, as shown in Figure 7b,c. Accordingly, Case C has fewer RITs than Case B, but most of them are located near the S and middle of the channel. As a result, RIT fluctuations will increase in a similar manner to Case B. This is evident by observing the 1D electrostatic potential energy versus channel position along with the S to D direction of three cases, as shown in Figure 8a–c for the three levels of D_{it} , respectively. Therefore, for Case A near S, the electron encounters the high barrier, which results in Case A having a large V_{th} , in comparison with other cases, as shown in Figure 8a. Therefore, the RITs positioned distant from the S have depleted interaction with mobile electrons owing to the moderately higher drift velocity and electron transport energy, and several local spikes of potential barriers still effectively obstruct surface current conduction, which is even more substantial than that of RITs presenting near the S. Therefore, the achieved results indicate that RITs placed at random in bulk FinFETs could be an effective choice. Accordingly, the medium and low levels of D_{it} have reduced potential barriers than others, as shown in Figure 8b,c, further reducing fluctuations in the V_{th} . Additionally, Figure 7a₁'–a₃' illustrate the 3D charge density of Cases A, B, and C, respectively. It is evident that the charge density increases as the value of the V_{th} is reduced.

Figure 9 illustrates the fluctuated subthreshold slope (SS) versus the number of RITs for the three levels of D_{it} . In the context of three levels of D_{it} , SS increases as the number of RITs increases. SS degradation becomes more critical when the level of D_{it} is high. Under the three levels of D_{it} of bulk FinFETs, Figure 10a'–a''' demonstrate the fluctuated I_{off} versus I_{on} characteristics induced by RITs. Figure 10a''' illustrates a fresh device by a filled red circle. I_{off} and I_{on} are reduced as a result of the increased number of RITs. In particular, the RITs-induced fluctuation variation $((6\sigma/\mu) \times 100\%)$ of I_{off} (145%) is higher than the I_{on} (40.9%) for the high level of D_{it} . This is due to the inversion charges filling the interface states and screen their impact, as shown in Figure 10a'. Figure 10a,b demonstrate a comparison of I_{off} and I_{on} with the random position effect of RITs at high D_{it} levels. RIT positions were randomly distributed across all three cases, associated with a local repulsive coulomb field and disturbed surface current-conducting directions in cases A, B, and C. Furthermore, both Cases A and B exhibit similar I_{on} but different I_{off} , as shown in Figure 10a,b. Due to the presence of fewer RITs near the middle and S of the channel in Case A, the leakage is less than in Case B, as shown in Figure 10a₁. In addition, their I_{off}

differs since RITs positioned near the S and middle of the channel result in a moderately higher spike of the potential barrier and a higher V_{th} , in comparison to RITs positioned near the D. As well, Case B has the same RITs as Case A, but many of the RITs are located in the vicinity of S and the middle of the channel, which is the opposite of Case A. As a result, it has a similar density of on-state current to Case A. Both Cases B and C have similar I_{off} and different I_{on} , so the on-state current densities are obtained at the surface of the channel, as shown in Figure 10b,c. It can be seen from both cases that Case C has a higher number of RITs. In contrast to Case B, Case C has a low on-state current. RITs have been shown to induce on-state current densities that are related to the number of RITs and the position of those RITs. Therefore, the RITs positioned distant from the S have depleted interactions with mobile electrons owing to the moderately higher drift velocity and electron transport energy. In addition, several local spikes of potential barriers continue to effectively obstruct surface current conduction, which is even greater than that encountered by RITs near the S. Moreover, Figure 10a₃–c₃ illustrate the off-state current densities for each case under high D_{it} levels.

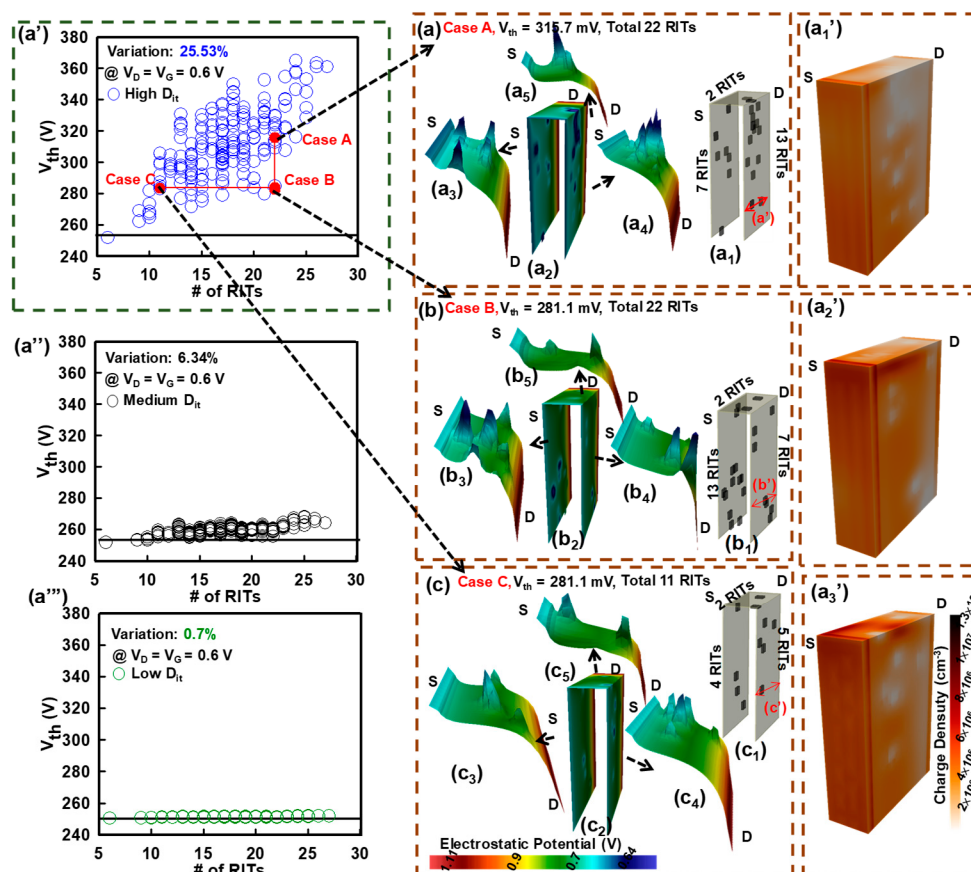


Figure 7. (a'–a''') RITs fluctuated V_{th} versus the number of RITs under the three levels of D_{it} , where the black line represents the fresh device V_{th} . In Figure (a'), both Cases A and B are the same number of RITs, but different values of V_{th} , and both Cases B and C are the same value of V_{th} but different number of RITs for the random position and number effect, respectively. (a–c) are the simulated devices' electrostatic potential according to Cases A, B, and C, respectively. (a₁–c₁) All the device channel regions under the presence of RITs. (a₂–c₂) Devices at on-state ($V_D = V_G = 0.6$ V) electrostatic potential are extracted at the surface of the channel. The corresponding on-state electrostatic potential of (a–c) are shown in (a₂–c₂), respectively. (a₃–c₃) and (a₄–c₄) are the extracted electrostatic potential of all the side fins of Cases A, B, and C. (a₅–c₅) are the electrostatic potential of the top fins of the three Cases, respectively. (a₁'–a₃') are the plots of the corresponding 3D charge density of the Cases A, B, and C in the channel, respectively.

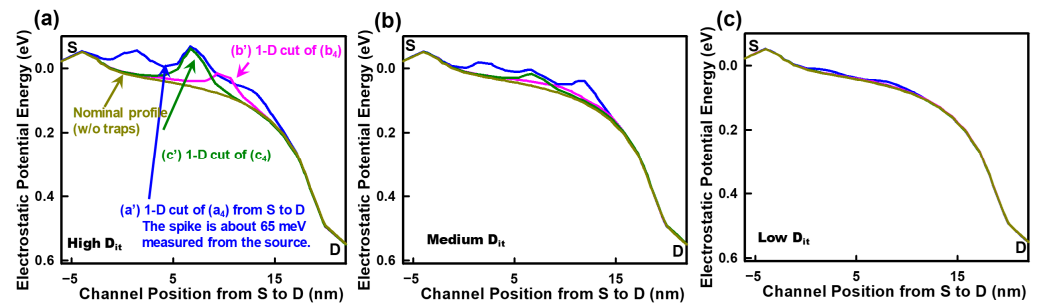


Figure 8. (a) The RITs fluctuated 1D cut (a'–c') from Figure 7 electrostatic potential energy versus channel position from S to D of the Cases A, B, and C under the high D_{it} , respectively. Similarly, (b) and (c) are the medium and low levels of D_{it} electrostatic potential profiles.

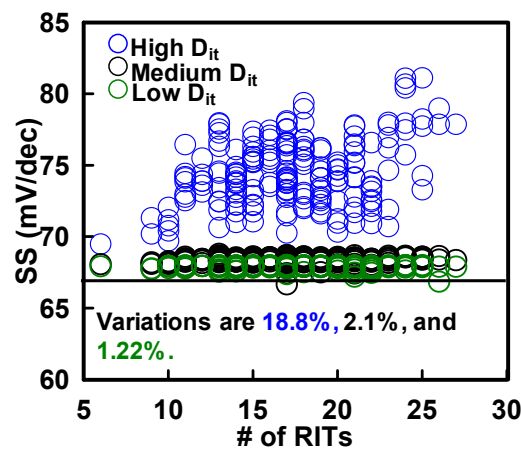


Figure 9. The RIT fluctuated subthreshold slope versus the number of RITs for the three levels of D_{it} , where the black line indicates the subthreshold slope value of fresh device.

3.3. Impact of RITs on Drain Current Mismatch

Figure 11a–c show the RIT-induced fluctuated drain current mismatch versus gate voltage of the investigated devices [64]. Normally, the mismatch is calculated from the linear difference between two drain current values of fluctuated devices; that is $\Delta I_D/I_D = (I_{D,j+1} - I_{D,j})/I_{D,j}$, where $I_{D,j+1} - I_{D,j}$ are two arbitrary adjacent drain currents for $j = 1, \dots, 196$. In fact, the drain current is mismatched for small changes in two drain currents as a result of trap capture and emission at the interface. A noteworthy point is that, in the high D_{it} , the variability is higher than in the other levels. Specifically, the low D_{it} has almost no mismatch. However, the RITs, which are acceptor-like traps, can capture electrons in the channel, resulting in an improvement in the mismatch at three levels of D_{it} . Moreover, the increase in RITs also results in a significant increase in the mismatch. For medium and low D_{it} values, using the standard linear difference of drain current may result in almost zero. Figure 12 illustrates the calculation of the standard deviation of the drain current mismatch $\sigma(\Delta I_D/I_D)$ versus the gate voltage, normalized by $(W_{FIN} \times L_G)^{1/2}$ [65]. For the high D_{it} , we observe that the normalized standard deviation of drain current mismatch is significant. Furthermore, because of the increased conduction in the channel at gate voltages above the V_{th} region, the standard deviation of drain current mismatch is significantly higher than in other regions.

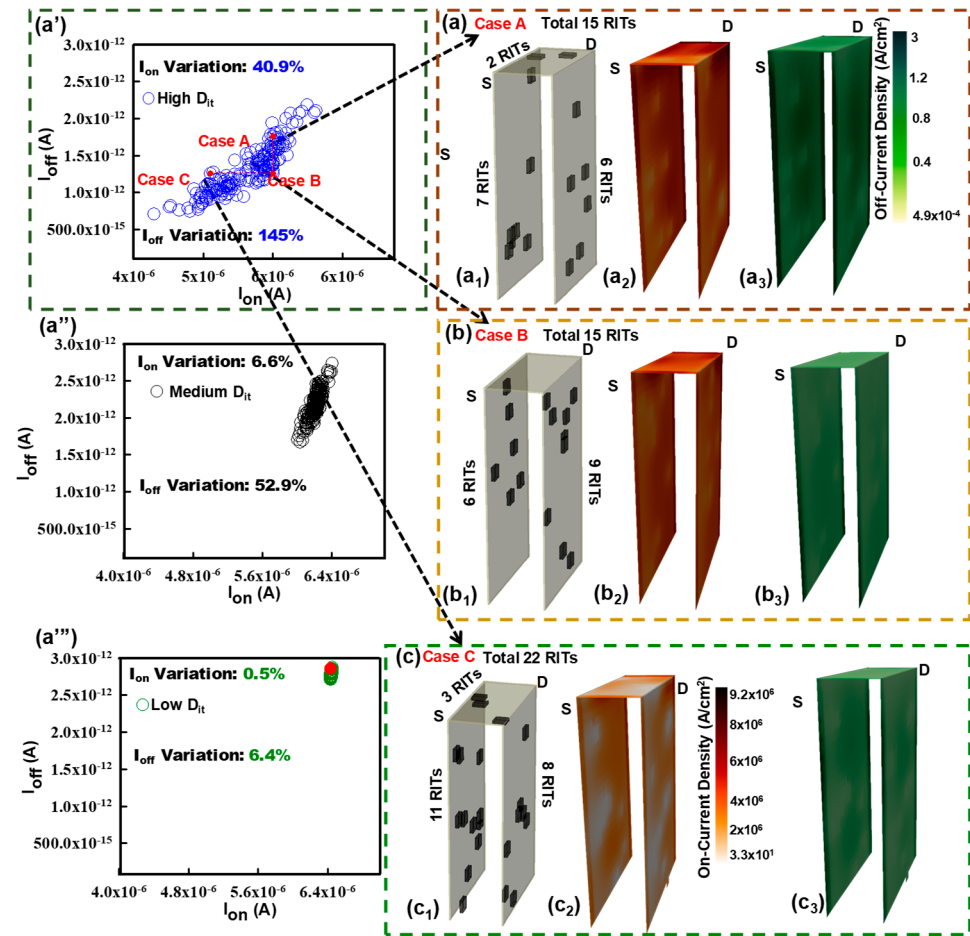


Figure 10. (a'–a''') The RITs fluctuated I_{off} versus the I_{on} of the bulk FinFETs under the three levels of D_{it} . The red-filled circle in (a''') indicates the fresh device. (a,b) are under the high level of D_{it} for the random position effect both Cases A and B under the similar I_{on} but different I_{off} . (b,c) are the random number effects of RITs, both Cases B and C with similar I_{off} but different I_{on} . (a₁–c₁) All the devices channel regions under the presence of RITs. (a₂–c₂) All the cases' on-state ($V_D = V_G = 0.6$ V) current densities are extracted at the surface of the channel. (a₃–c₃) The channel surface off-state current ($V_D = 0.6$ V and $V_G = 0$ V) density of Cases A, B, and C, respectively.

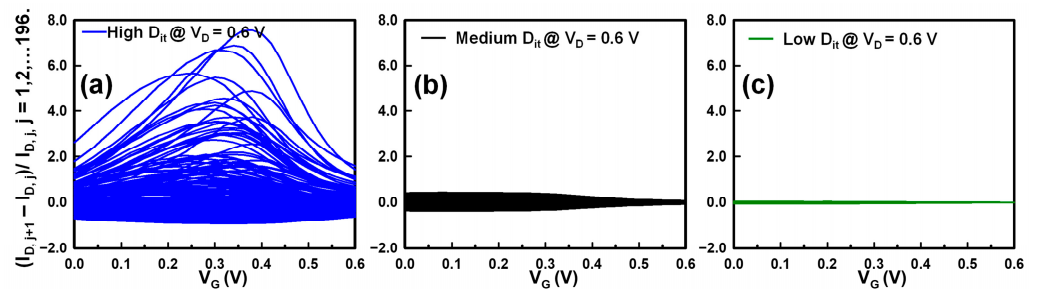


Figure 11. The RITs fluctuated drain current mismatch $\Delta I_D/I_D = (I_{D,j+1} - I_{D,j})/I_{D,j}$, where are two arbitrary adjacent drain currents for $j = 1, \dots, 196$, versus the gate voltage of explored bulk FinFET devices with respect to three levels of D_{it} : (a) high D_{it} , (b) medium D_{it} , and (c) low D_{it} , respectively.

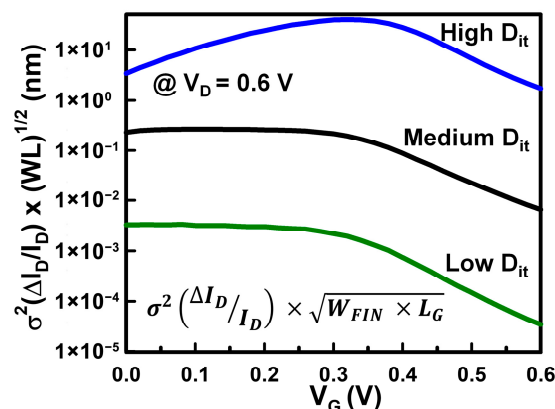


Figure 12. Normalized standard deviation of the drain current mismatch versus the gate voltage under the three levels of D_{it} , where the drain current is normalized by $(W_{FIN} \times L_G)^{1/2}$.

3.4. Impact of RITs on RTS Noise

It has been extensively calculated that the random telegraph signal (RTS) noise is significant in the characterization of interface traps in MOSFETs [66]. RTS effects were modeled using a quasi-static statistical framework, avoiding full time-domain simulations to maintain computational efficiency across large 3D ensembles. Capture and emission times were calculated from trap parameters, and occupancy probabilities were derived using Fermi–Dirac statistics under bias. Device behavior was then sampled across randomized trap configurations to emulate RTS-induced current fluctuations. The resulting amplitude distributions were consistent with reported time-resolved RTS measurements in nanoscale FinFETs, confirming the robustness of the approach. It is thought that the relative change in the drain current (RTS) is caused by the random trapping of electrons in the channel region. Under three levels of D_{it} , Figure 13a–c show the calculated RTS variations versus the gate voltage induced by RITs. It is observed that the RTS magnitude varies with the gate voltage, i.e., at the threshold voltage the RTS magnitude is high under the three levels of D_{it} . It has been observed that RTS magnitude is increasing under high D_{it} conditions. Furthermore, under high D_{it} , RTS variation also increases. As a result, the impact of RITs on RTS variation is marginal for medium D_{it} . RITs have a relatively small impact on RTS magnitude and variation for low D_{it} . The high D_{it} of the RITs, therefore, has a greater impact on the RTS magnitude than other factors. RITs-fluctuated transconductance efficiency (g_m/I_D) versus gate voltage for three different levels of D_{it} , as shown in Figure 14a–c. g_m/I_D is a design metric that measures the maximum transconductance that a device can provide at a given bias. At low gate voltage it should be saturated to a constant.

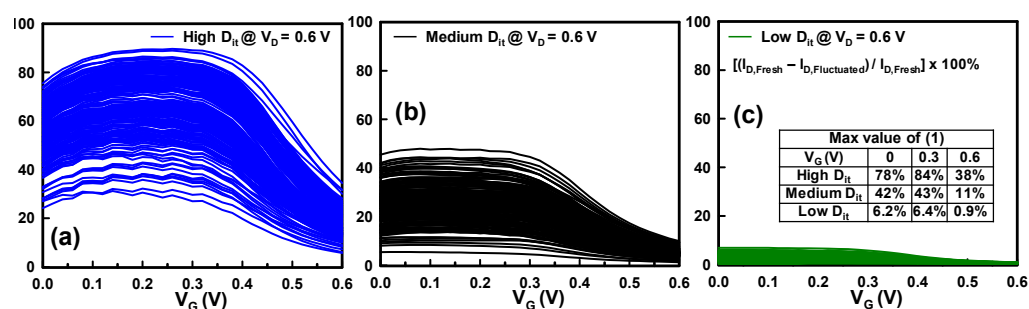


Figure 13. The fluctuated relative drain current random telegraph signal amplitude variation $[(I_{D,Fresh} - I_{D,Fluctuated})/I_{D,Fresh}] \times 100\%$ versus the gate voltage induced by RITs of the explored bulk FinFET devices under the three levels of the D_{it} : (a) high D_{it} , (b) medium D_{it} , and (c) low D_{it} , respectively. In figure (c), the inset table shows the maximum value of random telegraph signal amplitude for three levels of D_{it} .

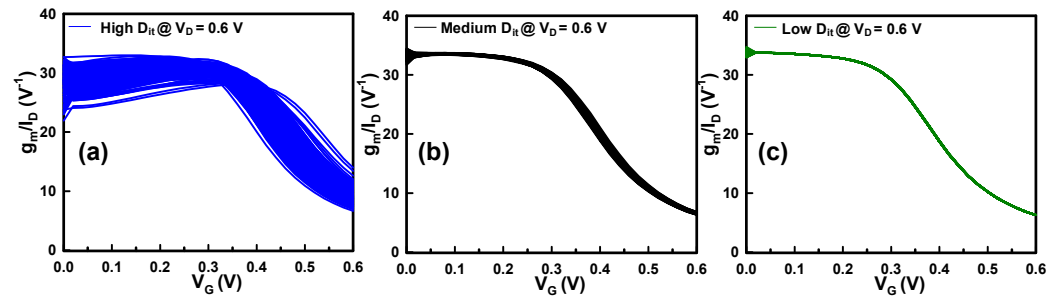


Figure 14. The fluctuated transconductance efficiency (g_m/I_D) versus the gate voltage induced by RITs under the three levels of D_{it} of the bulk FinFETs. (a) High D_{it} , (b) medium D_{it} , (c) low D_{it} , respectively.

Figure 14a illustrates the severe effects of RITs on g_m/I_D under high D_{it} conditions. Additionally, the variations of g_m/I_D with the high D_{it} are more significant than those with the low D_{it} .

3.5. Impact of RITs on AC Characteristics

A major AC characteristic is parasitic capacitance, which is the total gate capacitance (C_G) directly derived from AC curves under strong inversion. Figure 15a–a'' illustrate the RIT-induced C_G - V_G characteristic fluctuations under the three levels of D_{it} , with an operating frequency of 10 GHz and a drain voltage of 0.05 volts. It was found that C_G - V_G characteristics have higher RIT fluctuations at high levels of D_{it} ; particularly significant variations are observed in the region above the threshold voltage. Due to the large number of charge carriers at high gate voltages, interface traps are more likely to capture and emit charge, resulting in significant fluctuation. As shown in the inset of Figure 15a, we calculated C_G versus the number of RITs for each level of D_{it} . Furthermore, the reductions in C_G are observed under the biasing of $V_G = 0.6$ V with an increased number of RITs under the three levels of D_{it} . A significant fluctuation in C_G has been observed at the high level of D_{it} . Under the three levels of D_{it} , Table 2 shows the statistical variations in C_G induced by RITs. The comparison is made between C_G values at different gate voltages since the capacitance is dominated by the depletion region and the inversion charge at low and high gate biases, respectively. Despite this, the RITs-induced C_G fluctuation is increased with increased gate voltage due to the increased occurrence of trap capture and emission of conduction carriers within the channel caused by RITs. Specifically, a significant variation is observed for the explored devices at high D_{it} and gate voltage levels. Our study shows that the C_G value is very small in comparison with reported values [56] under high D_{it} .

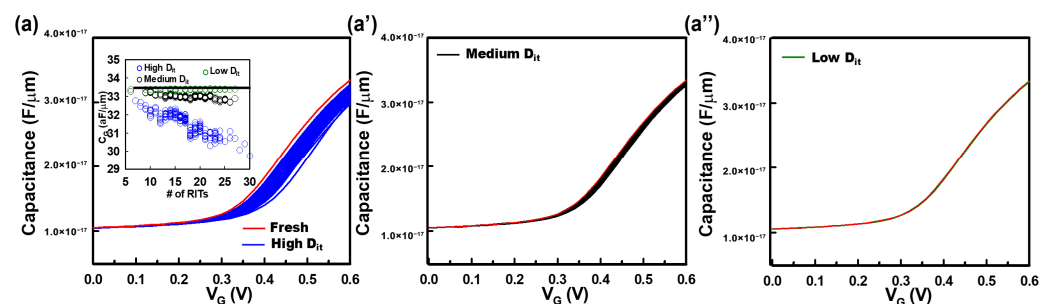


Figure 15. (a–a'') The RITs-fluctuated gate capacitance versus gate voltage characteristics under the three levels of D_{it} , respectively, where the red lines indicate a fresh device. The inset in figure (a) is C_G fluctuations versus the number of RITs under the three different D_{it} conditions, where the black line indicates the fresh device gate capacitance.

Table 2. List of statistical variation of C_G fluctuations under different V_G under the high, medium, and low levels of D_{it} .

Source	C_G Variation(%)		
	$V_G = 0$ V	$V_G = 0.3$ V	$V_G = 0.6$ V
Low D_{it}	0.33	0.31	0.2
Medium D_{it}	0.45	2.6	1.9
High D_{it}	0.85	7	10.6

3.6. Significance of RITs on RF Characteristics

The inset of Figure 16a depicts a common-source amplifier circuit for high frequency (RF) characteristic fluctuation. There is a sinusoidal wave input to the circuit with an amplitude of 0.05 volts, and the circuit operates between $V_G = 0.4$ V and $V_D = 0.5$ V. The fluctuated curves of voltage gain in dB versus the frequency of input signal induced by RITs under three levels of D_{it} are shown in Figure 16a–a'', respectively. It has been noted that the fresh device (red line) has a voltage gain of 11.9 dB. We calculate the voltage gain at a frequency of 10^7 Hz, we estimate f_T using the unitary voltage gain, and we estimate f_{3dB} using the 3-dB point voltage gain as defined by

$$-3 \text{ dB} = 20 \log_{10} \left(0.707 \times \frac{V_{out}}{V_{in}} \right). \quad (1)$$

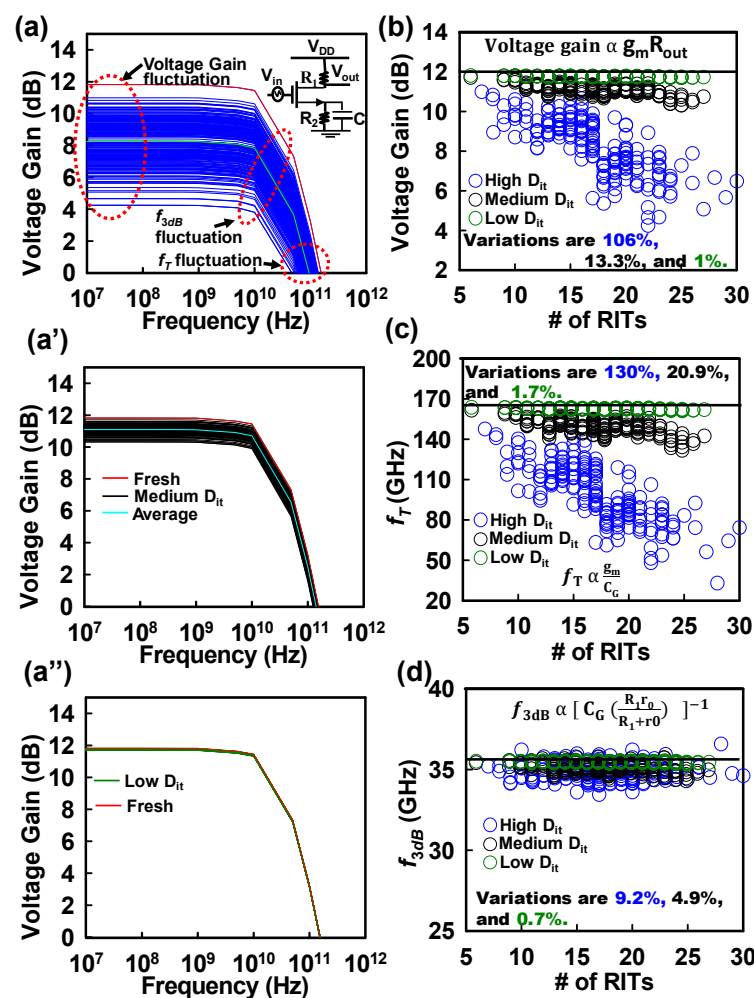


Figure 16. (a–a'') The RITs-fluctuated voltage gain versus the frequency curves under the three levels of D_{it} ; the inset in figure (a) is utilized common-source amplifier circuit for RF simulations, where the

value of R_1 is 50 K Ω , R_2 is 10 K Ω , and C is 10^{-6} F. (b) The fluctuated voltage gain versus the number of RITs with varied D_{it} . (c) The fluctuated cut-off frequency versus the number of RITs with varied D_{it} . (d) The fluctuated 3 dB frequency versus the number of RITs under three levels of D_{it} . The black lines in figures (b–d) indicate the fresh device for voltage gain, cut-off frequency, and 3-dB frequency [67], respectively.

It is observed that the significant voltage gain fluctuations under the low frequency, the signal frequency increases the reductions in voltage gain fluctuations for the three levels of D_{it} . As a result of the increased level of D_{it} , voltage gain fluctuations are further increased. A voltage gain of unity is generated at the cutoff frequency and the f_T is defined as [67]

$$f_T = \frac{g_m}{2\pi C_G} \quad (2)$$

In this equation, g_m and C_G represent the transconductance and gate capacitance, respectively. According to the fresh device, the voltage gain, the f_{3dB} , and the f_T , are respectively, 11.9 dB, 35.5 GHz, and 168 GHz. As shown in the inset of Figures 6a and 15a, the f_T fluctuations are affected by the results of the g_m and C_G fluctuations. Comparing the simulated devices to previously reported values, the simulated devices display an outstanding f_T [6,68]. Compared with other frequencies, significant voltage gain fluctuations are observed at 10^7 Hz. Moreover, as shown in Figure 16b, voltage gain fluctuations are significantly reduced with increasing numbers of RITs, and they vary by 106%, 13.3%, and 1% for three levels of D_{it} . Figure 16b,c insets show the tendency of voltage gain, f_T , and f_{3dB} as a function of characteristics of the device and circuit element. As the number of RITs increases, the f_T fluctuation decreases, but significant fluctuations occur at high RIT levels. For the three levels of D_{it} , from high to low, the statistical variation of f_T fluctuation is 130%, 20.9%, and 1.7%. Similarly, marginal f_{3dB} fluctuations can be observed at all three levels of D_{it} . In the case of high-level and low-level D_{it} , the fluctuation variation of f_{3dB} is 9.2%, 4.9%, and 0.7%, respectively. Moreover, as V_{th} increases, the output resistance of the transistor (R_{out}), r_o , increases as well. Our recent study provides a detailed description of the physical mechanism [67]. The voltage gain of the studied RF circuit is proportional to the resistance of the output and g_m . By increasing the number of RITs, the I_{on} of the transistor, which is associated with the RF circuit's output current, decreases and, thus, the circuit's output voltage increases. As a result, the tendency for voltage gain fluctuations is dominated by an increase in output resistance with increasing V_{th} . In Figure 7a–a'', the V_{th} increases as the number of RITs increases. Figure 16c illustrates the relationship between the f_T and the number of RITs. As the number of RITs increases, the fluctuations in f_T are reduced, resulting in a fluctuation variation of 130% at zero voltage gain. Earlier, it was noted that the f_T is proportional to g_m/C_G in the expression (3). Thus, reducing the g_m and increasing the C_G fluctuation values can decrease the f_T fluctuations. Figure 16d shows f_{3dB} versus the number of RITs for the three levels of D_{it} , and its fluctuation variation is 9.2%, 4.9%, and 0.7%. Therefore, under the three levels of D_{it} , the studied devices are almost independent at f_{3dB} fluctuations. Figure 17a illustrates the fluctuation of f_{3dB} versus f_T of the RF circuit induced by RITs at three levels of D_{it} . A decrease in f_T fluctuation results in a decrease in the magnitude of f_{3dB} fluctuation. As shown in Figure 15a, the fluctuation of f_T and f_{3dB} is dominated by the C_G and is reduced when compared with the fresh device. The relationship between f_T and f_{3dB} fluctuations versus voltage gain fluctuations for the RF circuit is illustrated in Figure 17b,c, where the filled red circle represents the fresh device. The f_T and f_{3dB} are decreased as the voltage gain of the RF circuit is decreased. According to Figure 17b,c, there is a decrease in the tendency of RF circuit voltage gain fluctuation due to the g_m , as compared with the fresh device. As the number of RITs increases, the

g_m fluctuation decreases, as shown in the inset of Figure 6a. C_G fluctuation accompanied by a decreasing g_m result in the reduction of f_T and f_{3dB} for an increasing number of RITs. Based on SRH estimates ($\tau \approx 1/(\sigma v_{th})$), the effective response frequency of interface traps in our study lies in the 10^8 – 10^{11} Hz range, consistent with reported HKMG devices. Thus, traps contribute to dispersion in C_G and gain within this frequency window, while their impact diminishes at higher RF frequencies where they can no longer follow the signal. Under the three levels of D_{it} , Table 3 summarizes and lists the normalized variation of fluctuation caused by RITs. According to the comparison, the SCE parameters, output characteristic parameters, and RF circuit parameters fluctuation variations increase with the increase in D_{it} .

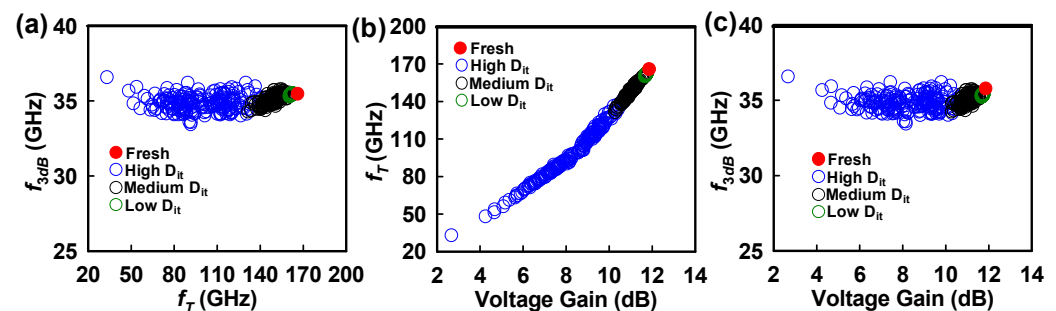


Figure 17. The high-frequency characteristic fluctuation of bulk FinFET circuit induced by RITs, where the filled red circle indicates the fresh device and empty circles are the RITs fluctuated cases under the three levels of D_{it} . (a) The RITs fluctuated 3-dB frequency versus the cut-off frequency of the simulated device RF characteristics. (b) The RITs fluctuated cut-off frequency versus the voltage gain. (c) The fluctuated 3-dB frequency versus the voltage gain of the simulated devices.

Table 3. List of statistical variation calculations of SCE and RF circuit parameter induced by RITs under different D_{it} of bulk FinFETs. The variation percentage is calculated by $(6\sigma/\mu) \times 100\%$, where σ is the standard deviation, and μ is the average value.

D_{it}	$6\sigma/\mu$	V_{th} (%)	I_{off} (%)	I_{on} (%)	g_m (%)	g_d (%)	Gain (%)	f_T (%)	f_{3dB} (%)	R_{on} (%)	R_{out} (%)
Low D_{it}		0.7	6.4	0.5	0.5	0.36	1.1	1.7	0.7	0.4	1.9
Medium D_{it}		6.4	52.9	6.6	2.6	5.2	13.4	21.0	4.9	5.2	24.7
High D_{it}		25.6	145.7	40.1	18.8	31.1	106.8	130.4	9.13	31.8	99.7

3.7. Significance of Interface Trap Random Position on RF and AC Characteristics

We study three different scenarios for calculating the effect of random position of RITs on both AC and RF characteristics. Figure 18a illustrates the adapted profiles for RITs near the source end, in the middle of channel, and near the drain end, respectively. Three groups according to RIT distribution are categorized: group 1: RITs located near the source end (two RITs located near the drain and middle of channel), group 2: RITs located in the middle of channel (two RITs located near the drain and source ends), and group 3: RITs located near the drain end (two RITs located near the source and middle of channel). Each time, only one group is filled with randomly generated RITs. Figure 18b shows the distribution of RITs for the three groups of devices, with an average of 17 RITs per group. There is a range of 5 to 30 RIT numbers in each device. In this manner, we will be able to study the fluctuation of RF and AC characteristics in channel as a result of RIT number and position at the same time. Following that, we investigate how RITs affect C_G and RF characteristics near the source end, in the middle of channel, and near the drain end. In the case of devices under high D_{it} , Figure 19a,c plot of the RITs fluctuated C_G versus the gate voltage of the RITs

near the source end, in the middle of channel, and near the drain end, respectively [69,70]. In the below threshold region, for three groups, the C_G fluctuation is very low. There is an increase in the C_G fluctuation for three groups in the just above threshold region. In addition, devices in the saturation region are more susceptible to fluctuations in the C_G . Furthermore, the saturation region C_G fluctuation becomes significant in the RITs located near source end, compared with the other two groups.

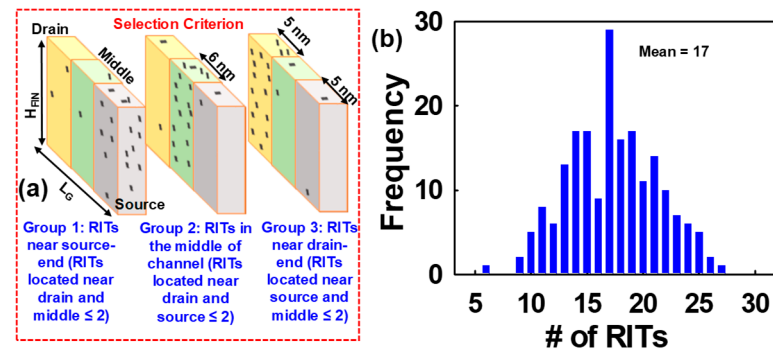


Figure 18. (a) The L_G of bulk FinFET is divided into three parts: 5, 6, and 5 nm, respectively. For the impact of position of RITs on AC and RF characteristics of fluctuated devices, we classify them into three groups: (1) devices with RITs located near the source end, (2) devices with RITs located middle of the channel, and (3) devices with RITs located near the drain end, respectively. (b) The distribution of RITs for the three group devices, where the average number of RITs in each group is 17.

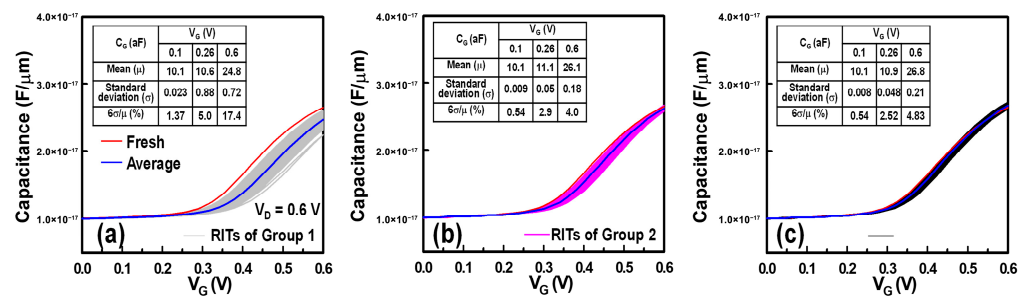


Figure 19. The RITs fluctuated gate capacitance versus the gate voltage curves under the high level of D_{it} , where the red lines indicate a fresh device, the blue lines indicate the average fluctuation. (a) Devices with RITs of Group 1. (b) Devices with RITs of Group 2. (c) Devices with RITs of Group 3.

In addition, the fluctuation of high-frequency characteristics with the three different groups are mainly followed by Figure 16. As shown in Figure 20a–c, the RITs fluctuated curves of voltage gain in dB versus the frequency of input signal under high D_{it} with three groups, RITs near the source end, middle of channel, and near the drain end. First, we compared devices with RITs located at the source end, at the middle of channel, and at the drain end. In three groups, voltage gain fluctuations are reduced when the signal frequency is low, whereas they increase when the signal frequency is high. Additionally, the RITs located near the source end contribute to the significant fluctuations in voltage gain. Figure 20c illustrates that the RITs located near the drain end are more resistant to RITs.

The high-frequency characteristics fluctuation in voltage gain, f_T and f_{3dB} for the devices under high D_{it} with the three groups, RITs near source end, in the middle of channel, near drain end devices are further explored. For three groups of devices, the voltage gain, f_T and f_{3dB} fluctuations are shown in Figure 21a,c. Moreover, the voltage gain fluctuations decrease significantly with the increasing number of RITs, as shown in Figure 21a, and they are decreasing for three groups of devices as well. In devices with RITs located near the source end, significant fluctuations in voltage gain have been

observed. As compared to RITs near source end devices, the near drain end devices exhibit a 23.4% reduction in fluctuation. As the number of RITs increases, the f_T fluctuations decrease for all three groups, as shown in Figure 21b. In comparison with other devices, devices with RITs located near the source end show significant f_T fluctuations. RITs near the drain end have a 38.4% decrease in fluctuation compared to RITs near the source end. Additionally, three groups of devices exhibit marginal fluctuations in f_{3dB} . A detailed description of the physical mechanism can be found in Subsection F. As shown in Table 4, the mean and standard deviation of RIT fluctuations under high D_{it} are summarized with three groups of devices, including the original device. As a result of the comparison, it has been found that the RF circuit parameters fluctuate significantly with devices having RITs located near the source end.

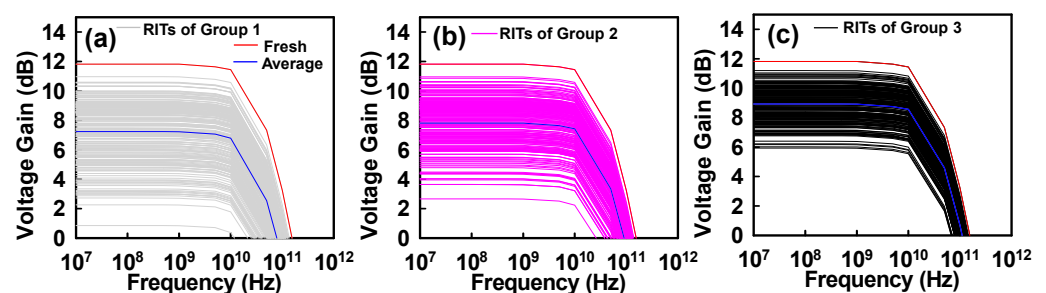


Figure 20. The fluctuated voltage gain versus the frequency curves induced by high D_{it} with three classified groups, where the red curves indicate the fresh device, blue curves indicate the average fluctuation. (a) Devices with RITs of Group 1. (b) Devices with RITs of Group 2. (c) Devices with RITs of Group 3.

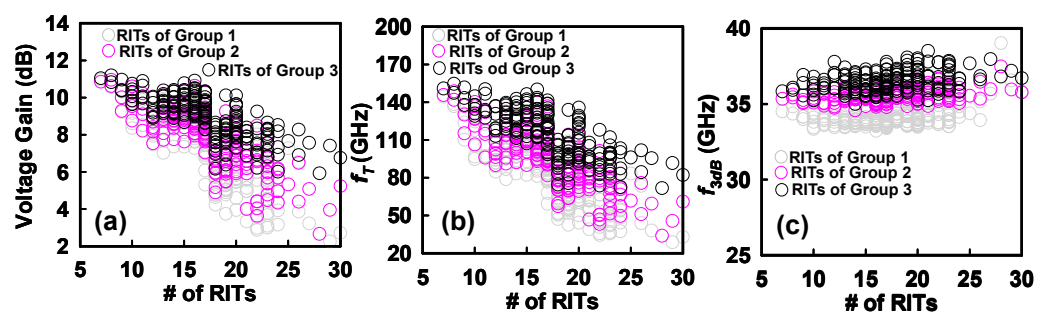


Figure 21. (a) The RITs fluctuated voltage gain versus the number of RITs for three groups, devices RITs of Group 1, devices RITs of Group 2, and devices RITs of Group 3. (b) The RITs fluctuated f_T versus the number of RITs under the high D_{it} condition with three different groups. (c) The RITs fluctuated f_{3dB} versus the number of RITs under high D_{it} condition with three different groups.

Table 4. List of mean and statistical deviation of gain, cut-off frequency, and 3-dB frequency fluctuations under high D_{it} with four different conditions.

Source	Gain (dB)			f_T (GHz)			f_{3dB} (GHz)		
	Average (μ)	Standard Deviation (σ)	$6\sigma/\mu$ (%)	Average (μ)	Standard Deviation (σ)	$6\sigma/\mu$ (%)	Average (μ)	Standard Deviation (σ)	$6\sigma/\mu$ (%)
Full random	8.25	1.42	103.27	99.6	21.2	127.7	34.86	0.52	8.95
Near source	7.23	2.04	169.3	83.4	25.6	184.2	34.2	0.65	11.4
Middle	7.82	1.64	125.8	95.4	23.2	145.9	35.6	0.41	6.91
Near drain	8.92	1.16	78.1	115.3	19.5	101.47	36.4	0.66	10.87

4. Conclusions

In summary, we have demonstrated that random interface traps (RITs) induce significant fluctuations in the DC, AC, and RF characteristics of HKMG bulk FinFETs at three different D_{it} levels. Despite devices having the same number of RITs, the random spatial distribution results in distinct variability trends. Quantitatively, under high D_{it} conditions, the variability of key device parameters is severe: V_{th} variation reaches ~25.6%, I_{off} spreads up to ~145%, and I_{on} fluctuates by ~40%. In the RF domain, voltage gain fluctuates by ~107%, cut-off frequency (f_T) by ~130%, while f_{3dB} remains relatively stable with ~9% variation. These results indicate that traps positioned near the source end strongly enhance variability, whereas traps near the drain end lead to relatively smaller fluctuations in gate capacitance, voltage gain, and RF figures of merit. Compared to previous studies that primarily focused on DC variability, this work provides the first unified statistical 3D device simulation framework quantifying the impact of RITs on DC, AC, and RF domains simultaneously. The findings highlight the critical importance of D_{it} control and trap spatial distribution in sub-5 nm FinFET design, and suggest that minimizing trap activity near the source region can effectively mitigate variability in both digital and RF applications.

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Abbreviations

The following abbreviations are used in this manuscript:

D_{it}	Density of Interface Trap
HKMG	High- κ metal gate
RIT	Random Interface Trap
FinFET	Fin Field-Effect Transistor

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