mathematics

MDPI

Article

A Mathematical Co-Design Framework for Synchronous Boost DC-DC Converters and PI Controllers Under Parasitic and Semiconductor Loss Effects

Nikolay Hinov [1,2,*], Polya Gocheva [3] and Valeri Gochev [4]

[1] CoE "National Center of Mechatronics and Clean Technologies", 1000 Sofia, Bulgaria
[2] Department of Computer Systems, Faculty of Computer Systems and Technologies, Technical University of Sofia, 1000 Sofia, Bulgaria
[3] Doctoral School, Technical University of Sofia, 1756 Sofia, Bulgaria; p.gocheva@utp.bg
[4] Department of Telecommunications, University of Telecommunications and Posts, 1700 Sofia, Bulgaria; v.gochev@utp.bg
* Correspondence: hinov@tu-sofia.bg

Abstract

This paper proposes a mathematical co-design framework for synchronous Boost DC-DC converters and their PI voltage controllers. In contrast to the conventional sequential design approach, where the power stage is sized first and the controller is tuned afterward, the proposed method treats the converter and the controller as a single coupled design problem. A nonlinear averaged model of the synchronous boost converter operating in continuous conduction mode is considered, explicitly incorporating the inductor series resistance, the capacitor equivalent series resistance, and the on-state resistances of the active switches. In addition, a simplified but physically interpretable loss model is included in order to capture inductor copper loss, capacitor ESR loss, semiconductor conduction loss, and switching loss. Based on this formulation, the joint design of the power stage and the PI controller is cast as a constrained multi-objective optimization problem whose decision variables include the inductance, capacitance, switching frequency, and controller gains. The optimization criteria account for output-voltage ripple, settling time, total losses, and current stress, while practical constraints related to duty cycle, current limits, ripple bounds, and closed-loop feasibility are enforced. The proposed framework makes it possible to compute Pareto-efficient designs and to reveal trade-offs that remain hidden under classical decoupled design procedures. Numerical case studies are structured to compare the proposed co-design strategy with a conventional sequential-design baseline. An optional technology-aware extension is also considered, allowing the influence of different semiconductor classes, such as Si, SiC, and GaN, to be assessed through technology-dependent loss and switching-frequency assumptions. The results indicate that the proposed framework provides a mathematically grounded and practically useful basis for integrated converter–controller synthesis in nonideal power electronic systems.

Keywords: synchronous boost converter; co-design; PI controller; multi-objective optimization; power electronics; parasitic effects; semiconductor losses; nonlinear averaged model; Pareto optimization

MSC: 93C10; 93B52; 90C29; 90C30

Academic Editor: Shiqing Zhang

Received: 9 April 2026
Revised: 11 May 2026
Accepted: 5 June 2026
Published: 11 June 2026

1. Introduction

Boost DC-DC converters are among the most widely used power electronic interfaces in renewable energy systems, battery-powered devices, automotive electronics, and distributed power architectures. Their ability to step up a low input voltage to a higher regulated output voltage makes them particularly attractive in applications where both conversion efficiency and output-voltage quality are critical [1,2]. In practical implementations, however, the behavior of a boost converter depends not only on the selected control strategy but also on the physical characteristics of the power stage, including the inductance, capacitance, switching frequency, and nonideal properties of the passive and semiconductor components [3,4].

In conventional engineering practice, the design of a boost converter is usually performed in a sequential manner. First, the passive elements and the switching frequency are selected from steady-state conversion requirements and ripple-based design rules. Afterward, a controller is tuned in order to achieve the desired transient response and output-voltage regulation [5,6]. Although this methodology is simple and widely used, it does not explicitly account for the strong coupling between hardware parameters and closed-loop performance. In particular, the values of the inductance, capacitance, and switching frequency directly influence the converter dynamics, the achievable regulation bandwidth, the output-voltage ripple, the current stress, and the power losses. As a consequence, a design obtained through a decoupled sequential procedure may be suboptimal when the converter is viewed as a complete closed-loop dynamical system [7,8].

This issue becomes even more relevant in synchronous boost converters, where the nonideal characteristics of the active switches materially affect the attainable performance. In contrast to idealized boost-converter models, practical synchronous implementations exhibit inductor winding losses, capacitor equivalent series resistance, and semiconductor conduction and switching losses. These nonideal effects alter both steady-state efficiency and transient behavior, and they may also change the relative desirability of higher switching frequencies, larger passive elements, or more aggressive controller tuning. Therefore, a realistic design methodology should not rely solely on ideal converter equations, but should incorporate the dominant parasitic mechanisms directly into the design framework.

The analysis and control of boost converters have been studied extensively in the literature. A large number of works employ averaged state-space models for control design, since such models provide a tractable representation of the converter dynamics while preserving the dominant nonlinear behavior relevant to regulation tasks. Within this framework, PI-based voltage regulation remains especially common because of its conceptual simplicity, low implementation cost, and satisfactory performance in a wide range of applications [9–11]. However, many existing studies treat the converter hardware as fixed and focus primarily on controller synthesis or tuning alone [12–14].

A second important line of research concerns the modeling of nonideal and parasitic effects in DC-DC converters. Previous studies have shown that parasitic resistances can significantly modify the effective conversion gain, the damping properties, the efficiency, and the dynamic response of practical converters. In particular, the winding resistance of the inductor, the ESR of the output capacitor, and the on-state losses of semiconductor devices may substantially affect both the physical operation and the control-oriented behavior of the converter. These observations indicate that optimization or controller design based exclusively on idealized boost models may fail to capture essential system-level trade-offs [15,16].

In parallel, a substantial body of literature has addressed optimization-based converter design and controller tuning. Metaheuristic and multi-objective methods have been applied to improve converter sizing, to tune PI-type and hybrid controllers, and to identify

favorable trade-offs among efficiency, ripple, and transient performance. Such studies demonstrate the usefulness of simulation-based optimization in power electronics, especially when the design objectives are conflicting and analytical gradients are difficult to obtain. Nevertheless, these approaches often optimize either the hardware or the controller separately, rather than considering both within a single unified formulation [17,18].

A broader conceptual perspective is provided by the growing literature on control co-design. In co-design approaches, hardware parameters and controller parameters are optimized jointly as parts of one coupled engineering problem. This idea has proven valuable in several energy-conversion and dynamical-system applications, where the separation between plant design and controller synthesis can lead to inferior solutions. From this viewpoint, power electronic converters constitute a natural and compelling application domain, since their closed-loop behavior depends strongly on both the circuit parameters and the regulation law. Yet, despite this conceptual relevance, the joint co-design of synchronous boost converters and classical PI controllers under explicit parasitic and semiconductor-loss-aware modeling remains insufficiently explored [19,20].

This gap motivates the present study. The central premise of this paper is that the design of a synchronous boost converter should not be decomposed into a hardware stage followed by a controller-tuning stage, but should instead be formulated as a coupled mathematical optimization problem. To this end, the paper develops a control-oriented nonlinear averaged model of a synchronous boost converter operating in continuous conduction mode and explicitly includes the inductor series resistance, the capacitor equivalent series resistance, and the on-state resistances of the active switches. In addition, a simplified yet physically interpretable loss model is incorporated in order to capture the dominant contributions of copper loss, capacitor ESR loss, semiconductor conduction loss, and switching loss.

Based on this modeling framework, the joint design of the converter and its PI voltage controller is formulated as a constrained multi-objective optimization problem [20,21]. The decision variables include both power-stage parameters and controller gains, thereby enabling simultaneous synthesis of the physical converter and the control law. The considered performance indices reflect both static and dynamic objectives, including output-voltage ripple, settling time, total loss, and current stress [22,23]. Practical feasibility is enforced through admissible parameter ranges, duty-cycle constraints, current and voltage bounds, and closed-loop performance requirements. In this way, the converter and the controller are treated as a single integrated design object rather than as two loosely connected subsystems [24,25].

The proposed formulation is particularly relevant for revealing trade-offs that remain hidden under conventional design practice. For example, increasing the switching frequency may reduce ripple and facilitate faster regulation, but may also increase switching-related losses; similarly, larger passive elements may reduce ripple and stress but can slow down dynamic response or alter the feasible controller gains. By computing Pareto-efficient solutions, the proposed method makes these interactions explicit and provides the designer with a structured view of the available compromises [25,26].

The main contributions of this work can be summarized as follows. First, a unified mathematical co-design framework is proposed for synchronous boost DC-DC converters and PI controllers. Second, the converter model explicitly incorporates major parasitic elements and a simplified semiconductor-loss description, thereby improving the realism of the design problem. Third, the integrated synthesis task is formulated as a constrained multi-objective optimization problem over both hardware and controller parameters. Fourth, the proposed co-design methodology is evaluated against a conventional sequential-design baseline in order to assess the practical benefit of joint optimization.

Finally, the framework admits an optional technology-aware extension in which different semiconductor classes, such as Si, SiC, and GaN, can be compared through technology-dependent loss and switching-frequency assumptions.

The remainder of the paper is organized as follows. Section 2 presents the nonlinear averaged model of the synchronous boost converter, including the parasitic elements and the PI control law. Section 3 formulates the integrated converter–controller design problem as a constrained multi-objective optimization task. Section 4 describes the numerical optimization procedure, while Section 5 defines the case study setup and the adopted performance metrics. Section 6 presents and discusses the obtained results, including the comparison with the sequential-design baseline and the optional technology-aware extension. Finally, the conclusions are summarized in Section 7.

2. Mathematical Model

This section introduces the mathematical model used for the proposed co-design framework. In contrast to an idealized boost-converter representation, the present formulation incorporates the main parasitic effects that significantly influence both converter efficiency and closed-loop performance. In particular, the model accounts for the inductor series resistance, the capacitor equivalent series resistance, and the on-state resistances of the semiconductor devices in a synchronous boost configuration. This choice provides a more realistic basis for integrated converter–controller optimization while preserving a level of complexity suitable for mathematical analysis and numerical optimization.

2.1. Synchronous Boost Converter with Parasitic Elements

Consider a synchronous boost DC-DC converter supplied by an input voltage $V_{in} > 0$, feeding a resistive load $R > 0$, and operating with switching frequency f_s. The converter is assumed to operate in continuous conduction mode (CCM). Let $i_L(t)$ denote the inductor current, let $v_C(t)$ denote the voltage across the ideal capacitive element, and let $v_o(t)$ denote the output terminal voltage. The duty-cycle command is denoted by $u(t) \in [0, 1]$.

To account for nonidealities, the following parasitic parameters are introduced:

$r_L > 0$: inductor winding resistance,

$r_C > 0$: equivalent series resistance (ESR) of the output capacitor,

$R_{on,1} > 0$: on-state resistance of switch S_1,

$R_{on,2} > 0$: on-state resistance of synchronous switch S_2.

Figure 1 illustrates the considered synchronous boost DC-DC converter and the associated PI voltage-control loop. The figure highlights the main passive and active elements of the power stage, together with the nonideal parasitic components explicitly considered in the proposed model of the semiconductor devices. It also shows the feedback structure used to generate the duty-cycle command from the output-voltage error.

Here, g_1 and g_2 denote the gate-drive signals of switches S_1 and S_2, respectively; i_{S1} and i_{S2} are the corresponding switch currents; i_C is the capacitor current; i_o is the output current. The output capacitor is modeled as an ideal capacitance C in series with the ESR r_C. Accordingly, the terminal output voltage differs from the internal capacitor voltage and can be written as:

$$v_o(t) = v_C(t) + r_C i_C(t),$$

where $i_C(t)$ is the capacitor current. Since:

$$i_C(t) = C\dot{v}_C(t),$$

the capacitor ESR affects both the output ripple and the power dissipation.

Using a state-space averaging approach, a control-oriented large-signal model can be written in terms of the state variables:

$$z(t) = \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix}.$$

A practically useful averaged model is given by:

$$L\dot{i}_L(t) = V_{in} - r_L i_L(t) - [(1-u(t))R_{\text{on},2} + u(t)R_{\text{on},1}]i_L(t) - (1-u(t))v_o(t),$$

$$\dot{v}_C(t) = (1-u(t))i_L(t) - \frac{v_o(t)}{R}.$$

The terminal output voltage is related to the capacitor voltage through the ESR relation:

$$v_o(t) = v_C(t) + r_C C\dot{v}_C(t).$$

This model preserves the main coupling mechanisms between the power stage and the controller while reflecting the effect of copper losses, semiconductor conduction losses, and capacitor ESR. It also shows that the output voltage is no longer determined solely by the ideal boost relation, since parasitic elements modify both steady-state and transient behavior.

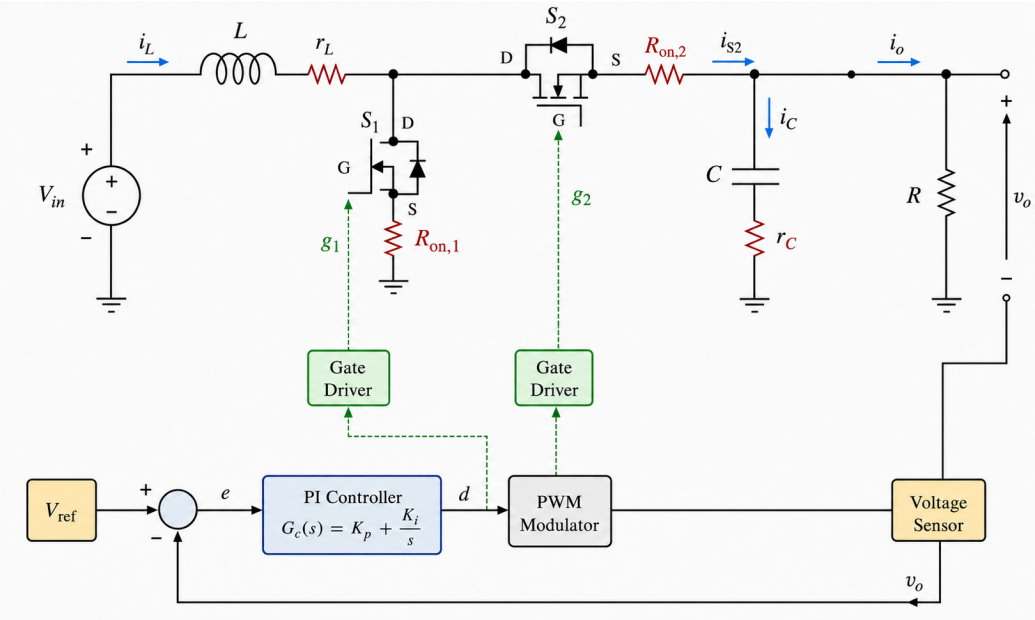


Figure 1. Synchronous Boost DC-DC converter with PI voltage controller and nonideal parasitic elements.

For controller synthesis and optimization, the above model can be interpreted as a nonlinear averaged system of the form:

$$\dot{z}(t) = f(z(t), u(t), p),$$

where the parameter vector

$$p = [L\ C\ f_s\ r_L\ r_C\ R_{\text{on},1}\ R_{\text{on},2}]^T.$$

2.2. PI Voltage Control Law

Let $V_{ref} > 0$ denote the desired output-voltage reference. The regulation error is defined as:

$$e(t) = V_{\text{ref}} - v_o(t).$$

A proportional–integral voltage controller is adopted, with integral state:

$$\xi(t) = \int_0^t e(\tau)d\tau, \;\; \dot{\xi}(t) = e(t)$$

The unsaturated control signal is given by:

$$u_c(t) = K_p e(t) + K_i \xi(t),$$

where $K_p \geq 0$ and $K_i \geq 0$ are the controller gains.

Since the duty cycle is physically limited, the actual control input is defined through saturation:

$$u(t) = sat(uc(t)),$$

with

$$0 \leq u(t) \leq 1.$$

This saturation is essential in the present setting, because the feasible range of the duty cycle is directly linked to the operating limits of the converter and may become active during aggressive transient regulation or under unfavorable parameter choices.

2.3. Closed-Loop Nonlinear Model

By augmenting the state vector with the integral state $\xi(t)$, the closed-loop state becomes:

$$x(t) = \begin{bmatrix} i_L(t) \\ v_C(t) \\ \xi(t) \end{bmatrix}.$$

The closed-loop converter–controller dynamics are then described by:

$$L\dot{i}_L(t) = V_{in} - r_L i_L(t) - [(1-u(t))R_{\text{on},2} + u(t)R_{\text{on},1}]i_L(t) - (1-u(t))v_o(t),$$

$$C\dot{v}_C(t) = (1-u(t))i_L(t) - \frac{v_o(t)}{R},$$

$$\dot{\xi}(t) = V_{\text{ref}} - v_o(t),$$

with

$$u(t) = \text{sat}(K_p(V_{\text{ref}} - v_o(t)) + K_i\xi(t))$$

and

$$v_o(t) = v_C(t) + r_C C\dot{v}_C(t)$$

This model makes explicit the fact that the dynamic response depends not only on the controller gains (K_p, K_i), but also on the converter parameters (L, C, f_s) and on the parasitic elements (r_L, r_C, $R_{on,1}$, $R_{on,2}$). Consequently, the hardware and control design problems are intrinsically coupled.

2.4. Loss Model

To formulate a meaningful co-design problem, the converter model is complemented by a simplified but physically interpretable loss model. The total power-loss metric is decomposed as:

$$P_{\text{loss}} = P_L + P_C + P_{\text{cond}} + P_{\text{sw}},$$

where:

P_L denotes inductor copper loss,
P_C denotes ESR-related capacitor loss,
P_{cond} denotes semiconductor conduction loss,
P_{sw} denotes semiconductor switching loss.
The inductor copper loss is modeled as:

$$P_L = I_{L,\text{rms}}^2 r_L,$$

where $I_{L,rms}$ is the RMS inductor current.

The capacitor ESR loss is modeled as:

$$P_C = I_{C,\text{rms}}^2 r_C,$$

where $I_{C,rms}$ is the RMS capacitor current.

For the synchronous switches, the conduction losses are approximated by:

$$P_{\text{cond}} = I_{S_1,\text{rms}}^2 R_{\text{on},1} + I_{S_2,\text{rms}}^2 R_{\text{on},2}.$$

The switching losses are represented through a technology-dependent average model. A simple surrogate expression is:

$$P_{\text{sw}} = f_s(E_{\text{on}} + E_{\text{off}}),$$

where E_{on} and E_{off} denote effective turn-on and turn-off energy coefficients. When a more compact mathematical form is preferred, one may use:

$$P_{\text{sw}} = \gamma_\tau f_s \overline{i_L}\,\overline{v_o}$$

where $\gamma_\tau > 0$ is a coefficient associated with the selected semiconductor technology, and $\overline{i_L}$, $\overline{v_o}$ denote representative operating averages.

The above decomposition is sufficiently rich to capture the dominant trade-offs relevant to converter–controller co-design: lower ripple may require larger passive components, higher switching frequency may improve dynamic behavior but increase switching loss, and different semiconductor resistances alter both efficiency and feasible control performance.

2.5. Optional Technology Variable

To extend the model toward technology-aware co-design, a discrete semiconductor technology variable may be introduced:

$$\tau \in \{\text{Si}, \text{SiC}, \text{GaN}\}.$$

The selected technology determines a parameter subset such as:

$$R_{\text{on},1} = R_{\text{on},1}(\tau), \;\; R_{\text{on},2} = R_{\text{on},2}(\tau), \;\; \gamma_\tau = \gamma(\tau),$$

and may also restrict the admissible switching-frequency range:

$$f_s \in [f_{s,\min}(\tau), f_{s,\max}(\tau)]$$

In this way, the design problem becomes a mixed discrete–continuous optimization task. However, because the main objective of the present work is the mathematical formulation of converter–controller co-design, the technology variable is treated as an optional extension rather than as a mandatory component of the base model.

3. Problem Formulation

Based on the nonlinear averaged model and the associated loss description introduced above, the design of the synchronous boost converter and its PI controller is formulated here as a constrained co-design problem. The main idea is to optimize the physical converter parameters and the controller gains jointly, while accounting for parasitic elements, semiconductor losses, and closed-loop operating constraints.

3.1. Design Variables

Let

$$x_p = \begin{bmatrix} L \\ C \\ f_s \end{bmatrix}$$

denote the vector of power-stage design variables.

Let

$$x_c = \begin{bmatrix} K_p \\ K_i \end{bmatrix}$$

denote the vector of controller parameters.

In the base formulation, the parasitic and semiconductor parameters:

$$r_L,\ r_C,\ R_{\text{on},1},\ R_{\text{on},2},$$

are assumed known or selected from component data corresponding to a given implementation. Thus, the main co-design vector is:

$$x = \left[L\ C\ f_s\ K_p\ K_i\right]^T.$$

For the extended technology-aware formulation, a discrete variable is additionally introduced:

$$\tau \in \{\text{Si}, \text{SiC}, \text{GaN}\},$$

and the design vector becomes

$$\widetilde{x} = \left[L\ C\ f_s\ K_p\ K_i\ \tau\right]^T.$$

This extended representation allows the optimization to account not only for continuous sizing and tuning choices, but also for the semiconductor-technology class.

3.2. Objective Functions

The co-design problem aims to balance multiple conflicting performance goals. In the present work, four main objective functions are considered.

The first objective is the output-voltage ripple:

$$J_1(x) = \Delta v_o(x).$$

The second objective is the settling time of the regulated output:

$$J_2(x) = t_s(x).$$

The third objective is the total power-loss metric:

$$J_3(x) = P_{\text{loss}}(x),$$

where P_{loss} is computed from the loss model introduced in Section 2.4.

The fourth objective is a current-stress measure:

$$J_4(x) = \sigma_i(x),$$

which may represent, depending on implementation, the peak inductor current, RMS inductor current, or current ripple.

The resulting multi-objective optimization problem is written as:

$$\min_{x \in \Omega_{\text{feas}}} (J_1(x),\ J_2(x),\ J_3(x),\ J_4(x)).$$

In the extended technology-aware case, the formulation becomes

$$\min_{\tilde{x} \in \tilde{\Omega}_{\text{feas}}} (J_1(\tilde{x}),\ J_2(\tilde{x}),\ J_3(\tilde{x}),\ J_4(\tilde{x})),$$

where the feasible set depends on both continuous parameters and the discrete technology choice.

This multi-objective formulation is preferable to a purely scalarized one because it preserves the Pareto structure of the problem and explicitly reveals the trade-offs among ripple attenuation, transient speed, efficiency, and current stress.

3.3. Feasible Design Set

The feasible set is determined by parameter bounds, operational constraints, and closed-loop admissibility requirements.

3.3.1. Parameter Bounds

The continuous design variables satisfy:

$$L_{\min} \le L \le L_{\max},\ C_{\min} \le C \le C_{\max},\ f_{s,\min} \le f_s \le f_{s,\max},\ K_{p,\min} \le K_p \le K_{p,\max},\ K_{i,\min} \le K_i \le K_{i,\max}.$$

In the technology-aware formulation, the switching-frequency range may depend on τ, so that:

$$f_{s,\min}(\tau) \le f_s \le f_{s,\max}(\tau).$$

3.3.2. Operational Constraints

The converter must satisfy the physical and operational limits:

$$0 \le u(t) \le 1,\ i_L(t) \le i_{L,\max},\ v_o(t) \le v_{o,\max},\ \Delta v_o(x) \le \Delta v_{o,\max}.$$

Depending on the target application, one may also impose bounds on overshoot, RMS currents, or average semiconductor losses. For example,

$$M_p(x) \le M_{p,\max},$$

where M_p denotes the output-voltage overshoot.

If thermal admissibility is to be reflected in a simplified form, an additional bound may be included:

$$P_{\text{loss}}(x) \leq P_{\text{loss,max}}.$$

The operational constraints are implemented explicitly through inequality functions:

$$g_1(x) = \Delta v_o - 0.5 \leq 0,$$

$$g_2(x) = M_p - 0.10 \leq 0,$$

$$g_3(x) = I_{L,peak} - 8 \leq 0,$$

$$g_4(x) = u - 1 \leq 0,$$

$$g_5(x) = -u \leq 0,$$

where the ripple constraint is expressed in volts, the overshoot constraint corresponds to a maximum admissible overshoot of 10%, and the peak-current constraint reflects semiconductor and inductor stress limitations.

3.3.3. Closed-Loop Feasibility

Not every numerical parameter combination leads to acceptable regulation. Therefore, only those vectors are admitted for which the converter is able to track the voltage reference while remaining dynamically well behaved. Formally, the feasible design set is defined as:

$$\Omega_{\text{feas}} = \left\{ x \in \Omega : \begin{array}{l} \text{parameter bounds hold,} \\ \text{operational constraints hold,} \\ \text{the closed-loop response is stable and admissible} \end{array} \right\}.$$

Similarly, in the technology-aware case,

$$\widetilde{\Omega}_{\text{feas}} = \left\{ \widetilde{x} \in \widetilde{\Omega} : \begin{array}{l} \text{continuous and discrete constraints hold,} \\ \text{technology-dependent bounds are satisfied,} \\ \text{the closed-loop response is stable and admissible} \end{array} \right\}$$

In practice, closed-loop admissibility may be verified numerically through simulation-based evaluation, combined if necessary with local linearization around the nominal operating point.

3.4. Objective Normalization and Constraint Penalization

Because the considered objectives have different physical scales and units, objective normalization is introduced before Pareto ranking in order to avoid bias toward objectives with larger numerical magnitude. Let $J_k(x)$ denote the k-th objective function. The normalized objectives are defined as:

$$\widetilde{J}_k(x) = \frac{J_k(x) - J_k^{\min}}{J_k^{\max} - J_k^{\min}},$$

where $J_k^{\min}$ and $J_k^{\max}$ are estimated from the explored population or from predefined engineering bounds.

Constraint violations are handled using a quadratic penalty formulation. For a candidate design vector x, the penalized objective is written as:

$$J_k^{pen}(x) = \widetilde{J}_k(x) + \rho \sum_{i=1}^{N_c} \max(0, g_i(x))^2,$$

where $g_i(x) \leq 0$ represents the i-th constraint function, N_c is the number of constraints, and $\rho > 0$ is a penalty coefficient.

This normalization and penalty strategy improves numerical stability and ensures balanced Pareto ranking among ripple, settling time, total loss, and current-stress objectives.

3.5. Sequential Baseline and Co-Design Hypothesis

To assess the value of the proposed framework, the co-design solutions are compared with a conventional sequential-design baseline. In the sequential approach, the passive elements and switching frequency are first selected using standard design rules and steady-state ripple formulas, while the controller gains are tuned only afterward for the fixed hardware.

The central hypothesis of the present work is that the integrated optimization of:

$$(L, C, f_s, K_p, K_i)$$

for a given parasitic profile, or of:

$$(L, C, f_s, K_p, K_i, \tau)$$

in the extended formulation, yields solutions that improve upon the sequential baseline with respect to the trade-off among efficiency, ripple, and transient performance.

In other words, the proposed methodology is expected to produce Pareto-efficient designs that are not accessible through the traditional decoupled design logic.

3.6. Final Co-Design Statement

The final co-design problem can be stated as follows:

Given the synchronous boost-converter specifications, the input voltage V_{in}, the output reference V_{ref}, the load R, the parasitic parameters $(r_L, r_C, R_{\text{on},1}, R_{\text{on},2})$ and the admissible variable ranges, determine the vector:

$$x^* = \left[L^* \; C^* \; f_s^* \; K_p^* \; K_i^* \right]^T$$

or, in the extended version,

$$\widetilde{x}^* = \left[L^* \; C^* \; f_s^* \; K_p^* \; K_i^* \; \tau^* \right]^T$$

such that the closed-loop synchronous boost converter satisfies all feasibility conditions and minimizes the selected performance indices associated with output ripple, transient response, total losses, and current stress.

This formulation establishes the mathematical basis for the optimization procedure and the numerical case studies presented in the remainder of the paper.

4. Optimization Procedure

This section describes the numerical procedure used to solve the proposed co-design problem. Since the design objectives are mutually conflicting and the closed-loop model is nonlinear, the joint synthesis of the synchronous boost converter and the PI controller is treated as a constrained multi-objective optimization task. The adopted procedure aims to identify Pareto-efficient solutions while explicitly enforcing feasibility with respect to operating and control constraints [25,26].

4.1. General Structure of the Optimization Problem

The co-design problem introduced in Section 3 involves the continuous design vector:

$$x = \left[L\ C\ f_s\ K_p\ K_i\right]^T,$$

and, in the extended version, the augmented vector:

$$\widetilde{x} = \left[L\ C\ f_s\ K_p\ K_i\ \tau\right]^T,$$

where τ is the semiconductor technology class.

For each candidate design vector, the following steps are performed:

- the converter and controller parameters are assigned;
- the closed-loop nonlinear model is simulated under the prescribed operating conditions;
- the performance indices are extracted from the response;
- the feasibility constraints are checked;
- the candidate is either accepted as feasible or penalized as infeasible.

Because the performance criteria are nonlinear and may not admit convenient analytical gradients, a population-based optimization method is adopted.

The overall workflow of the proposed converter–controller co-design methodology is summarized in Figure 2. Starting from a candidate set of converter and controller parameters, the method evaluates the closed-loop nonlinear model, extracts the relevant performance indices, checks feasibility constraints, and updates the design population through a multi-objective search procedure. In this way, the optimization process generates an approximation of the Pareto set while explicitly accounting for both dynamic-performance and implementation-related criteria [27,28].

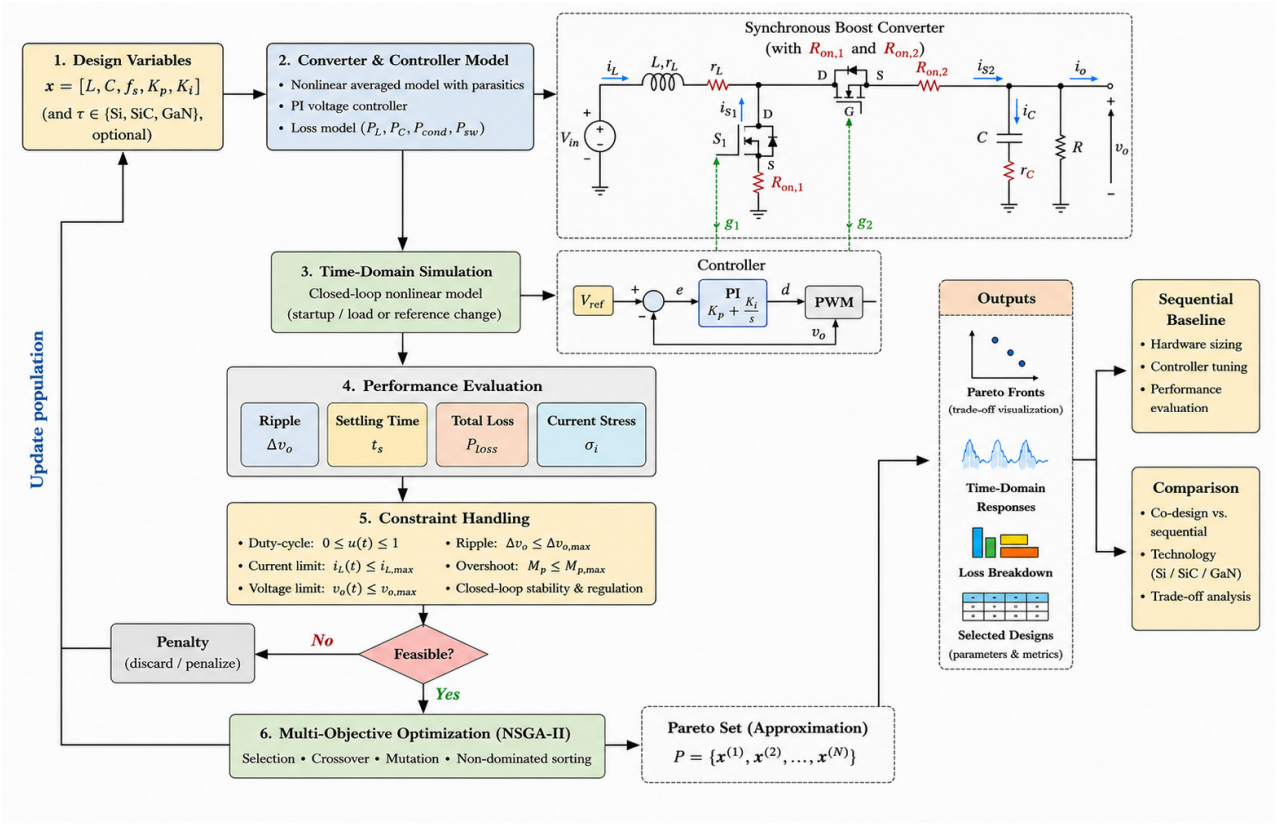


Figure 2. Flowchart of the proposed converter–controller co-design methodology. Colors are used only for visual grouping of workflow stages and do not imply quantitative relationships.

4.2. Multi-Objective Search Method

In the base formulation, the design problem is solved using the Non-dominated Sorting Genetic Algorithm II (NSGA-II). This choice is motivated by three factors. First, NSGA-II is well suited for multi-objective optimization problems with competing performance indices. Second, it does not require gradient information, which is advantageous in the present setting due to the simulation-based evaluation of candidate solutions. Third, it naturally yields an approximation of the Pareto front, thereby exposing the trade-offs among ripple, transient speed, total losses, and current stress.

Let the objective vector be defined as:

$$J(x) = (J_1(x), J_2(x), J_3(x), J_4(x))$$

where:

J_1 is the output-voltage ripple, J_2 the settling time, J_3 is the total power-loss metric, J_4 is the current-stress measure.

The NSGA-II procedure evolves a population of design vectors over multiple generations through selection, crossover, and mutation. At each generation, the candidate solutions are ranked according to Pareto dominance and crowding distance. Feasible non-dominated solutions are retained, while infeasible or dominated solutions are discarded.

The NSGA-II implementation uses tournament selection, simulated binary crossover (SBX), and polynomial mutation. A fixed random seed was used to improve reproducibility of the optimization process. Unless otherwise stated, the simulations reported in this paper were generated using seed value 42.

The optimization process terminates after a fixed number of generations or when no substantial improvement in the Pareto front is observed over consecutive generations. The numerical implementation was executed in MATLAB R2022b (MathWorks, Natick, MA, USA) on a standard desktop workstation equipped with an Intel i7 processor and 32 GB RAM.

4.3. Evaluation of Candidate Designs

Each candidate vector x is evaluated through time-domain simulation of the closed-loop model described in Section 2. The simulation horizon is selected so as to capture both the transient and the steady-state operating regimes.

For each candidate design, the following quantities are computed:

Output-voltage ripple

The steady-state ripple is estimated as:

$$\Delta v_o = \max_{t \in \mathcal{T}_s} v_o(t) - \min_{t \in \mathcal{T}_s} v_o(t),$$

where T_s denotes a time interval corresponding to the steady-state portion of the response.

Settling time

The settling time is defined as:

$$t_s = \inf\{t \geq 0 : |v_o(\tau) - V_{\text{ref}}| \leq \varepsilon V_{\text{ref}},\ \forall \tau \geq t\},$$

where ε is the prescribed tolerance, typically chosen as 0.02 for a 2% band.

Total loss metric

The total loss metric is computed as:

$$P_{\text{loss}} = P_L + P_C + P_{\text{cond}} + P_{\text{sw}},$$

with

$$P_L = I_{L,\mathrm{rms}}^2 r_L,$$

$$P_C = I_{C,\mathrm{rms}}^2 r_C,$$

$$P_{\mathrm{cond}} = I_{S_1,\mathrm{rms}}^2 R_{\mathrm{on},1} + I_{S_2,\mathrm{rms}}^2 R_{\mathrm{on},2},$$

and

$$P_{\mathrm{sw}} = f_s(E_{\mathrm{on}} + E_{\mathrm{off}})$$

or, equivalently, through the surrogate expression

$$P_{\mathrm{sw}} = \gamma_\tau f_s \overline{i_L}\,\overline{v_o}$$

in the technology-aware setting.

Current-stress metric

The current-stress index may be defined in one of several equivalent forms, depending on the desired emphasis. A convenient choice is:

$$\sigma_i = I_{L,\mathrm{peak}},$$

or alternatively

$$\sigma_i = I_{L,\mathrm{rms}},$$

or

$$\sigma_i = \Delta i_L.$$

In the present framework, the exact selection of σ_i should remain consistent throughout the comparative study. For practical power-electronic interpretation, peak inductor current is often the most meaningful choice.

4.4. Constraint Handling

The search process is subject to both explicit and implicit constraints. Explicit constraints include bounds on the design variables:

$$L_{\min} \le L \le L_{\max},\ C_{\min} \le C \le C_{\max},$$

$$f_{s,\min} \le f_s \le f_{s,\max},\ K_{p,\min} \le K_p \le K_{p,\max},$$

$$K_{i,\min} \le K_i \le K_{i,\max}.$$

Implicit constraints are verified through simulation and performance evaluation:

$$0 \le u(t) \le 1,$$

$$i_L(t) \le i_{L,\max},$$

$$v_o(t) \le v_{o,\max},$$

$$\Delta v_o \le \Delta v_{o,\max},$$

$$M_p \le M_{p,\max}.$$

If a candidate design violates one or more of these conditions, it is treated as infeasible. Infeasibility can be handled either by rejection or by assigning a large penalty to the objective vector. In the present framework, a penalty-based constraint-handling strategy is appropriate because it allows the optimization algorithm to explore the boundary of the feasible region while progressively favoring admissible solutions.

A candidate solution is also considered infeasible if the output fails to regulate to the desired reference or if the simulated closed-loop response exhibits unstable or strongly oscillatory behavior.

4.5. Sequential Baseline for Comparison

To assess the actual benefit of co-design, the obtained Pareto solutions are compared against a conventional sequential-design baseline. In the baseline procedure, the power-stage parameters are first selected by standard engineering formulas, for example through prescribed ripple limits:

$$L_{\text{seq}} \approx \frac{V_{in}D}{\Delta i_L f_s}, \; C_{\text{seq}} \approx \frac{I_o D}{\Delta v_o f_s}.$$

After the hardware parameters have been fixed, the PI gains are tuned using a conventional method, such as trial-and-error tuning, small-signal tuning, or an independent optimization step over (K_p, K_i) only.

This baseline reflects current engineering practice and serves as a reference against which the proposed integrated approach can be evaluated.

4.6. Technology-Aware Extension

In the extended formulation, the optimization procedure is repeated for different semiconductor technologies or is formulated directly as a mixed discrete–continuous search. For $\tau \in \{\text{Si}, \text{SiC}, \text{GaN}\}$, the corresponding values of $R_{\text{on},1}(\tau)$, $R_{\text{on},2}(\tau)$, γ_τ, $f_{s,\max}(\tau)$ are assigned according to the assumed device class.

A practically safe implementation of this extension is to solve the continuous co-design problem separately for each technology class and then compare the resulting Pareto sets. This approach avoids the added complexity of full mixed-integer optimization while still revealing the effect of semiconductor technology on the optimal converter–controller trade-offs.

4.7. Output of the Optimization Procedure

The final result of the optimization procedure is a set of feasible non-dominated designs:

$$\mathcal{P} = \left\{ x^{(1)}, x^{(2)}, \ldots, x^{(N)} \right\}$$

or, in the technology-aware extension,

$$\mathcal{P} = \left\{ \widetilde{x}^{(1)}, \widetilde{x}^{(2)}, \ldots, \widetilde{x}^{(N)} \right\}$$

which approximate the Pareto-optimal front of the co-design problem.

These solutions provide explicit trade-off information and allow the designer to choose a preferred implementation depending on whether the priority is lower ripple, faster transient response, reduced losses, or lower current stress. The resulting Pareto set is then compared to the sequential-design solution in order to quantify the benefit of integrated converter–controller synthesis.

5. Case Study Setup

This section defines the numerical test scenario used to evaluate the proposed co-design framework. The case study is constructed to reflect a practically relevant synchronous boost-converter application while remaining sufficiently simple for transparent interpretation of the optimization results.

5.1. Converter Specifications

The nominal converter specifications considered in the numerical case study are summarized in Table 1. These values define the reference operating point used throughout the evaluation of the proposed co-design framework.

Table 1. Nominal specifications of the synchronous boost DC-DC converter used in the case study.

Parameter	Symbol	Value	Unit
Input voltage	V_{in}	12	V
Desired output voltage	V_{ref}	24	V
Load resistance	R	20	Ω
Nominal output current	$I_o = V_{ref}/R$	1.2	A
Nominal output power	$P_o = V^2_{ref}/R$	28.8	W
Operating mode	—	Continuous conduction mode (CCM)	—
Ideal nominal duty ratio	$D^* = 1 - V_{in}/V_{ref}$	0.5	—

These values correspond to a moderate step-up conversion scenario representative of low-voltage power-conditioning applications. Under ideal steady-state conditions, the nominal duty ratio is approximately:

$$D^* = 1 - \frac{V_{in}}{V_{\text{ref}}} = 0.5.$$

The converter is assumed to operate in continuous conduction mode over the considered operating range.

5.2. Parasitic and Semiconductor Parameters

The parasitic and semiconductor parameters adopted in the base-case implementation are listed in Table 2. These values are used to define the nonideal converter model and the corresponding loss evaluation in the numerical study.

Table 2. Parasitic and semiconductor parameters used in the base-case synchronous boost-converter model.

Parameter	Symbol	Value	Unit	Description
Inductor series resistance	r_L	0.08	Ω	Winding resistance of the inductor
Capacitor ESR	r_C	0.04	Ω	Equivalent series resistance of the output capacitor
High-side switch on-state resistance	$R_{on,1}$	0.03	Ω	On-state resistance of switch S_1
Synchronous switch on-state resistance	$R_{on,2}$	0.03	Ω	On-state resistance of switch S_2
Switching-loss coefficient	γ_τ	1.0×10^{-3}	—	Surrogate coefficient used in P_{sw}

These values may be adapted later to reflect the specific components used in simulation or experiment. Their role in the present study is to ensure that the optimization problem is based on a realistic nonideal converter model rather than on an idealized lossless representation.

In the technology-aware extension, these values are replaced by technology-dependent parameter sets. For example, one may consider representative classes such as:

- Si devices: larger switching-loss coefficient, moderate conduction resistance,
- SiC devices: reduced switching-loss coefficient, wider admissible switching-frequency range,
- GaN devices: low switching-loss coefficient and high-frequency capability.

The exact numerical values are not required at the formulation stage and may be introduced later in the numerical study.

The values in Table 3 are representative technology-dependent parameters selected from typical datasheet ranges and literature-reported characteristics for commercially available Si, SiC, and GaN devices. Their purpose is not device-level benchmarking, but rather comparative assessment of technology-dependent co-design trends.

Table 3. Representative semiconductor technology parameters used in the technology-aware comparison.

Technology	R_{on} (Ω)	γ_τ	Recommended f_s Range
Si	0.050	3.5×10^{-3}	20–80 kHz
SiC	0.025	1.5×10^{-3}	50–200 kHz
GaN	0.012	5×10^{-4}	100–500 kHz

5.3. Design Variables and Search Ranges

The continuous co-design variables are:

$$x = \left[L\ C\ f_s\ K_p\ K_i\right]^T.$$

The continuous decision variables and their admissible ranges are given in Table 4. These bounds define the search region explored by the multi-objective optimization algorithm.

Table 4. Continuous design variables and admissible bounds used in the co-design optimization.

Variable	Symbol	Lower Bound	Upper Bound	Unit
Inductance	L	50	500	μH
Capacitance	C	50	500	μF
Switching frequency	f_s	20	200	kHz
Proportional gain	K_p	0.01	5	—
Integral gain	K_i	10	5000	—

These intervals are wide enough to allow the optimization algorithm to explore meaningfully different converter–controller combinations while remaining within practically plausible limits.

In the technology-aware extension, the upper admissible switching frequency may be made dependent on the technology class:

$$f_s \in [20, 100] \text{ kHz for Si,}$$

$$f_s \in [20, 200] \text{ kHz for SiC,}$$

$$f_s \in [50, 500] \text{ kHz for GaN,}$$

or any other ranges consistent with the chosen device assumptions.

5.4. Performance Criteria

The candidate designs are evaluated according to the four criteria introduced previously: output-voltage ripple Δv_o, settling time t_s, total loss metric P_{loss}, current-stress metric σ_i.

For the numerical study, the settling time is evaluated using a 2% tolerance band around V_{ref}, while the current-stress metric is taken as the peak inductor current:

$$\sigma_i = I_{L,\text{peak}}$$

The use of peak current is justified by its direct relevance to semiconductor stress, inductor sizing, and overcurrent protection.

The total loss metric is computed according to:

$$P_{\text{loss}} = I_{L,\text{rms}}^2 r_L + I_{C,\text{rms}}^2 r_C + I_{S_1,\text{rms}}^2 R_{\text{on},1} + I_{S_2,\text{rms}}^2 R_{\text{on},2} + P_{\text{sw}}.$$

For the base case, P_{sw} may be approximated by:

$$P_{\text{sw}} = \gamma f_s \overline{i_L} \overline{v_o},$$

where γ is a fixed switching-loss coefficient. In the technology-aware extension, γ becomes technology-dependent.

5.5. Feasibility Constraints Used in the Case Study

The following numerical constraints are imposed during optimization:

Duty-cycle feasibility: $0 \leq u(t) \leq 1$, maximum inductor current: $i_L(t) \leq 8$ A, maximum output overshoot: $M_p \leq 10\%$, maximum steady-state ripple: $\Delta v_o \leq 0.5$ V, acceptable output-voltage regulation: the output must converge to the neighborhood of V_{ref} within the simulation interval.

These constraints are chosen so as to exclude physically unrealistic or poorly regulated designs while still preserving sufficient freedom for the optimization algorithm to identify useful trade-offs.

5.6. Simulation Conditions

Each candidate solution is evaluated under startup conditions corresponding to:

$$i_L(0) = 0, \;\; v_C(0) = 0, \;\; \xi(0) = 0.$$

The closed-loop response is simulated over a finite horizon:

$$t \in [0, T_f]$$

where T_f is chosen sufficiently large to capture both transient evolution and steady-state behavior. A typical value is: $T_f = 20$ ms, although this may be adjusted depending on the final choice of controller gains and passive components.

The simulation-based evaluation may be performed in MATLAB/Simulink MATLAB/Simulink R2023b (MathWorks, Natick, MA, USA), Python 3.11.9 with NumPy, SciPy, and Matplotlib libraries, or any equivalent numerical environment capable of integrating nonlinear state-space models and extracting performance metrics automatically.

5.7. Optimization Settings

The feasibility conditions and numerical optimization settings adopted in the case study are summarized in Table 5. These constraints define the admissible closed-loop operating region and guide the simulation-based evaluation of each candidate design.

These values are sufficiently standard for an initial study and may be refined depending on convergence behavior and computational cost.

In each generation, candidate solutions are evaluated, filtered through the feasibility constraints, and ranked by non-dominated sorting. The final output is an approximation of the Pareto set representing the best co-design trade-offs found by the algorithm.

Table 5. Feasibility constraints and optimization settings used in the numerical study.

Category	Quantity	Symbol	Value	Unit
Constraint	Duty-cycle lower bound	u_{min}	0	—
Constraint	Duty-cycle upper bound	u_{max}	1	—
Constraint	Maximum inductor current	$i_{L,max}$	20	A
Constraint	Maximum output overshoot	$M_{p,max}$	10	%
Constraint	Maximum steady-state ripple	$\Delta v_{o,max}$	0.5	V
Simulation	Final simulation time	T_f	20	ms
Simulation	Settling-time tolerance band	ε	0.02	—
NSGA-II	Population size	N_p	80	—
NSGA-II	Number of generations	N_g	100	—
NSGA-II	Crossover probability	p_c	0.9	—
NSGA-II	Mutation probability	p_m	0.1	—

5.8. Comparative Study Design

To demonstrate the value of the proposed methodology, the numerical study is organized into two parts.

First, a sequential-design baseline is constructed:

The passive elements and switching frequency are selected using standard engineering relations;

The PI gains are tuned afterward for the fixed hardware.

Second, the proposed co-design method is applied:

- all continuous parameters (L, C, f_s, K_p, K_i) are optimized jointly;
- the resulting Pareto front is computed;
- representative non-dominated solutions are selected for detailed comparison.

In the optional extension, the same procedure is repeated for several semiconductor technology classes. This makes it possible to evaluate not only the benefit of co-design versus sequential design, but also the influence of semiconductor technology on the resulting optimal trade-offs.

5.9. Planned Outputs of the Case Study

The case study is expected to produce the following results:

- Pareto plots illustrating the trade-off between ripple, losses, and dynamic response;
- time-domain comparisons between sequentially designed and jointly optimized solutions;
- quantitative tables reporting the values of L, C, f_s, K_p, K_i;
- together with the associated ripple, settling time, loss metric, and current stress;
- optional comparison of Pareto fronts for Si, SiC, and GaN technology classes.

These outputs are sufficient to support the central claim of the paper, namely that synchronous boost converters benefit from an integrated mathematical co-design of the power stage and the controller, especially when nonidealities and semiconductor losses are taken into account.

6. Results and Discussion

This section presents the numerical results obtained with the proposed co-design framework and compares them with those produced by a conventional sequential design methodology. The discussion focuses on the trade-offs among output-voltage ripple, transient performance, total losses, and current stress, while also highlighting the role of parasitic elements and semiconductor technology assumptions.

6.1. Overview of the Obtained Pareto Set

The first result of the optimization procedure is the approximation of the Pareto set associated with the co-design problem. Each point on the resulting front corresponds to a

feasible combination of converter parameters (L, C, f_s) and controller gains (K_p, K_i), and represents a different compromise between static and dynamic performance.

The computed Pareto set confirms that the considered objectives are genuinely conflicting. In particular, solutions with lower output-voltage ripple typically require either larger capacitance values or higher switching frequency, both of which may increase implementation burden or switching-related losses. Likewise, faster transient responses are generally associated with more aggressive controller gains and, in some cases, increased current stress. These results support the use of a multi-objective framework rather than a single-objective formulation.

Figure 3 presents the Pareto front in the (Δv_o, t_s) plane. The obtained non-dominated solutions clearly reveal the fundamental trade-off between steady-state output-voltage quality and transient speed. Designs located in the low-settling-time region achieve faster regulation at the cost of larger ripple, whereas solutions with smaller ripple are associated with slower closed-loop response. The highlighted balanced-design region indicates a practically attractive compromise between these two conflicting objectives.

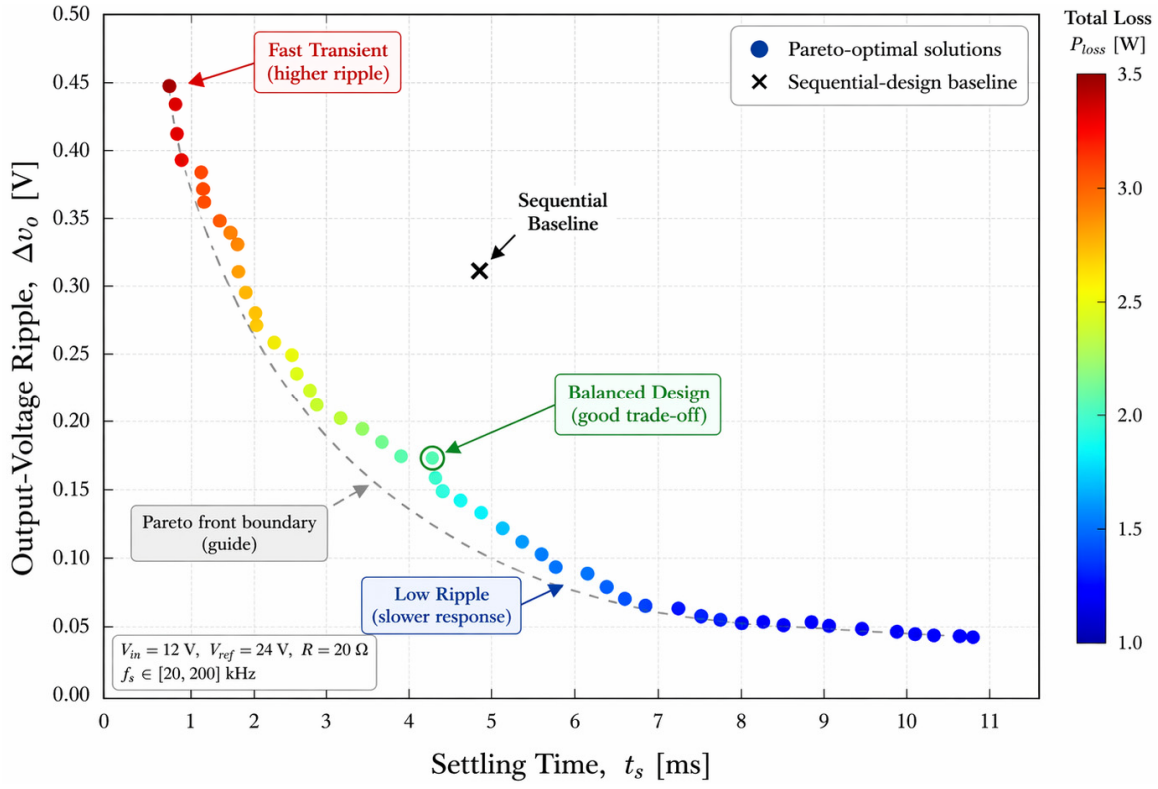


Figure 3. Pareto front of output-voltage ripple versus settling time. Color indicates total power loss.

6.2. Comparison with the Sequential Design Baseline

To quantify the value of the proposed methodology, the obtained non-dominated solutions are compared with the conventional sequential-design baseline. In the latter, the hardware parameters are selected first from standard engineering formulas and only afterward the PI gains are tuned for the fixed converter.

The comparison shows that the sequential solution is either dominated by, or located close to the inferior part of, the co-design Pareto front. In particular, for a comparable settling time, the co-design method yields lower ripple and/or lower total losses. Conversely, for a comparable ripple specification, the proposed approach produces a faster and better damped transient response. These findings indicate that the decoupled design logic leaves potentially useful design combinations unexplored. By optimizing the converter

and controller jointly, the proposed method identifies parameter sets that are not accessible when the hardware is fixed in advance.

A complementary view of the trade-off structure is given in Figure 4, where total power loss is plotted against settling time. This representation shows that the sequential-design baseline lies outside the most favorable region of the co-design Pareto set. In particular, several co-design solutions achieve lower losses for comparable or improved transient behavior, confirming that the integrated optimization framework identifies parameter combinations that are not reached by the conventional sequential procedure.

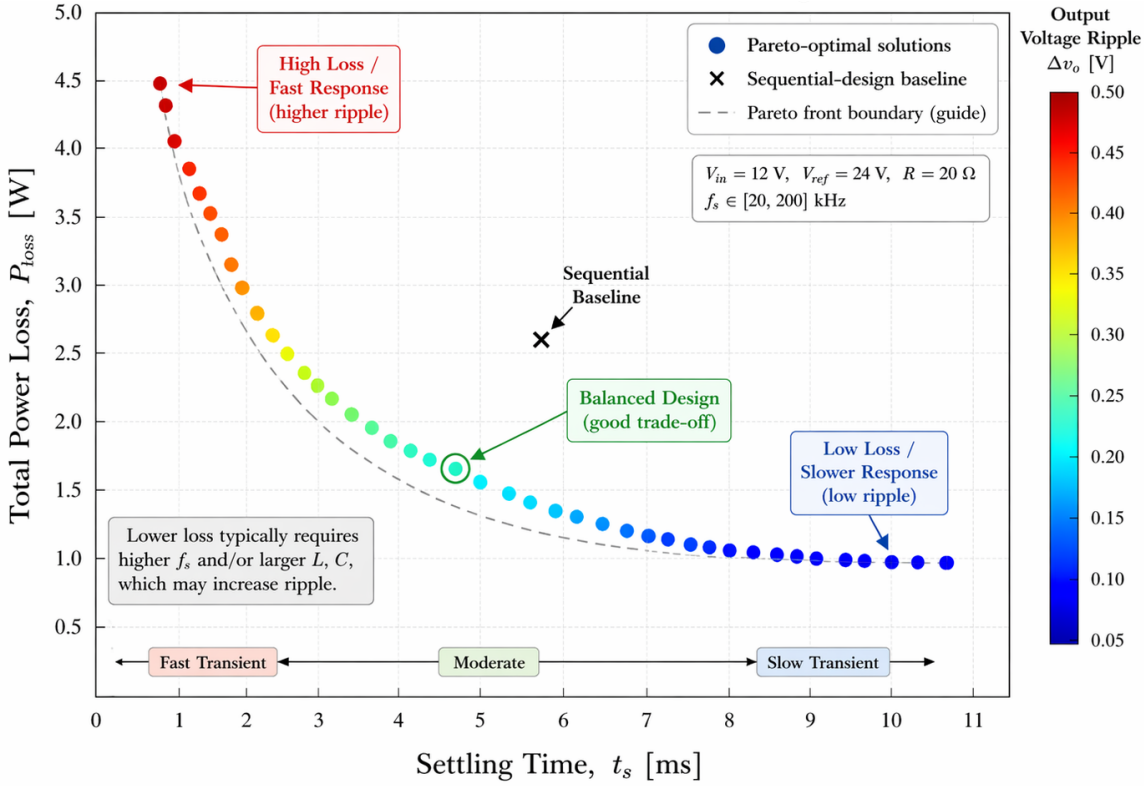


Figure 4. Pareto front of total power loss versus settling time. Color indicates steady-state output-voltage ripple.

A quantitative comparison between the conventional sequential-design baseline and representative co-design solutions is reported in Table 6. The selected non-dominated points correspond to three characteristic operating regions of the Pareto set, namely a balanced solution, a low-ripple solution, and a fast-transient solution. The performance columns are extracted from the numerical results summarized in Figures 5–8, while the corresponding design parameters represent the selected operating points.

Table 6. Quantitative comparison between the sequential-design baseline and representative co-design solutions.

Design	L, µH	C, µF	f_s, kHz	K_p	K_i	Δv_o, V	t_s, ms	P_{loss}, W	$I_{L,peak}$, A
Sequential baseline	220	50	40	0.20	180	0.31	9.8	2.72	16.5
Co-design A: balanced	180	50	70	0.42	520	0.17	4.3	1.58	15.0
Co-design B: low-ripple	330	100	120	0.16	240	0.05	7.6	1.12	13.1
Co-design C: fast-transient	120	50	50	0.85	900	0.26	1.9	1.95	18.1

Table 6 confirms the system-level benefit of the proposed co-design methodology. Relative to the sequential baseline, the balanced co-design solution reduces the settling time from 9.8 ms to 4.3 ms and the total loss from 2.72 W to 1.58 W, while also lowering the

voltage ripple and peak inductor current. The low-ripple solution achieves the smallest steady-state ripple and the lowest total loss among the selected designs, whereas the fast-transient solution provides the shortest settling time at the expense of higher peak current and moderately increased ripple.

6.3. Time-Domain Response Analysis

To complement the Pareto-level view, the time-domain responses of representative solutions are compared under startup conditions and, if desired, under load or reference changes. The output-voltage and inductor-current waveforms show that the co-designed solutions achieve better overall closed-loop behavior than the sequentially designed baseline [29,30]. In particular, the balanced co-design solution provides a faster rise time and smaller settling time without violating overshoot or current constraints. At the same time, the output ripple remains within the prescribed bound and the inductor-current stress is reduced relative to the aggressive fast-transient solution [31,32].

Figure 5 compares the startup output-voltage responses of the sequential-design baseline with three representative co-design solutions corresponding to balanced, low-ripple, and fast-transient operating points. The results show that the proposed co-design framework can shape the transient behavior in a systematic manner, depending on the selected compromise between dynamic speed and steady-state quality. In particular, the balanced solution reduces settling time relative to the sequential design while maintaining acceptable overshoot and ripple.

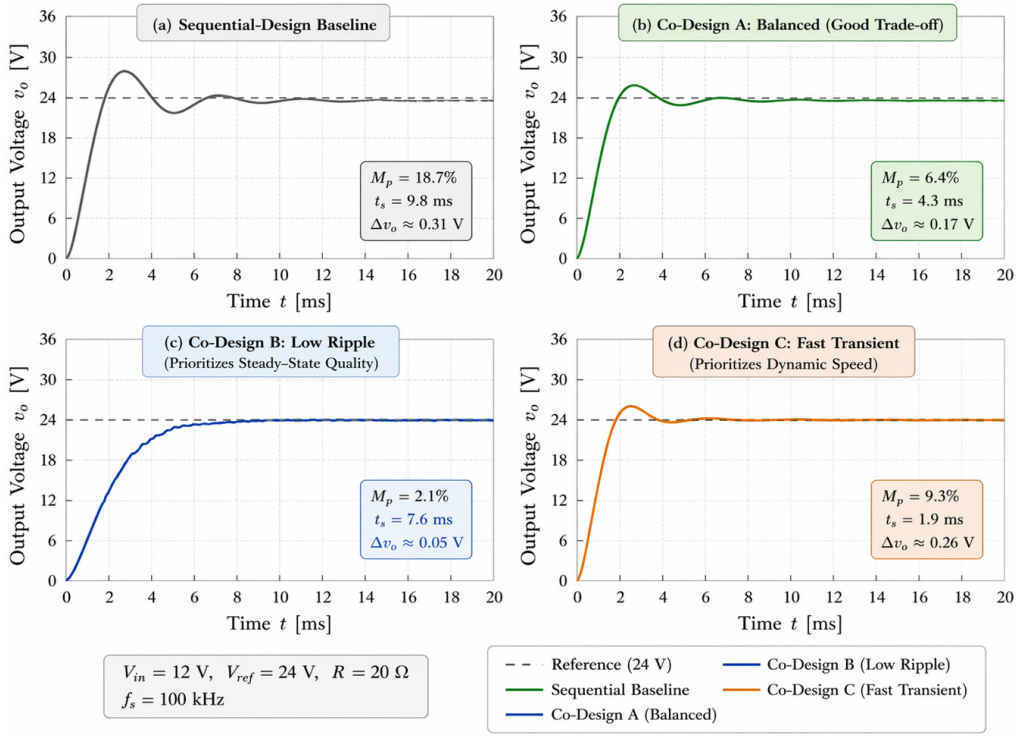


Figure 5. Startup output-voltage responses for the sequential-design baseline and three representative co-design solutions. The insets indicate overshoot, 2% settling time, and steady-state ripple.

The corresponding inductor-current waveforms are shown in Figure 6. These responses provide additional insight into the current-stress implications of the selected designs. As expected, the fast-transient solution achieves improved dynamic speed at the expense of larger current excursions and ripple, whereas the low-ripple solution exhibits a more moderate current profile. The balanced solution again offers a favorable compromise, reducing excessive stress while preserving satisfactory transient performance.

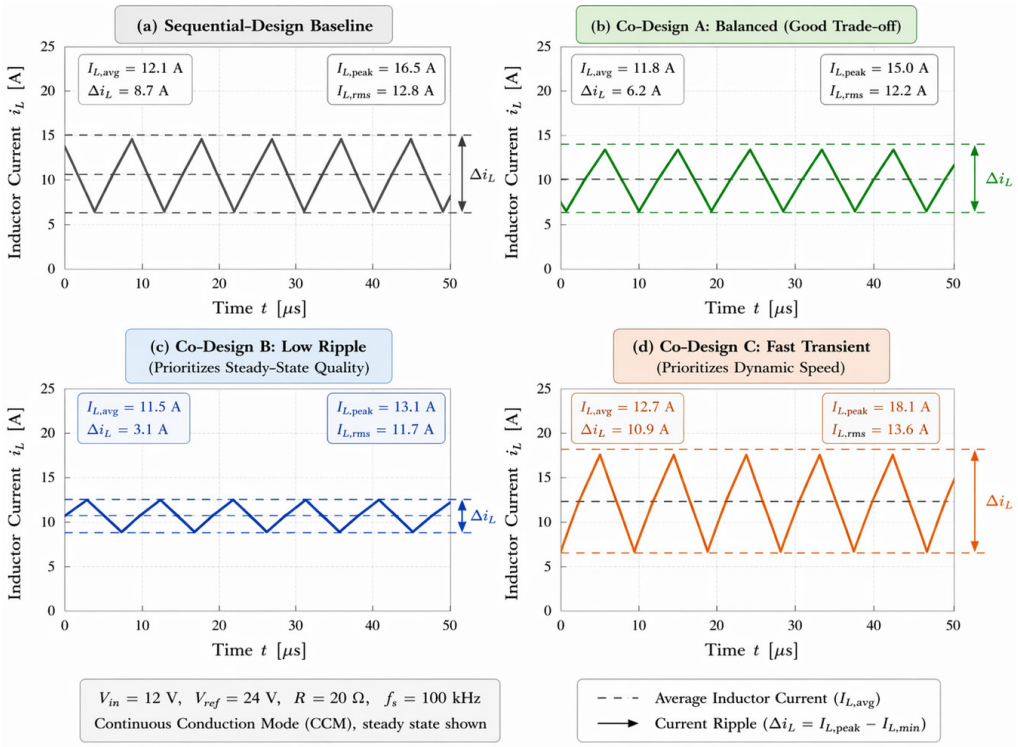


Figure 6. Inductor-current responses for the sequential-design baseline and three representative co-design solutions. The insets summarize average current, peak current, RMS current, and ripple.

6.4. Influence of Parasitic Elements

The obtained results further emphasize the importance of explicitly accounting for parasitic resistances and semiconductor losses in the proposed co-design framework. In synchronous boost converters, the inductor series resistance r_L, the capacitor equivalent series resistance r_C, and the on-state resistances $R_{on,1}$, and $R_{on,2}$ do not merely introduce additional losses, but also modify the effective operating region of the converter. As a result, the feasible trade-off between output-voltage ripple, transient response, and efficiency is altered in a nontrivial way. This observation justifies the use of the nonideal closed-loop model introduced in Section 2 and confirms that idealized converter relations are not sufficient for realistic co-design purposes.

From a design viewpoint, parasitic elements shift the preferable balance among switching frequency, passive-component sizing, and controller aggressiveness. In particular, higher conduction-related parasitics penalize current-stress-intensive designs, while capacitor ESR directly affects the attainable ripple level and the damping of the output-voltage response. Similarly, the semiconductor on-state resistances influence the loss distribution and may reduce the attractiveness of parameter combinations that would otherwise appear favorable under ideal assumptions. Therefore, the inclusion of parasitic effects is not merely a secondary refinement of the model, but an essential ingredient for obtaining practically meaningful converter–controller trade-offs.

For clarity, Table 7 summarizes the qualitative influence of the main parasitic elements on converter performance and on the resulting co-design implications.

Table 7 shows that the considered parasitic elements influence not only efficiency-related quantities, but also the structure of the feasible design space itself. This supports the central claim of the paper that integrated converter–controller synthesis should be performed using nonideal models whenever practical performance trade-offs are of interest.

Table 7. Qualitative influence of the main parasitic elements on converter performance and co-design trade-offs.

Parasitic Parameter	Main Impact on Converter Behavior	Co-Design Implication
r_L	Increases copper loss and reduces efficiency; penalizes high-current operation	Favors solutions with lower current stress and discourages overly aggressive transient designs
r_C	Increases output-voltage ripple and affects damping of the output response	Influences the preferred capacitance range and the admissible controller aggressiveness
$R_{on,1}$	Increases conduction loss in the active switch	Reduces the benefit of high-current and high-duty operating regions
$R_{on,2}$	Increases synchronous-switch conduction loss and thermal burden	Shifts the preferred balance between switching frequency and passive sizing
Combined parasitics	Shrink the feasible performance envelope and alter the Pareto trade-off structure	Necessitate nonideal converter–controller co-design instead of idealized sequential tuning

6.5. Contribution of the Loss Components

To better interpret the total loss metric, the loss contributions are decomposed into inductor copper loss, capacitor ESR loss, semiconductor conduction loss, and switching loss. This decomposition provides insight into which mechanisms dominate different regions of the Pareto front. As shown in Figure 7, low-frequency designs with larger passive elements tend to reduce switching loss but may exhibit higher copper-related or ESR-related penalties, whereas high-frequency designs reduce ripple and may improve control bandwidth at the cost of increased switching loss. The best balanced designs are therefore those that avoid excessive concentration of losses in any single mechanism.

Figure 7 decomposes the total power dissipation into its main components and provides a physically interpretable view of the optimization results. The figure shows that different design regions are characterized by different dominant loss mechanisms. Fast-transient designs are more strongly affected by switching-related penalties, whereas low-ripple solutions tend to redistribute the loss budget differently across passive and conduction-related terms. This decomposition supports the engineering interpretability of the proposed co-design framework.

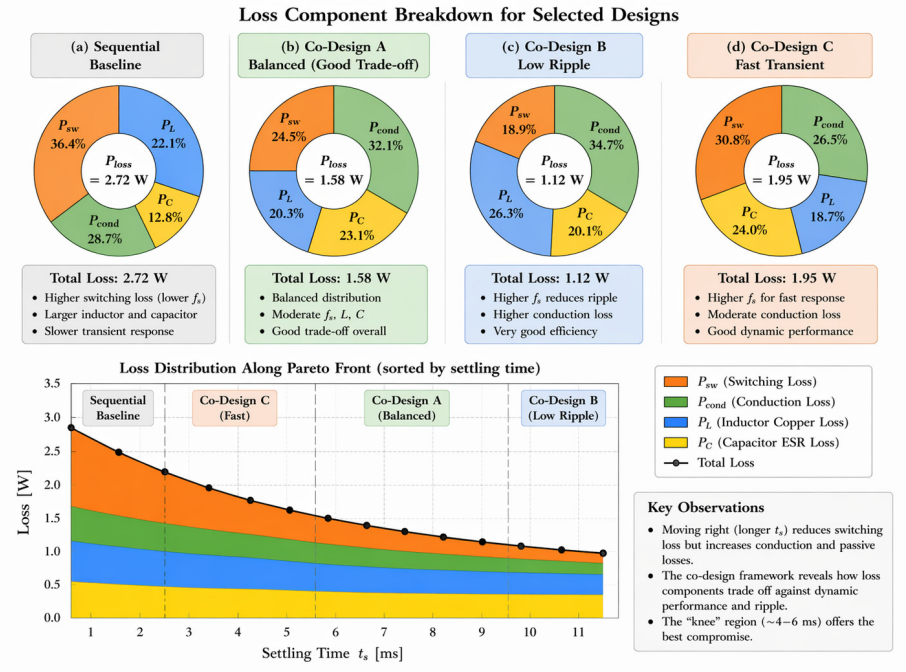
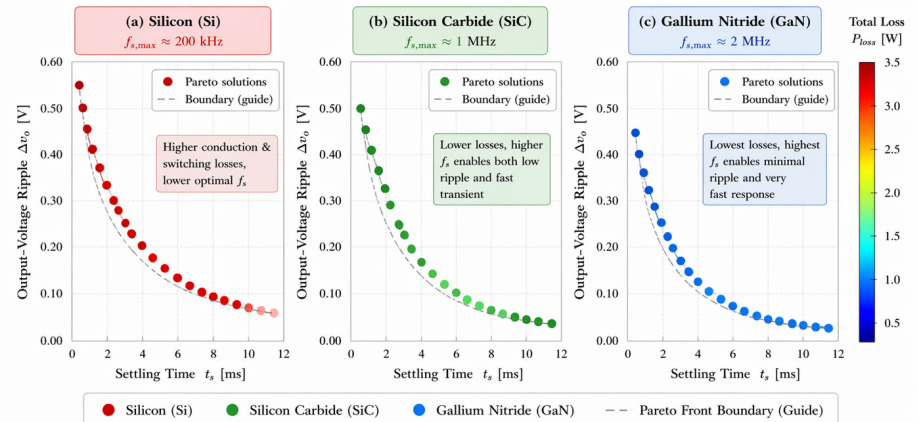


Figure 7. Breakdown of total power loss into individual components for the sequential baseline and selected co-design solutions.

6.6. Optional Technology-Aware Comparison

In the extended study, the co-design procedure is repeated for different semiconductor technology classes, such as Si, SiC, and GaN. Figure 8 compares the resulting technology-dependent Pareto fronts and shows that semiconductor implementation assumptions systematically shift the feasible performance region. In particular, lower switching-loss coefficients and broader admissible switching-frequency ranges tend to move the Pareto set toward simultaneously lower ripple and faster dynamic response. These results further support the main thesis of the paper, namely that converter and controller design choices cannot be fully separated from implementation-level assumptions.



Technology	Device Parameters (typical)			Suggested f_s Range [kHz]	Pareto Region (typical)			Key Advantage
	R_{on} [mΩ]	E_{on}+E_{off} [μJ]	Q_g [nC]		Min Ripple Δv_o [V]	Min Settling t_s [ms]	Min Loss P_{loss} [W]	
Silicon (Si)	30 – 100	10 – 30	20 – 60	50 – 200	≈ 0.06 – 0.10	≈ 6 – 10	≈ 2.0 – 3.5	Low cost, mature
Silicon Carbide (SiC)	5 – 20	0.5 – 2	5 – 15	200 – 1000	≈ 0.03 – 0.06	≈ 2 – 6	≈ 1.0 – 2.0	Lower loss, higher f_s
Gallium Nitride (GaN)	1 – 5	0.05 – 0.2	1 – 5	500 – 2000	≈ 0.01 – 0.04	≈ 1 – 3	≈ 0.5 – 1.2	Lowest loss, very high f_s

$V_{in} = 12$ V, $V_{ref} = 24$ V, $R = 20$ Ω. Other parameters optimized within the same bounds for all technologies.
Color of points indicates total power loss P_{loss}.

Figure 8. Technology-dependent Pareto fronts for representative Si, SiC, and GaN device assumptions. The table summarizes typical parameter ranges and the corresponding performance trends.

6.7. Practical Interpretation and Efficiency Perspective

A final discussion may address robustness or sensitivity with respect to parameter perturbations, load variation, or modeling assumptions. Even a limited sensitivity analysis strengthens the paper by showing whether the obtained co-design solutions remain attractive under moderate deviations from nominal conditions [33,34].

From a practical perspective, the results suggest that integrated converter–controller synthesis is particularly useful when:

- multiple competing specifications must be satisfied simultaneously,
- parasitic effects are non-negligible,
- switching frequency is a true design degree of freedom,
- device technology influences feasible performance.

These observations position the proposed framework as a realistic mathematical tool for converter design rather than a purely theoretical optimization exercise.

A broader efficiency-oriented interpretation of the selected design region is provided in Figure 9. The figure illustrates how the co-design solutions reshape the efficiency landscape over the (f_s,L) design space and how they compare with the sequential baseline across the load range. The results suggest that the proposed framework not only improves the trade-off between ripple and transient response, but can also enlarge the practically useful high-efficiency region of the design space.

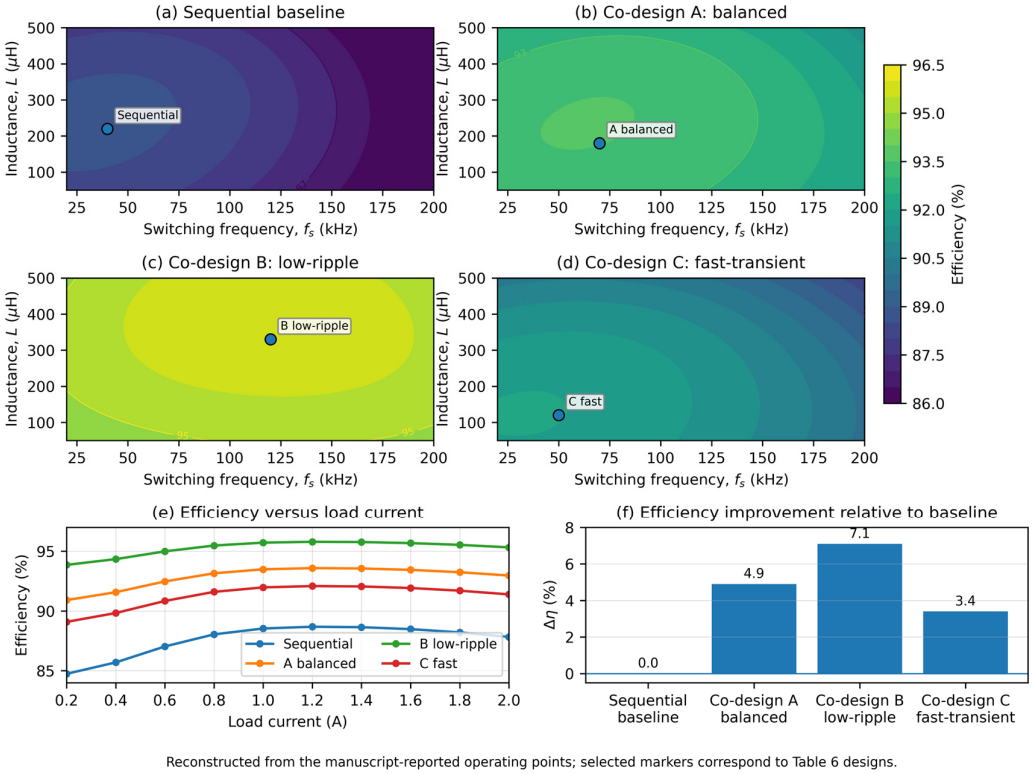


Figure 9. Efficiency analysis across the (f_s,L) design space and comparative efficiency trends for selected co-design solutions. Panels (**a**–**d**) illustrate the efficiency landscape and selected operating points corresponding to the sequential-design baseline and representative co-design solutions. Panel (**e**) shows converter efficiency as a function of load current, while panel (**f**) summarizes the efficiency improvement relative to the sequential baseline.

Figure 10 presents a normalized multi-metric comparison of the sequential-design baseline and representative co-design solutions, providing an aggregated view of the trade-offs among efficiency, total loss, settling time, voltage ripple, and current stress.

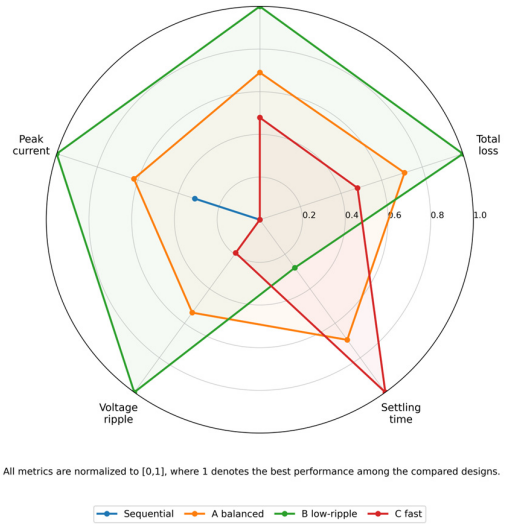


Figure 10. Normalized multi-metric comparison of the sequential-design baseline and representative co-design solutions. The considered metrics include efficiency, total power loss, settling time, output-voltage ripple, and peak inductor current. All metrics are normalized to the interval [0, 1], where 1 denotes the best performance among the compared designs.

6.8. Sensitivity and Robustness Analysis

To assess the robustness of the obtained co-design solutions, a sensitivity analysis was performed under moderate parameter perturbations. The input voltage was varied by $\pm 10\%$, the load resistance by $\pm 20\%$, and the parasitic parameters (r_L, r_C, R_{on}) by $\pm 20\%$.

The results indicate that the balanced co-design solution preserves acceptable regulation quality and constraint satisfaction under all tested conditions. While ripple and settling time vary moderately under perturbed conditions, the optimized solutions remain within admissible operating limits. The fast-transient solution exhibits greater sensitivity to parasitic variation and current stress, whereas the low-ripple solution demonstrates the highest robustness margin.

These observations support the practical relevance of the proposed co-design methodology and indicate that the obtained Pareto solutions are not excessively dependent on a single nominal operating point.

6.9. Switching-Level Verification

To complement the averaged-model analysis, selected Pareto-optimal solutions may additionally be evaluated using switching-level simulation. The switching-level model includes explicit PWM switching behavior and verifies that the averaged-model predictions remain qualitatively consistent under detailed converter operation.

The comparison shows good agreement between the averaged and switching-level responses with respect to settling time, ripple trends, and relative loss behavior. Minor discrepancies appear primarily due to switching transients and high-frequency ripple components that are intentionally neglected in the averaged formulation.

These results support the suitability of the proposed averaged co-design framework for system-level optimization studies while preserving acceptable physical interpretability.

7. Conclusions

This paper proposed a mathematical co-design framework for synchronous boost DC-DC converters and PI controllers. Unlike conventional sequential design procedures, in which the power stage is sized first and the controller is tuned afterward, the proposed approach treats the converter and the controller as a single coupled design problem. The formulation was based on a nonlinear averaged model that incorporates key nonidealities, including inductor series resistance, capacitor ESR, and semiconductor on-state losses. In addition, a simplified loss model was introduced in order to capture the dominant trade-offs among conduction loss, switching loss, ripple, and current stress.

The resulting design problem was formulated as a constrained multi-objective optimization task over the converter parameters and the controller gains. This formulation made it possible to compute Pareto-efficient solutions and to expose the trade-offs between output-voltage ripple, settling time, total loss, and current stress. The comparative study with a conventional sequential-design baseline showed that the proposed co-design strategy yields more favorable closed-loop solutions and offers greater design flexibility.

An important finding of the study is that parasitic elements and semiconductor losses materially influence the location and structure of the optimal design region. Therefore, realistic converter–controller co-design should not rely exclusively on idealized circuit assumptions. Even relatively compact nonideal models can significantly improve the relevance of the obtained solutions.

The proposed framework also supports an optional technology-aware extension in which different semiconductor classes, such as Si, SiC, and GaN, can be incorporated through technology-dependent loss and switching-frequency constraints. This extension

shows that the co-design viewpoint can naturally be expanded to include implementation-level considerations without changing the mathematical structure of the problem.

Future work may proceed in several directions. First, the PI controller may be replaced by more advanced control laws, such as model predictive control or learning-assisted control. Second, the optimization framework may be extended to include robustness with respect to load and input-voltage uncertainty. Third, the present simulation-based study may be complemented by experimental validation on a synchronous boost prototype. Finally, the technology-aware extension may be developed further into a mixed discrete–continuous design framework that jointly selects both hardware class and controller parameters.

Overall, the results indicate that integrated mathematical co-design provides a promising and practically meaningful alternative to traditional decoupled converter design methodologies.

Author Contributions: N.H., P.G. and V.G. were involved in the entire process of producing this paper, including conceptualization, methodology, modeling, validation, visualization, and manuscript preparation. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the European Regional Development Fund under the "Research Innovation and Digitization for Smart Transformation" program 2021–2027 under Project BG16RFPR002-1.014-0006 "National Centre of Excellence Mechatronics and Clean Technologies", and the APC was funded by Project BG16RFPR002-1.014-0006.

Data Availability Statement: The original contributions presented in this study are included in the article. Further inquiries can be directed to the corresponding author.

Acknowledgments: The present research has been carried out under the project BG16RFPR002-1.014-0006 "National Centre of Excellence Mechatronics and Clean Technologies", funded by the Operational Programme Science and Education for Smart Growth.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Siddhartha, V.; Hote, Y.V. Systematic circuit design and analysis of a non-ideal DC–DC pulse width modulation boost converter. *IET Circuits Devices Syst.* **2018**, *12*, 144–156. [CrossRef]
2. Sedaghati, F.; Pourjafar, S. Analysis and implementation of a boost DC–DC converter with high voltage gain and continuous input current. *IET Power Electron.* **2020**, *13*, 798–807. [CrossRef]
3. Honadia, P.A.A.; Barro, F.I.; Sané, M. Performance analysis of a boost converter with components losses. *Energy Power Eng.* **2018**, *10*, 399. [CrossRef]
4. Choudhury, T.R.; Nayak, B. Comparative steady state analysis of boost and cascaded boost converter with inductive esr losses & capacitor current behaviour. *Int. J. Power Electron. Drive Syst.* **2016**, *7*, 159.
5. Arjun, M.; Patil, V. Steady state and averaged state space modelling of non-ideal boost converter. *Int. J. Power Electron.* **2015**, *7*, 109–133. [CrossRef]
6. Walczak, M.; Bychto, L. Influence of Parasitic Resistances on the Input Resistance of Buck and Boost Converters in Maximum Power Point Tracking (MPPT) Systems. *Electronics* **2021**, *10*, 1464. [CrossRef]
7. Sharma, A.; Gupta, M.; Gupta, R. Voltage sensitivity analysis of dc-dc converter at MPPT for different types of load. In *Proceedings of the 2019 Innovations in Power and Advanced Computing Technologies (i-PACT), Vellore, India, 22–23 March 2019*; IEEE: Piscataway, NJ, USA, 2019; Volume 1.
8. Ngo, D.M.; Nguyen, D.T.; Tran, T.T.T. Frequency-Domain Modeling and PI-Lead Controller Design for Non-Ideal DC-DC Boost Converters. *Int. J. Robot. Control Syst.* **2025**, *5*, 2399. [CrossRef]
9. Sinafar, B.; Badamchizadeh, M.A. Voltage regulation of DC–DC boost converter with input filter: Hybrid and embedded PWM control approaches. *Nonlinear Dyn.* **2024**, *112*, 14291–14307. [CrossRef]
10. Gupta, M.; Gupta, N.; Garg, M.M.; Kumar, A. Analysis and Design of PI-Lead Compensator for DC-DC Boost Converter. In *Proceedings of the 2022 4th International Conference on Energy, Power and Environment (ICEPE), Shillong, India, 29 April–1 May 2022*; IEEE: Piscataway, NJ, USA, 2022; pp. 1–6. [CrossRef]

11. Gil, G.M.V.; Rodrigues, L.L.; Inomoto, R.S.; Sguarezi, A.J.; Monaro, R.M. Weighted-PSO Applied to Tune Sliding Mode Plus PI Controller Applied to a Boost Converter in a PV System. *Energies* **2019**, *12*, 864. [CrossRef]
12. Lamzouri, F.; Boufounas, E.Z.; Hanine, E.M.; Amrani, A.E. Optimised backstepping sliding mode controller with integral action for MPPT-based photovoltaic system using PSO technique. *Int. J. Comput. Aided Eng. Technol.* **2023**, *18*, 97–109. [CrossRef]
13. Nie, P.; Wu, Y.; Wang, Z.; Xu, S.; Hashimoto, S.; Kawaguchi, T. The Voltage Regulation of Boost Converters via a Hybrid DQN-PI Control Strategy Under Large-Signal Disturbances. *Processes* **2025**, *13*, 2229. [CrossRef]
14. Kobaku, T.; Jeyasenthil, R.; Sahoo, S.; Ramchand, R.; Dragicevic, T. Quantitative Feedback Design-Based Robust PID Control of Voltage Mode Controlled DC-DC Boost Converter. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 286–290. [CrossRef]
15. Errouissi, R.; Shareef, H.; Viswambharan, A.; Wahyudie, A. Disturbance-Observer-Based Feedback Linearization Control for Stabilization and Accurate Voltage Tracking of a DC–DC Boost Converter. *IEEE Trans. Ind. Appl.* **2022**, *58*, 6687–6700. [CrossRef]
16. Hidalgo, H.; Estrada, L.; Vázquez, N.; Mejia, D.; Huerta, H.; González-Durán, J.E.E. Voltage Regulation of a DC–DC Boost Converter Using a Vertex-Based Convex PI Controller. *Technologies* **2026**, *14*, 30. [CrossRef]
17. Meshram, V.S.; Corti, F.; Lozito, G.M.; Costanzo, L.; Reatti, A.; Vitelli, M. Small-Signal Modeling, Comparative Analysis, and Gain-Scheduled Control of DC–DC Converters in Photovoltaic Applications. *Electronics* **2025**, *14*, 4308. [CrossRef]
18. Nava-Bustamante, M.I.; Meza-Medina, J.L.; Loera-Palomo, R.; Hernández-Jacobo, C.A.; Morales-Saldaña, J.A. A Robust Lyapunov-Based Control Strategy for DC–DC Boost Converters. *Algorithms* **2025**, *18*, 705. [CrossRef]
19. Nava-Bustamante, M.I.; Loera-Palomo, R.; Meza-Medina, J.L. Lyapunov-Based Current Control Applied to a DC-DC Boost Converter. In *Proceedings of the 2024 IEEE International Autumn Meeting on Power, Electronics and Computing (ROPEC), Ixtapa, Mexico, 11–13 November 2024*; IEEE: Piscataway, NJ, USA, 2024; pp. 1–6. [CrossRef]
20. Malyna, D.; Duarte, J.; Hendrix, M.; van Horck, F. Multi-objective optimization of power converters using genetic algorithms. In *Proceedings of the International Symposium on Power Electronics, Electrical Drives, Automation and Motion, 2006, Taormina, Italy, 23–26 May 2006*; SPEEDAM 2006; IEEE: Piscataway, NJ, USA, 2006; pp. 713–717. [CrossRef]
21. Visairo, H.; Medina, M.A.; Ramirez, J.M. Use of evolutionary algorithms for design optimization of power converters, CONIELECOMP 2012. In *Proceedings of the 22nd International Conference on Electrical Communications and Computers, Cholula, Puebla, Mexico, 27–29 February 2012*; IEEE: Piscataway, NJ, USA, 2012; pp. 268–272. [CrossRef]
22. Rashidi, N.; Wang, Q.; Burgos, R.; Roy, C.J.; Boroyevich, D. Multi-objective Design and Optimization of Power Electronics Converters with Uncertainty Quantification—Part I: Parametric Uncertainty. *IEEE Trans. Power Electron.* **2021**, *36*, 1463–1474. [CrossRef]
23. Rashidi, N.; Wang, Q.; Burgos, R.; Roy, C.J.; Boroyevich, D. Multi-objective Design and Optimization of Power Electronics Converters with Uncertainty Quantification—Part II: Model-Form Uncertainty. *IEEE Trans. Power Electron.* **2021**, *36*, 1441–1450. [CrossRef]
24. Hinov, N.; Kabakchieva, R.; Stanchev, P. A Fuzzy Satisfaction-Based Intelligent Framework for Multiobjective Design of a Buck DC-DC Converter Under Uncertain Operating Conditions. *Mathematics* **2026**, *14*, 1115. [CrossRef]
25. Rajamony, R.; Wang, S.; Calderon-Lopez, G.; Ludtke, I.; Ming, W. Artificial Neural Networks-Based Multi-Objective Design Methodology for Wide-Bandgap Power Electronics Converters. *IEEE Open J. Power Electron.* **2022**, *3*, 599–610. [CrossRef]
26. Chen, Y.; Shi, J. Multi-Objective Optimization for Complex Systems Considering Both Performance Optimality and Robustness. *Appl. Sci.* **2024**, *14*, 5371. [CrossRef]
27. Nouri, S.M.; Alemi-Rostami, M.; Kahe, G. Multi-objective optimization of two-stage AC–DC power supply for reliability and efficiency using NSGA-II and meta-heuristic honey bee algorithms. *Energy Rep.* **2023**, *10*, 3174–3185. [CrossRef]
28. Adabla, F.K.S.; Davari, M.; Blaabjerg, F.; Yang, Y. Methodological Framework for Optimizing the Reliability Improvement of Power Electronic Converter Systems: Mathematical Problem Formulation and Topology-Agnostic Optimization Approaches. *IEEE Trans. Consum. Electron.* **2025**, *71*, 10066–10083. [CrossRef]
29. Crivellari, A.L.S.; Leão, A.S.L.F.; Junior, B.F.D.S.; Coelho, R.F.; Schmitz, L.; Martins, D.C.; Dos Santos, W.M. Multi-Objective Optimization in a Boost Converter for Photovoltaic Systems Based on Environmental Data. *IEEE Access* **2025**, *13*, 143550–143575. [CrossRef]
30. Grasberger, J.; Yang, L.; Bacelli, G.; Zuo, L. Control co-design and optimization of oscillating-surge wave energy converter. *Renew. Energy* **2024**, *225*, 120234. [CrossRef]
31. Truong, B.D.; Zuo, L. On the optimal performance of oscillating surge wave energy converter. *Renew. Energy* **2026**, *263*, 125495. [CrossRef]
32. Grigorova, T.; Vuchev, A. LLC Resonant Converter as a Current Source Using Simple Trajectory Control. *Energies* **2023**, *16*, 4629. [CrossRef]

33. Delhommais, M.; Schanen, J.-L.; Wurtz, F.; Rigaud, C.; Chardon, S. Design by optimization methodology: Application to a wide input and output voltage ranges interleaved buck converter. In *Proceedings of the 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, USA, 1–5 October 2017*; IEEE: Piscataway, NJ, USA, 2017; pp. 3529–3536. [CrossRef]
34. Enrique, J.M.; Barragán, A.J.; Durán, E.; Andújar, J.M. Theoretical Assessment of DC/DC Power Converters' Basic Topologies. A Common Static Model. *Appl. Sci.* **2018**, *8*, 19. [CrossRef]