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Mathematical Models of Critical Soft Error in Synchronous and Self-Timed Pipeline

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Abstract: This paper analyzes the impact of a single soft error on the performance of a synchronous and self-timed pipeline. A nuclear particle running through the integrated circuit body is considered the most probable soft error source. The existing estimates show that self-timed circuits offer an advantage in terms of single soft error tolerance. The paper proves these estimates on the basis of a comparative probability analysis of a critical fault in two types of pipelines. The mathematical models derived in the paper describe the probability of a critical fault depending on the circuit's characteristics, its operating discipline, and the soft error parameters. The self-timed pipeline operates in accordance with a two-phase discipline, based on the request–acknowledge interaction within the pipeline's stages, which provides it with increased immunity to soft errors. Quantitative calculations performed on the basis of the derived mathematical models show that the self-timed pipeline has about 6.1 times better tolerance to a single soft error in comparison to its synchronous counterpart. The obtained results are in good agreement with empirical estimates of the soft error tolerance level of synchronous and self-timed circuits.

Keywords: synchronous pipeline; self-timed pipeline; soft error tolerance; single soft error; probability; Gauss law distribution; stochastic mathematical model

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1. Introduction

The reliability of electronic equipment, including soft errors (SEs), is one of the most important characteristics of hardware, especially in adverse operating conditions. Cosmic rays, radiation, and nuclear particles are the causes of SEs in digital circuits in computing and control systems in most cases [1–3]. A soft error is expressed in the inversion of a signal logical level. It becomes critical if it leads to distortion of the initial data processing result or a pipeline stall.

Among all possible faults associated with external influences, SEs constitute the predominant part. Research has shown [1] that in integrated circuits, SEs are the cause of spacecraft on-board system failures in 95% of cases. With scaling down the design rules, the probability of SE occurrence increases [4], and SEs occur several orders of magnitude more often than failures [5]. A similar ratio of SEs and failures is observed in information systems [6]. Therefore, the development of methods for increasing the fault tolerance of digital circuit components and units is relevant and a priority. Soft error tolerance in this case is understood as the circuit's ability to continue correct operation when an SE occurs, without loss or corruption of the processed data.

Over the past few decades, the response of digital circuits to SEs has been actively studied [7–9], and methods for protecting against SEs have been developed [10–12]. To increase the circuit's immunity to SEs, correction codes [13,14], self-correcting circuits [15] providing automatic correction of SE-induced errors, electrical and time masking [16], and special circuit solutions for typical digital cells and units [17–21] are used. Methods to protect against SEs based on the circuit's hardware redundancy, such as duplication [22], tripling [23], and "M-of-N" voting [24], are very popular.

Hardware redundancy increases the level of digital circuit immunity to SEs by means of SE control and masking tools built into the circuit. Asynchronous circuits operating on the principles of request–acknowledge interactions are initially hardware redundant. This ensures the circuit's correct operation control [25–27]. Self-timed (ST) circuits, which belong to the subclass of quasi-delay-insensitive asynchronous circuits, have the maximum immunity to SEs with acceptable hardware costs [28,29]. Due to hardware redundancy, they demonstrate a higher fault tolerance level compared to synchronous and asynchronous counterparts [30].

Publications in recent years [30–32] have consider the digital circuit's SE tolerance "in the first approximation" based on speculative estimates of the digital circuit's response to an SE. References [33,34] use SE emulation to estimate fault tolerance, which allows critical circuit parts to be identified and the probability of SE propagation to the circuit's outputs to be determined using multiple modeling sessions. There are probabilistic methods that estimate the SE's observability [35,36] at the level of individual logical cells, large blocks, and systems [37,38]. They are similar to functional analysis and logical function system simulation.

This paper's objective is to construct a mathematical model for calculating the probability of a single SE turning into a critical fault in a digital synchronous and ST circuit at a constant nuclear particle flux density as the most dangerous source of SEs [39]. Qualitative estimates show that ST circuits have a much higher immunity level to SEs compared to their synchronous counterparts [30,40]. However, they are empiric and based on approximately accounting for the event probabilities accompanying the SE's occurrence and its propagation throughout the circuit. In particular, to calculate the probability, a speculative analysis of the outcome binary "tree" of the specified events is used, in which each outcome has a probability of 0.5. This article solves the current problem of theoretically assessing the probability of a critical SE occurrence by constructing a mathematical model for synchronous and ST pipelines. The proposed model can be used to determine and compare the digital synchronous and ST circuits' SE tolerance levels.

The scientific novelty of the paper is as follows:

- Mathematical models of the critical SE occurrence caused by a nuclear particle run through the body of the circuit chip in the synchronous and ST pipeline stages were obtained.
- A comparative analysis of the synchronous and ST pipelines' SE tolerance was carried out based on analytical estimates, taking into account hardware costs for the typical parameter values of the circuit components and SE characteristics.

2. Statement of the Problem

Modern high-performance computing and control systems have a pipeline structure. Therefore, we chose synchronous and ST pipelines as the objects for constructing a critical SE mathematical model. Figure 1 shows a typical synchronous pipeline block diagram. Here, D_{in} is the input data; D_{out} is the output data; and Clk is the global clock signal. Figure 2 shows a typical ST pipeline block diagram. Here, Ack_i is the signal acknowledging

the completion of the phase transition in the first pipeline stage and Ack_o is the signal acknowledging the completion of the phase transition in the output data D_{out} receiver.

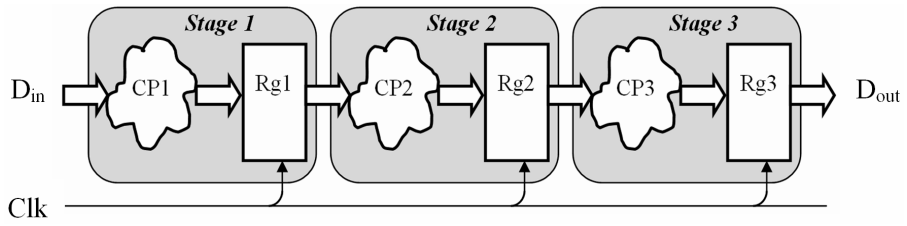


Figure 1. Block diagram of a synchronous pipeline.

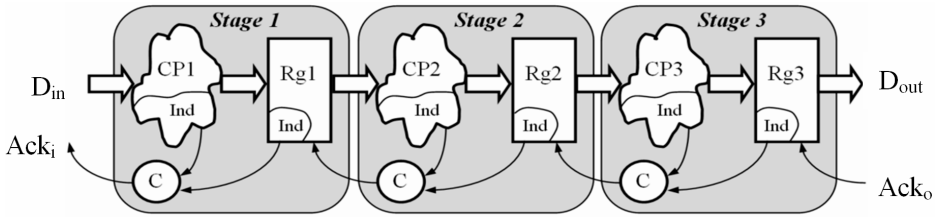


Figure 2. Block diagram of a self-timed pipeline.

The stages of both pipeline types consist of a combinational part (CP) and an output register (Rg). In the ST pipeline, the CP and register include an indication part (Ind), which generates signals acknowledging the CP and register switching completion to the current phase. The Muller's C-element [26] combines these signals into stage indication output. In the synchronous pipeline, the register bit is implemented on a D flip-flop, while in the ST pipeline it is implemented on two modified two-input C-elements [41].

The ST pipeline stage operates according to a two-phase discipline, including working and spacer phases [28]. It uses an indication subcircuit to detect the completion of all transitions, initiated during the stage switching to the current operation phase. The entire operating cycle of the ST pipeline stage can be divided into four consecutive intervals:

- Stage data output transition to a working phase (I_1);
- Stage's indication output working value generation (I_2);
- Stage data output transition to a spacer phase (I_3);
- Stage's indication output spacer value generation (I_4).

SEs can appear both in the CP stage and the register at any ST stage in the operation cycle interval. It becomes critical if it leads to pipeline output result corruption or "hanging" of the data processing, which is possible in the ST pipeline. The paper's purpose is to create a stochastic mathematical model of the occurrence of critical SEs in the synchronous and ST pipeline stages because of the impact of nuclear particles.

3. Initial Hypotheses

The development of critical fault mathematical models rests on the following initial hypotheses:

1. The density γ_{NP} of the nuclear particle flux that is the SE source is constant in time and within the pipeline layout area. The characteristics of the nuclear particle flux, including its density, depend on the circuit's operating conditions. The adopted assumption corresponds to the most practical applications.
2. Each nuclear particle causes the appearance of an SE, which is not necessarily critical, with probability P_{NP}, and at any moment in time no more than one SE is observed in the circuit. Such hypotheses average the conditions of an SE caused by an interaction

with the semiconductor, determined by the particle's incidence angle on the semiconductor's surface, its energy, the type of active semiconductor structure affected by the particle, and so on.

3. An SE's duration is described by the Gaussian law with the probability density function:

$$f(T_{SE}) = \frac{e^{-\frac{(T_{SE}-m_{SE})^2}{2\sigma_{SE}^2}}}{\sigma_{SE}\sqrt{2\pi}}, \quad (1)$$

where T_{SE} is the SE duration; m_{SE} is the mathematical expectation of T_{SE}; and σ_{SE} is the standard deviation of T_{SE}.

4. The average probability that stage CP does not mask an SE logically equals P_{NM}. In a specific circuit, this probability is determined by the circuit hardware complexity and the input data set processed by the circuit when a particle hits it. However, the accepted hypothesis allows one to draw a generalized conclusion in relation to a comparison of the synchronous and ST circuits' reactions to the SE's impact.

An SE's duration is mainly determined by the particle energy. This fact has predetermined the choice of Gauss' law to describe it. For example, in nuclear physics, Gauss's law describes the distribution of the mean track length of heavy charged particles in matter and the signal pulse amplitude recording the particle track, which are also determined by the particle energy [42]. The SE's duration is a positive value, so Gauss's law describes it with some error. Since the area of the figure bounded by the probability density function curve and the abscissa axis on the interval (0, ∞) is less than 1, this error is taken into account when calculating the SE probability using Equation (1) by means of a normalizing coefficient K_{err}:

$$K_{err} = 1 - \frac{1}{\sigma_{SE}\sqrt{2\pi}} \int_{-\infty}^{0} e^{-\frac{(x-m_{SE})^2}{2\sigma_{SE}^2}} dx. \quad (2)$$

If $m_{SE} > 3\sigma_{SE}$, then the error can be neglected (K_{err} = 1).

Based on the adopted initial hypotheses, let us estimate the probabilities of a critical SE occurring in the synchronous and ST pipeline stages depending on the SE's characteristics (duration, time, and place of occurrence) and the cell delay parameters of the analyzed stages.

4. Critical Soft Errors in the Synchronous Pipeline Stage

Let us introduce the set of variables that we operate with to estimate the SE probability in synchronous circuits, which is presented in Table 1. The performance reserve factor equals $k_P = \frac{T_{\max}}{T_C}$.

Table 1. Variables for calculating SE probability in synchronous circuits.

Variable	Name
Clock period	T_C
An SE's appearance time relative to the last active clock edge	t_S
Signal propagation delay from the faulty element to the stage register inputs	t_{DS}
Critical path delay of the stage's CP in the worst case	$T_{\max}$
Performance reserve factor	k_P
Inverter switching delay	t_I
Die area of the stage's CP	S_{CP_S}
Die area of the stage's register	S_{R_S}

It is assumed that t_S is uniformly distributed over the segment [0, T_C) and t_{DS} is uniformly distributed over the segment [0, $T_{\max}$). The zero value of t_{DS} corresponds to the SE in the stage's CP output cascade cell. In accordance with the hypothesis of fault source flow density immutability, the SE is written to the register if the following conditions are simultaneously met:

$$\begin{cases} T_{SE} > T_C - (t_S + t_{DS}), \\ t_S + t_{DS} < T_C. \end{cases}$$

The probability P_{S1} of the condition ($t_S + t_{DS} < T_C$) being fulfilled is estimated using the geometric method illustrated in Figure 3. It is expressed by the following formula:

$$P_{S1} = \frac{0.5{T_{\max}}^2 + T_{\max}(T_C - T_{\max})}{T_C T_{\max}} = 1 - \frac{T_{\max}}{2T_C} = 1 - 0.5k_P.$$

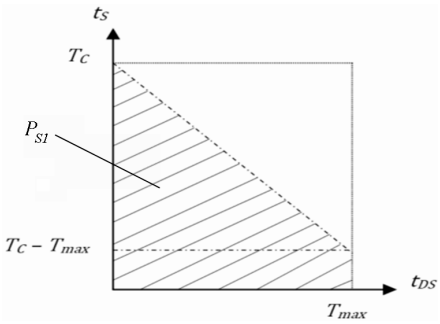


Figure 3. Condition $t_S + t_{DS} < T_C$ probability calculation.

It is a constant with fixed clock frequency values, supply voltage, and ambient temperature.

Then, an SE that hit the stage's CP enters the stage register with a probability whose integral function F_{CP_S} is described by the following formula:

$$F_{CP_S}(t_S, t_{DS}) = \frac{(1 - 0.5k_P)P_{NM}}{K_{err}} \left(1 - \frac{1}{\sigma_{SE}\sqrt{2\pi}} \int_0^{T_C - (t_S + t_{DS})} e^{-\frac{(x - m_{SE})^2}{2\sigma_{SE}^2}} dx \right). \quad (3)$$

The SE can hit the pipeline stage register. Taking into account the typical register bit circuit design as a D-flip–flop on bidirectional keys and inverters, the SE's uniform distribution in time and the independence of the SE's appearance in different nets of the register bit circuit, the integral function F_{R_S} of the probability of the critical SE's appearance in it is estimated using the following formula:

$$F_{R_S}(t_S) = \frac{1}{16} \left\{ \frac{5}{K_{err}} + 5 - \frac{1}{K_{err}\sigma_{SE}\sqrt{2\pi}} \left[3 \int_0^{T_C - t_S} e^{-\frac{(x - m_{SE})^2}{2\sigma_{SE}^2}} dx + 2 \int_0^{t_I} e^{-\frac{(x - m_{SE})^2}{2\sigma_{SE}^2}} dx \right] \right\}, \quad (4)$$

where t_I is the inverter switching delay.

In accordance with the hypothesis that only a single SE can be observed at any time, the events leading to the appearance of an SE in the CP or in the stage register are incompatible. The probability of a nuclear particle entering the CP or stage register area is directly proportional to the die area of the CP (S_{CP_S}) and the register (S_{R_S}). Then, the critical SE's total probability in a synchronous pipeline stage can be described by the integral probability function F_{CF_S}:

$$F_{CF_S}(t_S, t_{DS}) = \frac{S_{CP_S}}{(S_{CP_S}+S_{R_S})}\frac{(1-0.5k_P)P_{NM}}{K_{err}}\left[1-\frac{1}{\sigma_{SE}\sqrt{2\pi}}\int_0^{T_C-t_S-t_{DS}} e^{-\frac{(x-m_{SE})^2}{2\sigma_{SE}^2}}dx\right]+$$
$$+\frac{S_{R_S}}{16(S_{CP_S}+S_{R_S})}\left\{\frac{5}{K_{err}}+5-\frac{1}{K_{err}\sigma_{SE}\sqrt{2\pi}}\left[3\int_0^{T_C-t_S} e^{-\frac{(x-m_{SE})^2}{2\sigma_{SE}^2}}dx+2\int_0^{t_I} e^{-\frac{(x-m_{SE})^2}{2\sigma_{SE}^2}}dx\right]\right\}. \quad (5)$$

Let us introduce the Laplace integral function $\Phi(x)$ [43] into Equation (5) by substitution:

$$\frac{x-m_{SE}}{\sigma_{SE}} = u; dx = \sigma_{SE}du. \quad (6)$$

Then, Equation (5) changes to the formula:

$$F_{CF_S}(t_S, t_{DS}) = \frac{(1-0.5k_P)P_{NM}S_{CP_S}}{K_{err}(S_{CP_S}+S_{R_S})}\left[1-\Phi\left(\frac{T_C-t_S-t_{DS}-m_{SE}}{\sigma_{SE}}\right)-\Phi\left(\frac{m_{SE}}{\sigma_{SE}}\right)\right]+$$
$$+\frac{S_{R_S}}{16(S_{CP_S}+S_{R_S})}\left\{\frac{5}{K_{err}}+5-\frac{1}{K_{err}}\left[3\Phi\left(\frac{T_C-t_S-m_{SE}}{\sigma_{SE}}\right)+5\Phi\left(\frac{m_{SE}}{\sigma_{SE}}\right)+2\Phi\left(\frac{t_I-m_{SE}}{\sigma_{SE}}\right)\right]\right\}. \quad (7)$$

Formula (7) serves as a mathematical stochastic model of a critical SE in a synchronous pipeline stage caused by the impact of a nuclear particle running through the chip body. It has been obtained for the case of nuclear particle flow leading to the appearance of a single SE and allows one to estimate the probability of a critical SE depending on the SE's parameters, appearance, place, and time.

5. Critical Soft Errors in the Self-Timed Pipeline Stage

Self-timed circuits use redundant data encoding. Combinational ST circuits typically use dual-rail (DR) encoding with a spacer. The DR signal has two working states ("01" and "10") and one spacer state ("00" or "11"). The DR signal can switch into an antispacer state, opposite to the spacer, only under the influence of an SE. With a proper ST circuit layout design [30,44], the DR signal fault manifests itself as one of the following events:

- A working state instead of a spacer;
- A spacer instead of a working state;
- An antispacer instead of a spacer;
- An antispacer instead of a working state.

For simplicity, we assume that adjacent ST pipeline stages are well matched and have approximately the same performance. Let us introduce the set of variables we operate with to estimate the probability of an SE in ST circuits, which is presented in Table 2. This probability also depends on the following factors:

- A faulty subcircuit (stage CP or register);
- Correspondence of the DR signal's faulty state to the expected state in the current phase;
- The probability of writing a faulty DR signal into the stage register.

Assume that the occurrence time t_i, i = 1...4, is uniformly distributed over the interval [0, T_i), i = 1...4, and the time t_{DR} is uniformly distributed over the interval [0, T_j), j = {1; 3}. The t_{DR} and t_{NX} have fixed values under the given operating conditions.

Table 2. Variables for calculating SE probability in self-timed circuits.

Variable	Name
An SE's appearance time relative to the interval I_i beginning	t_i, i = 1...4
Interval I_i duration	T_i, i = 1...4
Faulty DR signal switching to the expected state	t_{DR}
Inclusive OR cell's switching delay	t_{NX}
C-element switching delay	t_{CE}
Die area of the stage's CP	S_{CP_ST}
Die area of the stage's register	S_{R_ST}
Die area of the entire ST pipeline stage	S_{A_ST}

In an ST pipeline, the probability that an SE that hit a pipeline stage becomes critical depends not only on the hit stage's response to the SE but also on its neighbors. In particular, maintaining the state of the current stage inputs during the SE action depends on the stage's indication subcircuit and the previous stage's register. Writing a faulty DR signal to the register of the current stage depends on the subsequent stage.

An SE, affecting the DR signal component in the ST pipeline stage's CP, can become critical only if the following conditions are simultaneously met:

$$\begin{cases} t_{CE} \le t_{DR} + t_i, i = \{1;3\}, \\ t_{NX} \le t_{DR} + t_i, i = \{1;3\}. \end{cases} \quad (8)$$

The probability of fulfilling each of the conditions in Equation (8) is estimated using the geometric method illustrated in Figure 4 for the SE at interval I_1. Here, t_x denotes t_{CE} or t_{NX}.

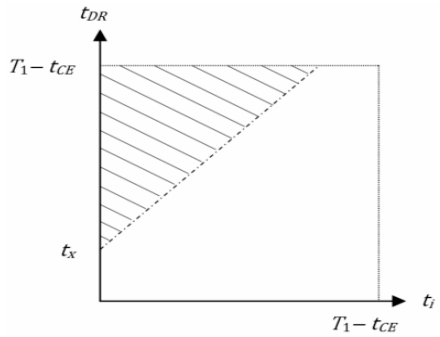


Figure 4. Condition $T_C > t_S + t_{DS}$ probability calculation (crosshatched region).

Let the ST pipeline stage CP and register indication subcircuits be implemented on three-input C-elements. The C-element masks the premature switching of one of its inputs in 75% of cases. Then, the probability function F_C of the C-element indicating a faulty DR signal prematurely switching to the expected state due to the SE is determined by the formula:

$$F_C(T_1) = \frac{(T_1 - 2t_{CE})^2 (T_1 - t_{CE} - t_{NX})^2}{4(T_1 - t_{CE})^4}, \quad (9)$$

Taking into account the request–acknowledge interaction of the ST pipeline stages and the CP and register die areas, the integral function F_{T1} of the probability of the critical SE's occurrence in the ST pipeline stage at interval I_1 equals:

$$F_{T1}(T_1, T_2) = \frac{{P_{NM}}^2 {F_C(T_1)}^2 (T_1 - 2t_{CE})^2 (3S_{CP_ST} + S_{R_ST})}{128(T_1 - t_{CE})^2 S_{A_ST} K_{err}} \left(1 - \frac{1}{\sigma_{SE}\sqrt{2\pi}} \int_0^{T_1+T_2-t_{CE}} e^{-\frac{(x-m_{SE})^2}{2\sigma_{SE}^2}} dx \right),$$

Note that S_{CP_ST} and S_{R_ST} do not take into account the indication subcircuit areas of the CP and register, since an SE's appearance in the indication subcircuit at interval I_1 is not critical.

At interval I_2, the outputs of this stage have already switched to the working state and initiated the subsequent stage transition to the working phase. Depending on the SE's appearance time t_2 and the place of its impact, it becomes critical with a probability described by the integral function F_{T2}:

$$F_{T2}(T_1, T_2, T_3, t_{DR}, t_2) = \frac{{P_{NM}}^2 S_{CP_ST}}{2S_{A_ST} K_{err}} \left(1 - \frac{1}{\sigma_{SE}\sqrt{2\pi}} \int_0^{T_1+T_2+t_{CE}-t_2} e^{-\frac{(x-m_{SE})^2}{2\sigma_{SE}^2}} dx \right) +$$
$$+ \frac{P_{NM}(T_2 - t_{NX})(T_2 - t_{CE}) S_{R_ST}}{2{T_2}^2 S_{A_ST} K_{err}} \left(1 - \frac{1}{\sigma_{SE}\sqrt{2\pi}} \int_0^{T_2+T_3+t_{CE}-t_2} e^{-\frac{(x-m_{SE})^2}{2\sigma_{SE}^2}} dx \right),$$

Interval I_3 combines the time of the current stage's CP outputs switching to the spacer and the time of writing the spacer onto the current stage register. Depending on the SE's appearance time t_3 and the place of its impact, it becomes critical with a probability described by the integral function F_{T3}:

$$F_{T3}(T_1, T_3, t_{DR}, t_3) = \frac{3{P_{NM}}^2 (2T_3 - T_1 - t_{CE})^2 S_{CP_ST}}{8T_3 S_{A_ST} K_{err}} \left(1 - \frac{1}{\sigma_{SE}\sqrt{2\pi}} \int_0^{T_3+t_{CE}-t_{DR}} e^{-\frac{(x-m_{SE})^2}{2\sigma_{SE}^2}} dx \right) +$$
$$+ \frac{P_{NM} S_{R_ST} T_3}{2S_{A_ST} K_{err}} \left(1 - \frac{1}{\sigma_{SE}\sqrt{2\pi}} \int_0^{T_1+t_{CE}-t_3} e^{-\frac{(x-m_{SE})^2}{2\sigma_{SE}^2}} dx \right).$$

An analysis of possible outcomes when an SE occurs at interval I_4 shows that none of them lead to a critical SE. In the worst case, they only cause a temporary suspension of the pipeline operation.

The events of a single SE occurrence in different ST pipeline cycle intervals are incompatible. Therefore, the total integral function of the probability of a critical SE occurrence in the ST pipeline stage equals the sum of the probability of an SE occurrence at individual intervals, weighted by the ratio of their durations to the total duration of all intervals:

$$F_{CF_ST}(T_1,T_2,T_3,t_{DR},t_2,t_3)=\frac{F_{T1}(T_1,T_2)T_1+F_{T2}(T_1,T_2,T_3,t_{DR},t_2)T_2+F_{T3}(T_1,T_3,t_{DR},t_3)T_3}{T_1+T_2+T_3+T_4}=$$
$$=\left[\frac{P_{NM}{}^2F_C(T_1)^2(T_1-2t_{CE})^2(3S_{CP_ST}+S_{R_ST})T_1}{128(T_1-t_{CE})^2S_{A_ST}K_{err}}\left(1-\frac{1}{\sigma_{SE}\sqrt{2\pi}}\int_0^{T_1+T_2+t_{CE}}e^{-\frac{(x-m_{SE})^2}{2\sigma_{SE}^2}}dx\right)+\right.$$
$$+\frac{P_{NM}{}^2S_{CP_ST}T_2}{2S_{A_ST}K_{err}}\left(1-\frac{1}{\sigma_{SE}\sqrt{2\pi}}\int_0^{T_1+T_2+t_{CE}+t_{DR}-t_2}e^{-\frac{(x-m_{SE})^2}{2\sigma_{SE}^2}}dx\right)+$$
$$+\frac{P_{NM}(T_2-t_{NX})(T_2-t_{CE})S_{R_ST}}{2T_2S_{A_ST}K_{err}}\left(1-\frac{1}{\sigma_{SE}\sqrt{2\pi}}\int_0^{T_2+T_3+t_{CE}-t_2}e^{-\frac{(x-m_{SE})^2}{2\sigma_{SE}^2}}dx\right)+ \quad (10)$$
$$+\frac{3P_{NM}{}^2(2T_3-T_1-t_{CE})^2S_{CP_ST}}{8T_3S_{A_ST}K_{err}}\left(1-\frac{1}{\sigma_{SE}\sqrt{2\pi}}\int_0^{T_3+t_{CE}-t_{DR}}e^{-\frac{(x-m_{SE})^2}{2\sigma_{SE}^2}}dx\right)+$$
$$\left.+\frac{P_{NM}S_{R_ST}T_3}{2S_{A_ST}K_{err}}\left(1-\frac{1}{\sigma_{SE}\sqrt{2\pi}}\int_0^{T_1+t_{CE}-t_3}e^{-\frac{(x-m_{SE})^2}{2\sigma_{SE}^2}}dx\right)\right]\frac{1}{(T_1+T_2+T_3+T_4)},$$

After moving to the Laplace integral function using the substituted Equations (6) and (9), we obtain:

$$F_{CF_ST}(T_1,T_2,T_3,t_2,t_3,t_{DR})=\left\{\frac{P_{NM}{}^2(T_1-t_{CE}-t_{NX})^4(T_1-2t_{CE})^6(3S_{CP_ST}+S_{R_ST})}{2048(T_1-t_{CE})^{10}S_{A_ST}}[1-\right.$$
$$-\Phi\left(\tfrac{T_1+T_2+t_{CE}-m_{SE}}{\sigma_{SE}}\right)-\Phi\left(\tfrac{m_{SE}}{\sigma_{SE}}\right)\Big]T_1+\left(\tfrac{P_{NM}^2}{2}\left[1-\Phi\left(\tfrac{T_1+T_2+t_{CE}+t_{DR}-t_2-m_{SE}}{\sigma_{SE}}\right)-\Phi\left(\tfrac{m_{SE}}{\sigma_{SE}}\right)\right]+\right.$$
$$+\tfrac{P_{NM}(T_2-t_{CE})(T_2-t_{NX})}{2T_2^2}\left[1-\Phi\left(\tfrac{T_3+T_2+t_{CE}-t_2-m_{SE}}{\sigma_{SE}}\right)-\Phi\left(\tfrac{m_{SE}}{\sigma_{SE}}\right)\right]\Big)\tfrac{S_{CP_ST}}{S_{A_ST}}T_2+ \quad (11)$$
$$+\left(\tfrac{3P_{NM}{}^2(2T_3-T_1-t_{CE})^2}{8T_3^2}\left[1-\Phi\left(\tfrac{T_3+t_{CE}-t_{DR}-m_{SE}}{\sigma_{SE}}\right)-\Phi\left(\tfrac{m_{SE}}{\sigma_{SE}}\right)\right]+\right.$$
$$\left.+\tfrac{P_{NM}}{2}\left[1-\Phi\left(\tfrac{T_1+t_{CE}-t_3-m_{SE}}{\sigma_{SE}}\right)-\Phi\left(\tfrac{m_{SE}}{\sigma_{SE}}\right)\right]\right)\tfrac{S_{R_ST}}{S_{A_ST}}T_3\Big\}\tfrac{1}{K_{err}(T_1+T_2+T_3+T_4)}.$$

Formula (11) serves as a mathematical probability model of a critical SE caused by a nuclear particle in the ST pipeline stage. It can be divided into two components that determine the probability of a critical SE in the stage CP (F_{CP_ST}) and register (F_{R_ST}):

$$F_{CP_ST}(T_1,T_2,T_3,t_2,t_{DR})=\left\{\frac{3(T_1-t_{CE}-t_{NX})^4(T_1-2t_{CE})^6}{1024(T_1-t_{CE})^{10}}\left[1-\Phi\left(\tfrac{T_1+T_2+t_{CE}-m_{SE}}{\sigma_{SE}}\right)-\Phi\left(\tfrac{m_{SE}}{\sigma_{SE}}\right)\right]T_1+\right.$$
$$+\left[1-\Phi\left(\tfrac{T_1+T_2+t_{CE}+t_{DR}-t_2-m_{SE}}{\sigma_{SE}}\right)-\Phi\left(\tfrac{m_{SE}}{\sigma_{SE}}\right)\right]T_2+ \quad (12)$$
$$\left.+\tfrac{3(2T_3-T_1-t_{CE})^2}{4T_3^2}\left[1-\Phi\left(\tfrac{T_3+t_{CE}-t_{DR}-m_{SE}}{\sigma_{SE}}\right)-\Phi\left(\tfrac{m_{SE}}{\sigma_{SE}}\right)\right]T_3\right\}\tfrac{S_{CP_ST}P_{NM}^2}{2S_{A_ST}K_{err}(T_1+T_2+T_3+T_4)},$$

$$F_{R_ST}(T_1,T_2,T_3,t_2,t_3)=\left\{\frac{P_{NM}(T_1-t_{CE}-t_{NX})^4(T_1-2t_{CE})^6}{1024(T_1-t_{CE})^{10}}\left[1-\Phi\left(\tfrac{T_1+T_2+t_{CE}-m_{SE}}{\sigma_{SE}}\right)-\right.\right.$$
$$-\Phi\left(\tfrac{m_{SE}}{\sigma_{SE}}\right)\Big]T_1+\tfrac{(T_2-t_{CE})(T_2-t_{NX})}{T_2^2}\left[1-\Phi\left(\tfrac{T_3+T_2+t_{CE}-t_2-m_{SE}}{\sigma_{SE}}\right)-\Phi\left(\tfrac{m_{SE}}{\sigma_{SE}}\right)\right]T_2+ \quad (13)$$
$$\left.+\left[1-\Phi\left(\tfrac{T_1+t_{CE}-t_3-m_{SE}}{\sigma_{SE}}\right)-\Phi\left(\tfrac{m_{SE}}{\sigma_{SE}}\right)\right]T_3\right\}\tfrac{P_{NM}S_{R_ST}}{2S_{A_ST}K_{err}(T_1+T_2+T_3+T_4)}.$$

Formulas (12) and (13) serve as mathematical stochastic models of the critical SE caused by a nuclear particle in the ST pipeline stage CP and register, respectively.

6. Critical Soft Errors in a Pipeline

The probability of a critical SE in the pipeline, generated by a single SE, depends on the probability of its occurrence in one stage and the affected stage's location in the pipeline structure. In a typical pipeline consisting of N stages, a critical SE in the k-th stage ($k = 1, \ldots, N–1$) can be masked by the subsequent stage logics. Then, the probability of the occurrence of a critical SE in the entire pipeline output when a single SE impacts one of its stages is described by the integral function:

$$F_{CF_P} = \frac{1}{N}\sum_{k=1}^{N}\left({P_{NM}}^{N-k}F_{CF,k}\right), \tag{14}$$

where $F_{CF,k}$ is the integral function of the critical SE probability in the k-th pipeline stage. Formula (14) is invariant to the synchronous and ST pipelines.

7. Discussion

Formulas (3)–(5), (7) and (10)–(14) correspond to the mathematical model definition: "A mathematical model is an approximate description of some class of phenomena, objects of the external world, expressed by means of mathematical concepts and symbols" [45]. Indeed, they describe the critical SE phenomenon in the synchronous and ST pipeline stage by means of mathematical concepts and symbols within the framework of formulated hypotheses and depending on some variables:

- Random time variables (t_S, t_i, i = 1…4, t_{DS}, t_{DR}), uniformly distributed over the corresponding intervals.
- SE durations distributed according to a truncated normal law.
- Logical cell transition delays that take a constant value at a given supply voltage and temperature.
- The duration of the clock period (in a synchronous pipeline) or an operation phase (in an ST pipeline).

These critical SE mathematical models are stochastic. They represent the probability that an SE appearing in the pipeline stage due to the impact of a nuclear particle running through the chip body becomes critical, i.e., corrupts data processing results or stops the pipeline's operation. Substituting the SEs' physical parameters and the specific values of their variables corresponding to the specified operating conditions and manufacturing technology process into these functions allows one to obtain the critical SE probability's numerical value in the pipeline stage and compare the fault tolerance levels of the synchronous and ST pipeline stages.

For the synchronous pipeline stage, such random variables are t_S and t_{DS}, which are distributed uniformly over the intervals (0, T_C) and (0, $T_{\max}$], respectively, and characterize the time and place of the SE's appearance in the pipeline stage. The remaining variables in Formulas (3)–(5) and (7) have fixed values for a specific pipeline circuit, a given synchronization frequency, supply voltage, and ambient temperature.

For the ST pipeline stage, the random variables in Formulas (10)–(13) are T_1, T_2, T_3, t_2, t_3, and t_{DR}. The first three of them depend mainly on the ST pipeline stage's complexity, supply voltage, and ambient temperature. The random variables t_2, t_3, and t_{DR} characterize the time of the SE's appearance and its place in the pipeline stage. Input data also introduce some randomness to Formulas (10)–(13), as their values affect the time of their processing in the ST pipeline stage.

For example, let us carry out a specific numerical calculation using the obtained models. To obtain quantitative estimates of the fault tolerance level of the synchronous and ST pipeline stages, we substitute typical values of the parameters used in them, which are

characteristic of the 65 nm CMOS process, into Equations (7) and (11): P_{NM} = 0.9; T_C = 1 ns; k_P = 0.8; S_{CP_S} = 0.8(S_{CP_S} + S_{CP_S}); t_{CE} = 40 ps; t_{NX} = 20 ps; t_I = 5 ps; S_{CP_ST} = 0.6S_{A_ST}; S_{R_ST} = 0.12S_{A_ST}. The normalizing coefficient K_{err} is determined by Equation (2) using the Laplace integral function for the selected parameters of the SE's duration and probability distribution function:

$$K_{err} = 1 - \left(\Phi\left(-\frac{m_{SE}}{\sigma_{SE}}\right) - \Phi(-\infty)\right) = 0.5 + \Phi\left(\frac{m_{SE}}{\sigma_{SE}}\right).$$

Figure 5 shows dependence diagrams for the probability of the occurrence of the critical SE integral functions F_{CF_S} and F_{CF_ST} on the variance in the SE duration distribution function σ_{SE} with the mathematical expectation m_{SE} = 1 ns calculated from Equations (7) and (11) for typical values of t_S = 0.5 ns, t_{DS} = 0.4 ns, $T_1 = T_3$ = 0.5 ns, T_2 = 0.3 ns, t_2 = 0.15 ns, t_3 = 0.25 ns, t_{DR} = 0.23 ns. Figure 6 shows dependence diagrams for the functions F_{CF_S} and F_{CF_ST} on the mathematical expectation m_{SE} with the variance σ_{SE} = 0.4 ns and the same typical values for the other variables in Equations (7) and (11).

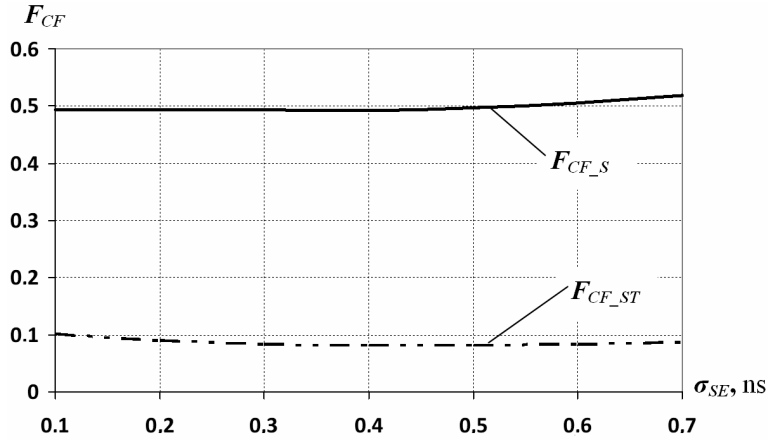


Figure 5. Critical SE probability vs. SE duration distribution function variance σ_{SE} at m_{SE} = 1 ns.

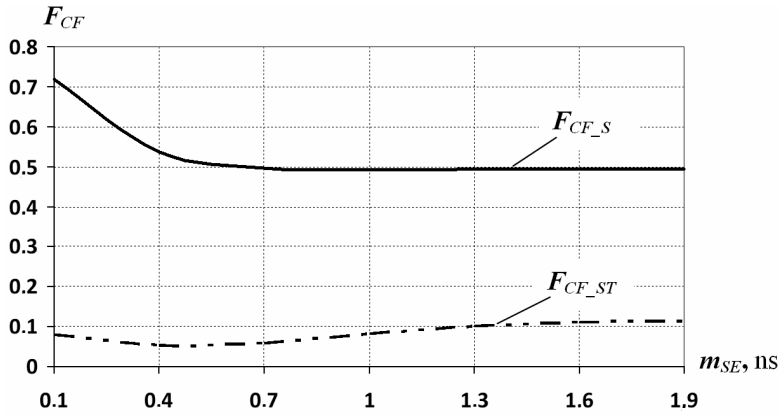


Figure 6. Critical SE probability vs. SE duration distribution function mathematical expectation m_{SE} at σ_{SE} = 0.4 ns.

Figure 5 shows that for the specific values of the mathematical expectation m_{SE} = 1 ns and variance σ_{SE} = 0.4 ns for the SE duration distribution, the probabilities of the critical SE occurrence in the synchronous (P_{CF_S}) and ST pipeline (P_{CF_ST}) stages equal P_{CF_S} = 0.493 and P_{CF_ST} = 0.081. The ratio of P_{CF_S} and P_{CF_ST} shows that an ST pipeline stage is 6.1 times better protected from an SE than the synchronous pipeline stage.

For eight-stage synchronous and ST pipelines (N = 8), where all stages are matched in hardware complexity and speed, with the above variable values, the critical SE probability

estimates according to Equation (14) are 0.350 for the synchronous pipeline and 0.057 for the ST pipeline. The advantage of the ST pipeline over the synchronous counterpart remained at the same level.

Thus, the mathematical models obtained allow one to estimate the SE tolerance level of the synchronous and ST pipelines. The resulting quantitative estimates of the critical SE probabilities in the synchronous and ST pipelines using these models support the qualitative result obtained in [30,40,41]. Further research will be devoted to the construction of a mathematical model of multiple SEs in synchronous and ST circuits.

8. Conclusions

Self-timed circuits are hardware-redundant and require proportionally more die area on the chip. Because of this, they are more susceptible to the influence of SEs compared to their synchronous counterparts. At a constant density of nuclear particle flux affecting the circuit, the intensity of an SE in an ST pipeline is also proportionally greater. However, due to the two-phase discipline and redundant data coding and dual rails in combinational circuits and pipeline registers, the ST pipeline masks SEs much better than its synchronous counterpart.

The stochastic mathematical models obtained describe the phenomenon of a single critical SE in a synchronous and ST pipeline. They allow one to evaluate and compare the stability levels of synchronous and ST pipelines to the SE source's impact in the case when the SE duration is distributed according to the normal law and the flow density of the SE sources is uniformly distributed in time and over the chip area.

Quantitative estimates of the synchronous and ST pipeline stages' SE immunity are obtained for integrated circuit components with typical operating conditions and electrical parameters. They are based on the mathematical models developed and prove the ST pipeline's advantage in terms of SE tolerance over its synchronous counterpart, being 6.1 times better.

In future studies, we intend to create stochastic models of multiple soft errors in synchronous and self-timed circuits.

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