aerospace

MDPI

Article

Radiation-Tolerant Design Strategies Using Commercial Bipolar Transistors in Power Systems for Small Satellites

Pablo Hernández [1], David Marroquí [2,*], Ausiàs Garrigós [2] and Ferdinando Tonicello [1]

[1] ESTEC, European Space Agency (ESA), 2201 AZ Noordwijk, The Netherlands; pablo.hernandez@esa.int (P.H.); ferdinando.tonicello@esa.int (F.T.)
[2] Space Power & Electronic Systems (SPES), Miguel Hernández University of Elche, 03202 Elche, Spain; augarsir@umh.es
* Correspondence: dmarroqui@umh.es

Abstract

The increase in small satellites demands the integration of commercial components to reduce costs and development time. However, the lack of standardized system-level methodologies to mitigate radiation-induced degradation limits their adoption. Although majority-carrier technologies such as MOSFET transistors dominate space power electronics, modern commercial off-the-shelf BJT transistors present a robust and cost-effective alternative. This paper evaluates the viability of the new-generation commercial off-the-shelf BJT transistors in space radiation environments by analyzing their response to total ionizing dose (measured at the circuit level) and single-event effects (inferred from component-level data). A fault-tolerant design methodology is proposed based on the strict definition of the safe operating area: the collector-emitter voltage is limited to safe values to mitigate single-event burnout, and an overdrive margin, specifically a 5× worst-case factor, is applied to compensate for the parametric degradation of the current gain. These strategies are empirically validated through two circuits: a voltage clamp and a proportional base driver operating in the 5 W to 40 W range. Experimental tests on the voltage clamp demonstrate stable operation up to one hundred kilorads, exceeding the 50 krad mission requirement by 100%. This indirectly supports the proportional base driver through shared mitigation principles, which rely on base current over-dimensioning to compensate for TID degradation. In conclusion, by applying appropriate derating rules, commercial off-the-shelf BJT transistors constitute a viable and robust alternative for small satellite power systems, mitigating the need for expensive radiation-hardened components.

Keywords: BJT; COTS; smallsats; space power systems; TID; SEE; safe operating area; radiation tolerance

Check for updates

Academic Editor: Paolo Tortora

Received: 30 March 2026
Revised: 11 May 2026
Accepted: 13 May 2026
Published: 26 May 2026

Copyright: © 2026 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license.

1. Introduction

The technological evolution of small satellites (smallsats), platforms typically defined by a mass of less than 500 kg, has consolidated cost-effective and agile access to space [1]. The conceptual development that began between the 1950s and 1970s led to the introduction of the CubeSat standard between 1999 and 2003, which democratized access to Earth orbit. Currently, smallsats represent approximately 80% of satellites launched annually [2,3], dominating critical infrastructures that include scientific payloads, telecommunication networks, and Earth observation constellations. Additionally, the sector faces a new operational frontier towards deep space. Pioneering missions, such as the NASA's MarCOs pair, and the upcoming ESA's HENON mission, demonstrate that these miniaturized

platforms can operate in severe radiation environments previously exclusive to large-mass interplanetary probes.

The development of this type of missions is strictly subject to budget and schedule constraints, which force the extensive use of commercial off-the-shelf (COTS) electronic components. Although the integration of COTS may drastically reduce costs and accelerates design iterations compared to space-qualified (Rad-Hard) components, the radiation demands of the orbital environment impose degradation mechanisms that must be addressed.

Within the scope of this work, the COTS approach focuses on discrete semiconductor components for power stages. The technical justification lies in the fact that COTS ICs exhibit vulnerability to production disruptions, undocumented silicon design revisions, and sudden end-of-life announcements. In contrast, ensuring prolonged availability, minimal lot-to-lot variation, and a lower risk of obsolescence.

Over the last four decades, in the field of space power conditioning, field-effect transistors (MOSFETs) and wide bandgap technologies (SiC and GaN) have largely displaced bipolar junction transistors (BJTs) in switching applications. While the development of space-qualified Rad-Hard BJTs has generally stagnated, with recommended devices remaining unchanged for decades [1], commercial bipolar technology has undergone drastic improvements driven by the automotive and terrestrial industries [4].

Compared to the default adoption of MOS or GaN topologies, the modern BJT presents significant operational advantages for direct use in smallsat missions. Although bipolar devices suffer the impact of Total Ionizing Dose (TID), the induced degradation in their main parameters, notably the decrease in the h_{FE} gain and the increases in base-emitter leakage currents, follows predictable and modelable deviation curves [5]. The BJT exhibits a well-understood physical behaviour [6,7]. By applying a strict derating strategy within the parametric Safe Operating Area (SOA) of these discrete devices [1], it is demonstrated that modern COTS BJTs represent a robust alternative for space power distribution systems, significantly reducing the reliance on expensive Rad-Hard components.

Despite the recognized potential of COTS components to reduce mission costs and development times, their widespread adoption in space power architectures is currently hindered by a critical lack of standardized, system-level design methodologies capable of mitigating radiation-induced degradation. Existing literature focuses on component-level characterization rather than actionable circuit-level integration strategies. The primary contribution of this manuscript is to bridge this methodological gap by proposing and validating a fault-tolerant design methodology for COTS BJT integration. This approach relies on the restriction of the operational envelope within a derated SOA to prevent Single-Event Burnout (SEB), combined with a topological safeguard consisting of a 5$\times$ worst-case base overdrive margin to compensate for TID-induced current gain degradation. By correlating component-level radiation physics with circuit-level design rules, this work provides a quantifiable and reproducible framework for deploying commercial BJT technologies. Direct TID irradiation testing was conducted on the voltage clamp circuit, whereas the radiation tolerance of the proportional base driver is analytically inferred through its application of identical mitigation strategies. Furthermore, it is important to distinguish that while TID robustness is empirically measured at the assembled circuit level, the system-level SEE tolerance is analytically inferred based on prior component-level heavy-ion evidence and the application of strict topological voltage constraints.

The remainder of this paper is structured as follows. Section 2 presents the selection criteria for discrete commercial (COTS) semiconductors for space applications, justifying the choice and validity of bipolar technology. Section 3 details the physical radiation degradation mechanisms in the space environment, specifically analysing the impact of TID and Single-Event Effects (SEE), culminating in the empirical definition of a parametric

SOA. Subsequently, Section 4 presents two practical cases of power systems (a voltage clamp stage and a proportional base driver) that implement the proposed methodological guidelines and derating rules, showing their analytical modelling and through a voltage clamp and a proportional base driver, supported by irradiation campaigns that demonstrate the effectiveness of the design rules against TID-induced degradation regardless of the specific BJT component selected. Finally, Section 5 synthesizes the general conclusions of the work.

2. Selection Criteria for Discrete Semiconductors in Space Applications

The selection of the optimal semiconductor device is a critical factor in the design of power systems for small satellites, where energy efficiency, thermal management, and operational reliability under severe radiation conditions constitute the main design constraints. Commercially available technologies, such as silicon BJTs, silicon MOSFETs, silicon carbide (SiC)-based devices, and gallium nitride field-effect transistors (GaNFETs), exhibit distinct operational characteristics in terms of conduction losses, switching speed, gate drive requirements, and intrinsic radiation tolerance. To establish a suitable selection framework for smallsat platforms, Table 1 comparatively evaluates the technological potential of these discrete COTS semiconductors applied to the space environment.

Table 1. Technology comparison of COTS discrete semiconductor devices.

	Silicon BJTs	**Silicon MOSFET**	**SiC MOSFET**	**GaN FET**
Device type	Bipolar (minority carrier)	Majority carrier	Majority carrier (wide bandgap)	Majority carrier (wide bandgap, lateral)
Conduction Loss	Low V_{CE}(sat) (≈ 0.05–0.3 V)	R_{DS}(on) dependent (increases with temp)	Very low R_{DS}(on), stable at high temp	Extremely low R_{DS}(on), minimal losses
Switching Speed	Moderate (limited by charge storage)	High (voltage-driven, low gate charge)	Very high (fast recovery, low capacitance)	Ultra-fast (lowest capacitance, no reverse recovery)
Drive Requirements	Current-driven	Voltage-driven	Voltage-driven	Voltage-driven (requires careful gate control)
Control Faults (Open/Short)	O: Safe turn-off. Sh(B-E): Safe turn-off.	O: High short-circuit risk. Sh(G-S): Safe turn-off.	O: High short-circuit risk. Sh(G-S): Safe turn-off.	O: Extreme short-circuit risk. Sh (G-S): Safe turn-off.
Primary Radiation Vulnerability	TID-induced h_{FE} degradation; SEGR immune.	SEGR, SEB, and TID-induced V_{th} shifts	High SEB susceptibility and anomalous leakage under heavy ions.	
Thermal Performance	Improved with modern packaging	Good, but limited by Si thermal properties	Excellent (high thermal conductivity)	Good, thermal management critical due to power density
Voltage Capability	Up to ~1 kV (special designs)	Up to ~1 kV (super-junction MOSFETs)	>1.2 kV typical, up to 3.3 kV+	Typically, <650 V (optimized for fast switching)
Temperature Stability	Good (stable gain vs temp)	Low (R_{DS}(on) rises with temp)	Excellent (minimal parameter drift)	Good, but sensitive to thermal runaway.
Efficiency in Power Apps	Good at low voltage, moderate power	Excellent for mid-voltage, high efficiency	Superior for high-voltage, high efficiency	Exceptional for high-frequency and low-voltage
Cost	Low (mature technology)	Low	High (evolving technology)	High (evolving technology)
Market Position	Small-signal, linear, some power apps	Dominant in power electronics	Growing in high-voltage, high-efficiency apps	Rapid growth in RF, fast chargers, HF converters

The state-of-the-art analysis derived from Table 1 reveals that the implementation of SiC MOSFETs is negligible in small satellites, given that their efficiency metrics are optimized for high-voltage systems that exceed the typical requirements of these platforms.

Conversely, silicon-based COTS devices (MOSFETs and BJTs) are widely used. While MOSFETs dominate architectures due to their fast switching and ease of control, BJTs maintain a notable technological relevance. Despite the emergence of wide bandgap technologies, the BJT provides inherent robustness, stable thermal behavior, and extensively characterized and predictable radiation failure mechanisms (TID and SEE). This predictability makes them highly reliable components for current amplification functions or linear stages in space systems. Furthermore, regarding terminal failure modes, BJT's current-driven nature offers an inherent fail-safe mechanism: an open-circuit failure at the base terminal naturally turns the device off. In contrast, MOSFETs and GaN-FETs are highly susceptible to catastrophic short-circuits if the gate terminal is left floating, as parasitic capacitances can easily induce spurious turn-on events [8].

The viability of new generations of COTS BJTs requires a technical reevaluation against traditional Rad-Hard alternatives. Historically, Rad-Hard power transistors are based on older silicon geometries, characterized by thick epitaxial layers, low internal electric fields, and guard-ring-based architectures. The radiation resilience certification of these components implicitly assumes that the power designer will apply aggressive derating on the applied voltage—frequently exceeding 50% of the nominal value—limit the operating current, and strictly avoid operating regions close to avalanche.

In contrast, modern COTS BJTs have undergone significant developments driven by the demands of the automotive and industrial sectors. These devices feature structural improvements and optimized thermal packaging (e.g., DFN/QFN) that substantially outperform their space-qualified counterparts. The new generations of discrete power BJTs provide extremely low collector-emitter saturation voltages ($V_{CE(sat)}$), typically between 0.05 V and 0.3 V, which mitigates conduction losses, and maintain a high and stable forward transfer current gain (h_{FE}) even under thermal variations and high-current regimes. As a quantifiable example of this technological leap, when comparing the historical Hi-Rel BUX77 BJT (STMicroelectronics, Geneva, Switzerland) with a modern COTS equivalent such as the 2SCR583D3 (ROHM Semiconductor, Kyoto, Japan), the commercial variant offers a thermal impedance performance that is more than twice as superior, a significant reduction in mass and volume, and a $V_{CE(sat)}$ drop that is three times lower. Additionally, the COTS device exhibits a transition frequency more than 5.6 times higher and turn-on times up to 6 times faster.

The justification for employing these COTS in space lies in the fact that, if implemented under the same strict voltage derating policies and protection assumed for Rad-Hard components, new commercial BJTs can tolerate parametric alterations and operate safely without incurring the prohibitive costs of full space qualification flows.

3. Using BJTs in the Space Environment

The implementation of COTS BJTs in the space environment requires a rigorous characterization of their vulnerability to radiation. Parametric degradation in these semiconductors is primarily caused by ionizing radiation and displacement damage in the crystal lattice [6,7]. Since the operation of BJTs depends on minority carrier transport, they exhibit greater parametric sensitivity to these phenomena compared to majority carrier technologies such as MOSFETs [6]. Ionizing radiation causes charge buildup at the device interfaces, which increases leakage currents, and reduces the current gain, especially at low operating levels [6,7]. Concurrently, displacement damage caused by high-energy particles (such as protons and neutrons) generates lattice defects that shorten the minority carrier lifetime, exacerbating the gain degradation and the increase in base current [6]. Additionally, the impact of heavy ions can trigger SEE, inducing localized transient faults or even catastrophic destruction due to burnout in power BJTs [9]. Consequently, the reliable use of

COTS components requires understanding the underlying physics of these mechanisms to implement appropriate design margins and mitigation strategies. It must be noted that while displacement damage is a known degradation factor in bipolar technologies, the empirical validation and the proposed derating rules in this work are strictly constrained to TID-dominated degradation and SEE effects. Therefore, the operational verification of the proposed COTS BJT architectures under significant high-energy proton and neutron fluences remains outside the scope of this study and constitutes a necessary phase for future characterization.

3.1. Total Ionizing Dose in Bipolar Transistors

TID quantifies the accumulated amount of energy absorbed by an electronic component due to ionizing radiation during its operational lifetime in the space environment [10]. Prolonged exposure to ionizing particles generates electron-hole pairs within the semiconductor materials and their passivation layers. The subsequent trapped charge progressively alters the intrinsic parameters of the device, degrading its performance. Expected annual dose levels, assuming a typical structural shielding of 2 to 3 mm of aluminum, vary substantially depending on the orbit, ranging from 1 to 10 krad in Low Earth Orbit (LEO) to values exceeding 50 krad in Highly Elliptical Orbits (HEO) [10]. Consequently, radiation tolerance requirements for spacecraft electronics are highly variable and strictly dependent on the specific mission profile. While short-term missions may only necessitate a tolerance of 5–10 krad, multi-year missions or those operating in deep space environments frequently encounter cumulative doses between 50 and 100 krad. Therefore, the evaluation thresholds established in this study—50 krad for the design baseline and 100 krad for survival testing—serve as general operational envelopes. These limits are defined to validate the effectiveness of BJT-based mitigation strategies across a comprehensive spectrum of potential mission scenarios, rather than targeting a singular mission requirement. Bipolar transistors exhibit acute sensitivity to this type of radiation. Charge trapping at the interfaces and in the semiconductor regions induces a direct increase in the base recombination current, which translates into a reduction in the forward transfer current gain (h_{FE}) and an increase in leakage currents [5]. Experimental lot-to-lot characterization studies demonstrate that, under TID exposure, the dominant degradation mechanisms lie in the increase in the base-emitter leakage current and the subsequent exponential drop in the h_{FE} gain [5]. These physical effects arise fundamentally from the reduction in the minority carrier lifetime in the base region, which alters the charge transport dynamics. Additionally, considerable variability is observed in the parametric tolerance to ionizing dose among different families of COTS devices. To ensure the operational reliability of COTS BJTs against ionizing radiation, the system-level approach must be based on a parametric fault-tolerant design. It is strictly necessary to apply a conservative derating on critical parameters, anticipating the loss of gain at the end of life (EOL). If the topological design is made robust against the degradation of h_{FE}, for example, by ensuring an adequate overdrive ratio between the base current (I_B) and the collector current (I_C) in switching applications, the use of commercial bipolar transistors becomes feasible, mitigating the impact of TID through the circuit architecture.

3.2. Single-Event Effects in Bipolar Transistors

SEEs originate from the interaction of a single high-energy charged particle—typically a heavy ion, a proton, or a high-energy neutron—with a sensitive region of a semiconductor device. When such a particle passes through the material, it deposits charge along its ionization track. If the magnitude of the collected charge exceeds certain critical design thresholds, it can induce transient or permanent perturbations in the nominal operation of

the device. The severity and impact of SEEs depend on multiple physical and operational factors, including the Linear Energy Transfer (LET) of the incident particle, the topological geometry of the device, the electrical bias conditions, and the operating temperature. Consequently, understanding these failure mechanisms and characterizing the sensitivity of the components under representative particle spectra constitutes an essential procedure for the design of reliable electronics in space environments.

Depending on the structure of the bipolar transistor and the nature of the radiation-induced disruption, SEEs can manifest in various typologies:

- **Soft effects (non-destructive)**: These consist of momentary disruptions of nominal operation that do not cause irreversible physical damage at the silicon level. Single-Event Upsets (SEUs), which are rarely relevant in bipolar transistors, are grouped into this category. However, Single-Event Transients (SETs) do represent a critical design factor; BJTs exhibit moderate sensitivity to SETs in analog circuits. During a SET event, charge collection in the base region of the transistor causes large-amplitude transient perturbations in the device's currents and voltages.
- **Hard effects (destructive):** These phenomena occur under conditions of high susceptibility, where the combination of intense internal electric fields and high bias voltages amplifies the charge collection generated by the impact, triggering the activation of parasitic conduction paths. The primary catastrophic failure mode associated with BJTs is Single-Event Burnout (SEB). Although it is a documented event in power bipolar transistors, it is generally less common than in homologous MOSFET technologies [11]. Susceptibility to an SEB event depends intrinsically on the architecture and structure of the device. It should be noted that complementary destructive mechanisms, such as Single-Event Gate Rupture (SEGR), are not applicable to BJT technology, given the total absence of gate oxides in their physical construction.

3.3. Definition of the BJT Safe Operating Area

Based on the previously explained physical phenomena, the definition of an SOA for BJTs in space environments requires the implementation of rigorous design margins that compensate for radiation-induced parametric degradation. The characterization of these operating limits is fundamentally based on the component's response to TID and SEE. Regarding TID mitigation, the primary documented effect is the progressive degradation of the current gain (h_{FE}). The fundamental technical conclusion to address this phenomenon lies in the topological design: if the power circuit is conceived to be inherently robust against the parametric degradation of h_{FE}, assuming the worst-case scenario expected at the EOL of the mission, the operational viability of the COTS BJT can be reliably ensured. On the other hand, the susceptibility to SEE, particularly SEB, imposes direct restrictions on the device's operational blocking voltage. In current technical literature, there are no universally applicable standardized guidelines to analytically predict whether a specific COTS BJT will respond robustly to an SEE. Nevertheless, recent experimental research conducted by our team provides decisive empirical SEE data on the latest generation of commercial power BJTs [12]. It must be emphasized that these specific heavy-ion irradiation tests were executed on the exact same discrete COTS components utilized in the application circuits proposed in this work. This study characterized seven different types of transistors (NPN and PNP) with nominal breakdown voltages ranging between 50 V and 250 V under the impact of heavy ions (Krypton and Xenon). As detailed in Table 2, the experimental results provide a reasonable indication of the safe utilization limits for BJTs in heavy ion/proton/neutron environments.

Table 2. Experimental results of SEE susceptibility in COTS power bipolar transistors. Conclusions drawn from [12].

DUT	V Rating	Type	SET Amplitude	SEB	LET [MeV/(mg/cm^2)]	Minimum Voltage at Which SEB Happened
2SCR583D3	50 V	NPN	42 A	No	N/A	N/A
2SAR583D3	50 V	PNP	400 mA	No	N/A	N/A
MJD44H11	80 V	NPN	45 A	Yes	62.5	50 V (Xe)
MJD45H11	80 V	PNP	300 mA	No	N/A	N/A
MJD31C	100 V	NPN	1 A	Yes	62.5	40 V (Xe)
ZXTN4004K	150 V	NPN	2 A	Yes	32.4	50 V (Kr)
MJD47T4	250 V	NPN	1.4 A	No	N/A	N/A

Finally, the establishment of these derating rules and the empirical definition of the SOA are intrinsically linked to the electrical conditions of the test environment. Conventional SEE characterization methodologies, governed by European verification standards such as the ESCC 25100 [13] specification, frequently employ rigorous laboratory setups that include large parallel capacitances connected directly between the collector and emitter terminals. This normative approach presents the undeniable advantage of subjecting and validating the transistor under the worst-case scenario, guaranteeing maximum safety margins against radiation. However, this excess of stored energy drastically modifies the dynamic response of the device during the particle impact, potentially inducing voltage collapses and injecting an electrical stress that is not representative of most real-world applications in small satellites.

In contrast, applying the "Test as You Fly" methodological concept allows faithfully emulating the real impedance and energy storage conditions of the final application circuit, thereby discriminating against the intrinsic silicon failures from those artificially amplified by the test bench. Nevertheless, since the *test as you fly* methodology does not certify the component for the absolute worst-case scenario, it is critical to find a technical balance and apply reasonable criteria in these types of designs. Space power engineering must reconcile the compliance and rigor of the verification standard with the operational reality of the circuit, avoiding penalizing oversizing or decreasing restrictions that derive exclusively from excessively pessimistic and unrealistic test conditions.

4. Practical Case Studies of Power Circuits Based on COTS BJTs

In this section, two practical application cases of COTS bipolar transistors in power conditioning systems for small satellites are presented. Part of the applications discussed herein were previously exhibited in [14]. Both reference designs exemplify the technical implementation of the methodological guidelines and conclusions drawn in the previous sections. The proposed architectures achieve robustness through a conservative SOA approach. TID-induced degradation of the current gain (h_{FE}) is mitigated using worst-case design margins. Furthermore, the collector-emitter voltage (V_{CE}) is strictly limited to minimize electric field stress, thereby preventing SEE. The analyzed circuits—a Voltage Clamp stage and a Proportional Base Drive (PBD)—apply the KISS design philosophy, minimizing hardware complexity and ensuring the resilience of the system against radiation without the need to integrate Rad-Hard components.

4.1. Case 1: The Voltage Clamp

4.1.1. Functional Concept and Use Cases

The Voltage Clamp circuit constitutes an active protection topology designed to operate in the linear region of bipolar transistors. An earlier iteration of this active protection topology and its preliminary validation were initially presented in [15]. Its primary function is to prevent overvoltage conditions in signal lines or low-voltage power distribution buses, dynamically diverting the excess current to the common return when the node voltage exceeds a predetermined safety threshold. By keeping the collector-emitter voltage (V_{CE}) strictly bounded, this design ensures that the BJTs operate within SOA that is intrinsically robust against SEE and electric field stress.

The applicability of this discrete hardware architecture in miniaturized space platforms (smallsats) encompasses various critical operational scenarios, among others:

- **Protection of communication interfaces:** Safeguarding sensitive logic transceivers, such as LVDS (Low-Voltage Differential Signaling) buses operating at nominal 3.3 V, ensuring their integrity against transient peaks of up to several amperes injected by upstream converter anomalies.
- **Fault propagation barriers:** Implementation of safety networks based on the "Do No Harm" methodological guideline, acting as a physical barrier that isolates subsystems and prevents a localized electrical overvoltage fault from propagating, thus preventing catastrophic system-level failures.
- **Transient conditioning:** Energy absorption during the disconnection of inductive loads or mitigation of high-amplitude overvoltage transients generated by SEE in the upstream, ensuring stability against rapid perturbations.

4.1.2. Specifications and Design Requirements

The evaluated circuit is specifically designed to limit and protect the voltage of a 3.3 V bus. The specifications require an extremely low quiescent current consumption (less than 5 mA) and a clamping voltage strictly confined between 3.5 V and 4.0 V. This threshold must remain stable under current injections ranging from 10 mA to 2 A in continuous steady state and must tolerate transient peaks of greater magnitude. Thermally, the system must guarantee its full-capacity performance over a range of -20 °C to +80 °C. In terms of radiation tolerance, the design must maintain its functionality unaltered after absorbing a TID of up to 50 krad and is required to mitigate SEE vulnerabilities for a LET of up to 34 MeV $\cdot$ cm^2/mg, relying on component-level characterizations and topological safeguards.

4.1.3. Circuit Architecture and Mitigation Strategies

The topology, shown in Figure 1, implements a band-gap voltage reference that establishes the primary control voltage, complemented by the base-emitter voltage (V_{BE}) of a transistor used as a secondary sensing element. Both elements exploit a high intrinsic stability under exposure to ionizing radiation. The derivation of the overcurrent falls upon a BJT amplification chain ($U2 \rightarrow Q1 \rightarrow Q2$), supported by low-ohmic value resistors that gradually distribute the power dissipation and the current limiting action.

To mitigate the parametric degradation induced by TID (specifically the drastic reduction in the gain h_{FE}), the amplification chain has been sized to provide a sufficient overdrive margin to maintain the clamping action even assuming a gain reduction by a factor of five in the worst-case scenario. Regarding SEEs, the clamping topological nature itself keeps the collector-emitter voltage (V_{CE}) bounded, eliminating the physical risk of SEB in the BJTs. However, since the commercial band-gap integrated circuit is susceptible to transient collapses caused by ion impacts, the architecture integrates a passive RC filter

($R3 = 150\ \Omega$, $C1 = 4.7\mu$F). This filter attenuates severe input perturbations, reducing them to voltage variations of less than 15 mV at the clamping node.

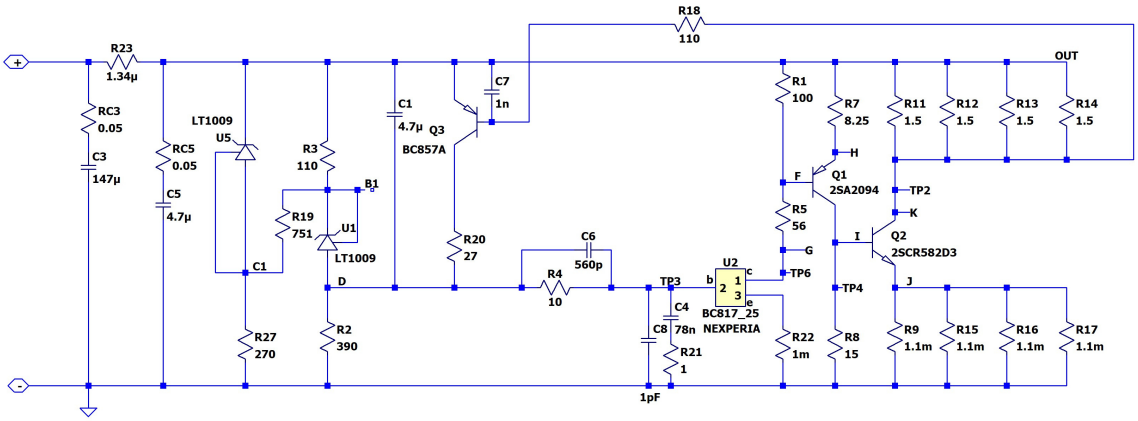


Figure 1. Schematic of the implemented Voltage Clamp.

4.1.4. Analytical Modeling and Simulations

Assuming a sufficiently high current gain, the nominal clamping voltage is governed in a simplified manner by the analytical equation $V_{clamp} \approx V_{BG} + V_{BE}$. The fundamental diode equation defines a negative temperature coefficient for V_{BE}, which reduces its magnitude as the temperature increases; this physical phenomenon is naturally incorporated into the thermal compensation of the regulation loop.

The reliability of the design was verified through Monte Carlo analysis (1108 iterations for a 95% confidence level and a 99.7% probability) in SPICE. To model the worst-case scenario under radiation, severe degradation was imposed where the h_{FE} was reduced by a factor of five in all BJTs, statistical dispersion was added to the voltage V_{BE}, and a drift ranging from -2.9% to $+7\%$ was injected into the band-gap reference. The analytical results demonstrated that the clamping voltage does not exceed the specified 4.0 V safety limit, even under 5 A transient perturbations under extreme parametric stress.

4.1.5. Experimental Validation

To corroborate the validity of the model and certify immunity against the inherent dispersion of commercial COTS manufacturing, twelve identical printed circuit boards (PCBs) were assembled and characterized using components from different lots, see Figure 2. The quantitative statistical spread of these components, including lot-to-lot variability and parametric drift under irradiation, is extensively documented in [5,15]. The evaluation of the twelve prototypes in this study is strictly focused on the functional validation of the system-level worst-case topological margins. Laboratory tests included thermal characterization ($-20\ ^\circ$C to $+80\ ^\circ$C), experimentally validating the predictable drift of V_{BE} (≈ -1.6 mV/K).

At the dynamic level, fast current steps (up to 1 A) and overload pulses (5 A) were injected to evaluate the stability of the control loop. Figure 3 presents the transient behavior of the voltage clamping circuit under a 5 A overload condition. As indicated by the green trace, the sudden input current step forces the clamping loop toward its maximum conduction capability. When the clamped current exceeds approximately 1.5 A, the circuit begins to operate like a crowbar: it deliberately forces the clamped voltage at the OUT node (blue trace) below the nominal regulated value to divert excess current and protect the pass element. This crowbar-like action is evident in the purple trace, where the collector-emitter voltage (V_{CE}) of Q2 falls as the device is intentionally driven out of its linear region. Additionally, deliberate empirical fault-injection tests were executed at the band-

gap terminals to emulate SEE-type perturbations. The RC network demonstrated its effectiveness by suppressing multi-volt transients and containing them to sub-20 mV levels. Throughout all the tests, the circuit maintained stable clamping.

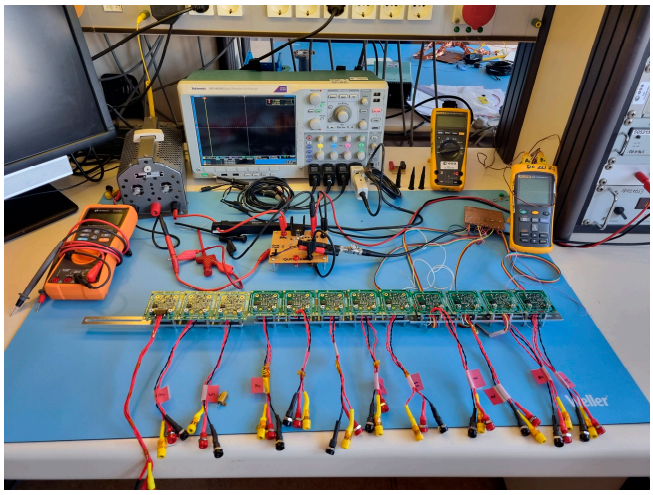


Figure 2. Prototypes implemented in a laboratory environment.

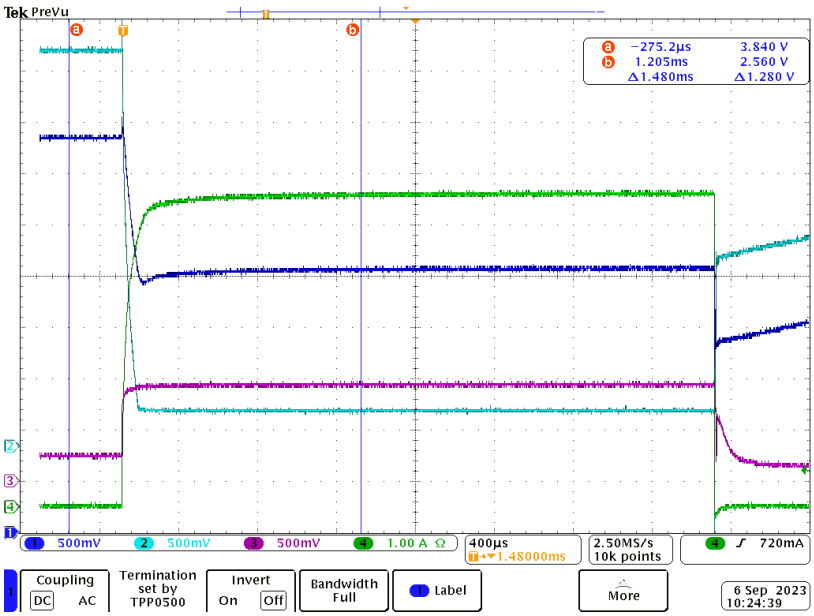


Figure 3. Transient operation of the voltage clamp against a 5 A overload. Green trace: Input current step (5 A). Blue trace: Regulated voltage at the clamping node (OUT). Purple trace: Collector-emitter voltage of the main BJT (node K on Q2, see Figure 1). Sky blue trace: Base voltage of the main BJT (node I on Q2, see Figure 1).

Following the nominal electrical characterization, the twelve prototypes were subjected to test campaigns in a representative radiation environment at the European Space Agency facilities, see Figure 4, to validate the implemented mitigation strategies. The comprehensive methodology defining the TID irradiation campaign, is extensively documented in [15]. To ensure the self-containment of this work, the primary parameters of the irradiation protocol are summarized in Table 3. The prototypes evaluated in this work were subjected to radiation stress following this exact established protocol. TID exposure tests revealed that the circuit, built entirely with COTS components without prior screening or lot control, exhibited negligible parametric degradation in its overall performance. The system successfully maintained a stable clamping voltage, operating

safely within rigorous specifications and showing no degradation under accumulated dose levels of up to 100 krad. These experimental results confirm that the topological overdesign effectively compensates for the deterioration of the current gain, validating the viability of the commercial BJT for long-duration missions.

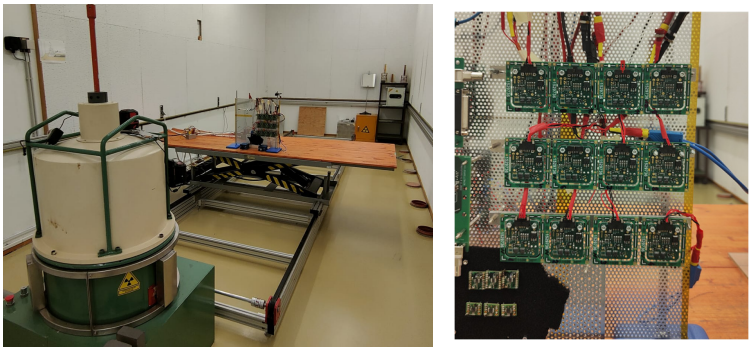


Figure 4. Prototypes implemented in the European Space Agency radiation chamber.

Table 3. Summary of the TID Irradiation Methodology from [15].

Parameter	Condition/Specification
Radiation Source	Cobalt-60 at ESA ESTEC facilities
Dose Rate	360 rad/h (Low Dose Rate window for enhanced low dose rate sensitivity testing)
Bias Conditions	Nominal operational bias (3.3 V) and Unbiased (all terminals grounded)
Checkpoints	Pre-irradiation, intermediate steps (20, 40, 60, 80 krad), 100 krad, and post-annealing
Annealing Procedure	24 h of Room Temperature Annealing followed by 168 h of accelerated aging at 100 °C
Sample Allocation	12 assembled prototypes
Pass/Fail Criteria	Stable clamping voltage (3.5 V to 4.0 V) under transient loads, quiescent current < 5 mA

4.1.6. Design Conclusions

The comprehensive evaluation of the Voltage Clamp indicates that the implementation of COTS BJT transistors in linear topologies constitutes a reliable solution for space radiation environments. Full compliance with bus protection specifications is achieved through three methodological strategies. First, the V_{CE} voltage is strictly limited to mitigate destructive SEB risks, relying on the safe operating limits analytically inferred from component-level heavy-ion data. Second, worst-case transistor gain margins are incorporated to compensate for TID degradation. Finally, passive filtering is applied to the vulnerable nodes. This approach supports the premise that those discrete commercial semiconductors, if operated within controlled SOA margins, represent a robust and economically viable alternative to the exclusive use of Rad-Hard components.

4.2. Case 2: The Proportional Base Driver

4.2.1. Functional Concept and Topological Use Cases

The proportional base driver (PBD) is a hardware biasing technique designed to ensure that, in the active region, the collector current maintains direct proportionality with the base current ($I_C = \beta I_B$) at all times. In power switching applications for DC/DC converters, this concept is typically implemented using a magnetic transformer provided with three

windings, operating in conjunction with an NPN control transistor and a power BJT. Its primary use case in the field of small satellites is the provision of a modular, *plug-and-play* switching stage, which is directly applicable to multiple DC/DC conversion architectures, such as buck, boost, or push-pull configurations.

4.2.2. Specifications and Design Requirements

While early literature explored proportional base drives for space applications [16–18], those historical designs fundamentally lacked mitigation strategies against radiation-induced parametric degradation. In contrast, this study modernizes the PBD approach to accommodate discrete COTS BJTs by inherently integrating strict overdrive margins to compensate for TID-induced gain loss and topological voltage restrictions to prevent SEE vulnerabilities.

The reference PBD circuit is specified to provide switching signals with an adjustable duty cycle between 10% and 80%, operating at nominal frequencies ranging from 100 kHz to 200 kHz. From a volumetric and integration standpoint, the design targets a highly compact footprint, consolidating the entire circuitry within a 2 cm $\times$ 2 cm PCB. To maximize efficiency in energy-constrained systems, an extremely low quiescent current consumption is required, less than 20 mA for a 10 V input supply. Full performance of the power stage must be guaranteed over an operating thermal range of -20 °C to +80 °C. From the perspective of radiation resilience, it is required to tolerate a guaranteed TID of at least 50 krad without degradation in dynamic performance. In terms of efficiency, the goal is to keep losses (combining switching and conduction) at marginal levels for medium-power applications.

4.2.3. Circuit Architecture and Mitigation Strategies

The topology, shown in Figure 5, is structured around a transformer provided with three magnetically coupled windings ($L1$, $L2$, and $L3$). The conduction cycle begins when a control pulse is injected into $L2$, forcing the main transistor $Q3$ into saturation. Once the collector current (i_C) flows, the magnetic coupling induces a proportional base current through the transformer. One of the most relevant technical characteristics of this architecture is its self-regulation: if the load on $Q3$ experiences dynamic variations, the value of i_C changes and, simultaneously, an automatic proportional adjustment is induced in the current injected into the secondary winding.

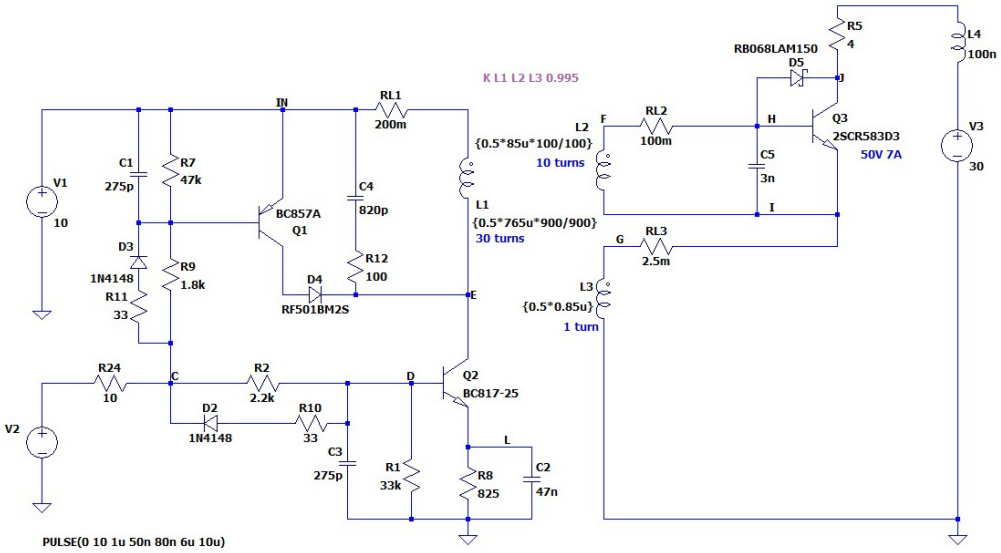


Figure 5. Schematic of the implemented PBD.

The design mitigates TID effects on the COTS components by addressing the parametric degradation of the current gain (h_{FE}). This is accomplished by establishing a transformer turns ratio ($L2/L3$) significantly lower than the minimum anticipated h_{FE} of transistor Q3.

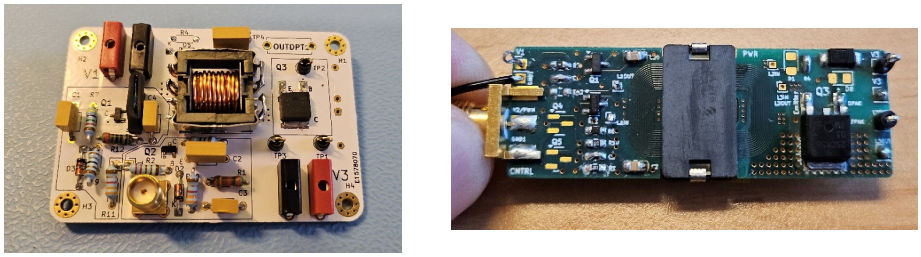
By establishing a significantly high turns ratio between the secondary windings (for example, with a factor of 10), the circuit injects the necessary base current to completely dominate the radiation-induced loss of h_{FE}. This ensures that the BJT remains in deep saturation even under the mission's end-of-life conditions. From a TID perspective, the methodology—relying on a 5× base overdrive margin—enables the use of any commercial power BJT, as the gain degradation is compensated by the base current over-dimensioning. The effectiveness of these rules was validated up to 100 krad in the Voltage Clamp architecture under linear operating conditions. Consequently, the radiation tolerance of the PBD is supported by these results, as it implements the same mitigation principles using the same COTS BJT reference for empirical consistency.

4.2.4. Analytical Modeling and Simulations

In this type of self-regulated circuits, the control of the commercial BJT's overdrive is parametrically defined by the turns ratio of the magnetic core. Mathematically, the quotient between the collector current and the required base current is equal to the quotient of the number of turns of the windings, expressed as $i_{collector}/i_{base} = N_{L3}/N_{L2}$.

4.2.5. Experimental Validation

To empirically corroborate the viability of the analytical design, several prototypes of the PBD circuit were developed. As can be observed in Figure 6, particularly in Figure 6b, this implementation achieves a remarkable level of miniaturization by integrating the COTS components described in Figure 5 and embedding planar magnetic elements directly into the printed circuit board. This compact approach not only optimizes the physical footprint for smallsat applications but also minimizes parasitic leakage inductances and enhances thermal performance.



(**a**) (**b**)

Figure 6. Two of the implemented PBD prototypes. (**a**) First version with a hand-wound transformer. (**b**) Second version with a planar transformer.

The functional characterization was initially evaluated by applying it to a buck converter topology. The test operating conditions established an input voltage $V_{IN} = 40$ V and an output voltage $V_{OUT} = 20$ V, operating with a 50% duty cycle at a frequency of 100 kHz. In this technical scenario, assuming a load current $I_{OUT} = 5$ A (equivalent to a nominal transferred power of 100 W), the power losses dissipated exclusively in the switching BJT transistor were quantified at 1.15 W. Consequently, the conversion efficiency calculation referring solely to the COTS bipolar switch stage reaches an outstanding 98.9%. The turn-on and turn-off switching times comfortably allow operation in the 200 kHz range, maintaining stable performance across varying duty cycles (30%, 50%, and 80%), as illustrated in Figure 7.

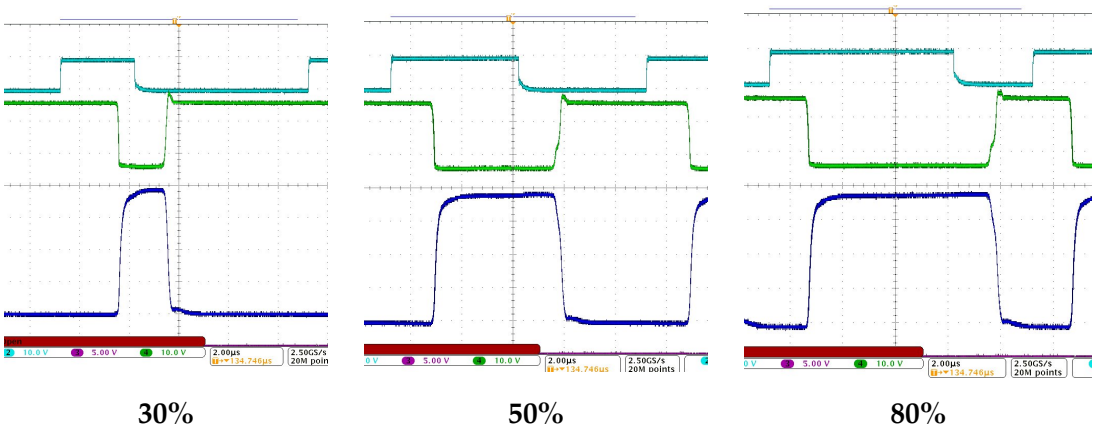


Figure 7. Operation of the PBD in a buck converter at 30%, 50%, and 80% duty cycles. Sky blue trace: Command pulse. Green trace: Collector-emitter voltage of the main BJT (Q3, see Figure 5) Dark blue trace: Collector current of the power BJT (Q3, see Figure 5). Time scale is 2 µs.

Furthermore, to assess the versatility and dynamic performance of the PBD across different switching architectures, the proposed circuit was also implemented and tested within a quasi-resonant push-pull converter [19] working as a 2:1 DCX. In this experimental scenario, the COTS BJT driven by the PBD was directly benchmarked against state-of-the-art GaN transistors to contextualize its operational performance. The experimental tests were conducted over a varying output power range, sweeping from 5 W up to 40 W. The comparative results derived from this setup are illustrated in Figure 8. Notably, this assessment demonstrates that, within this low-to-medium power regime, the BJT-based solution maintains highly competitive efficiency levels.

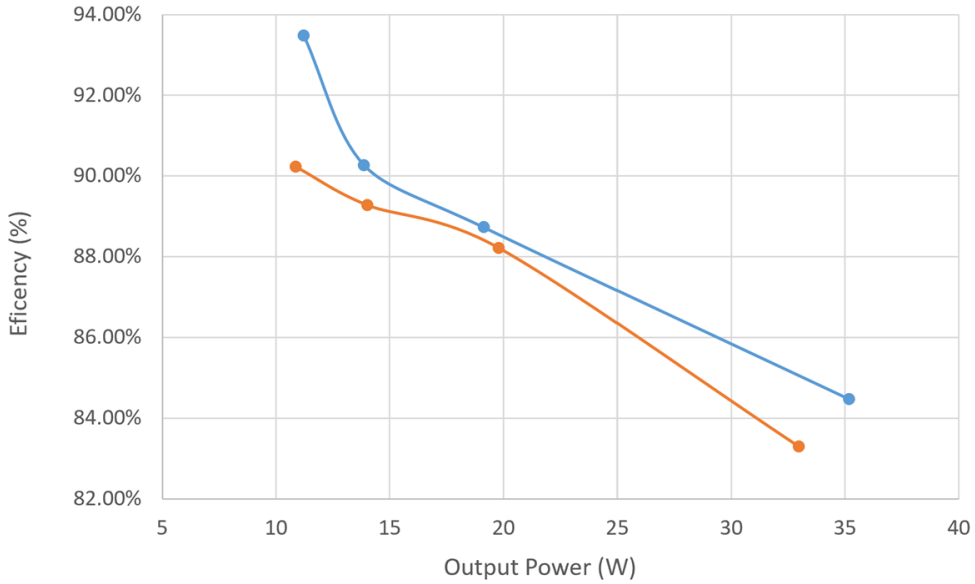


Figure 8. Efficiency comparison between the proposed PBD COTS BJT and state-of-the-art GaN transistors in a resonant push-pull converter across an output power range of 5 W to 40 W. Blue trace: push–pull converter with GaN Transistor efficiency. Orange trace: push–pull converter with PBD efficiency.

To provide further empirical support for the PBD's radiation tolerance, the functional characterization and efficiency measurements were conducted using the specific BJT transistors that had previously accumulated a TID of 100 krad during the Voltage Clamp irradiation campaigns. The fact that the PBD maintained stable switching and high

efficiency while driving these degraded transistors constitutes a strong practical evidence that the system's design is effective.

4.2.6. Design Conclusions

Within the evaluated 5 W to 40 W power range and the specific quasi-resonant push-pull topology, the experimental characterization demonstrates that COTS bipolar transistors constitute a viable switching alternative. While SiC and GaN technologies provide superior efficiency at very high frequencies, their commercial implementation in small satellites frequently requires specific SEE mitigations for the gate drivers. The proposed PBD architecture avoids these specific vulnerabilities, offering highly competitive efficiency for low-to-medium power converters operating under the defined test conditions. By resorting to a PBD approach using commercial COTS BJTs with the V_{CE} voltage strictly limited, TID mitigation is intrinsically guaranteed by the transformer ratio, while SEB mitigation is analytically inferred topologically by avoiding critical voltage thresholds. This design substantially reduces the mission risks associated with non-qualified components, supporting the rapid iterative cycle demanded by current scientific smallsat missions.

5. Conclusions

The results support the hypothesis that BJTs exhibit increased resilience to typical space radiation effects when the proposed worst-case design margins and topological safeguards are strictly followed. Although majority-carrier technologies dominate terrestrial power electronics, their commercial implementation in the space environment frequently requires specific mitigations against threshold voltage drifts or SEE vulnerabilities in the gate drive circuitry. In contrast, the physical behavior of the BJT under radiation is predictable and allows for its safe use through strict parametric derating rules and appropriate topological choices.

The theoretical and experimental investigations presented in this paper allow for drawing the following fundamental conclusions for space power design:

- **Predictable degradation due to TID:** BJTs exhibit a consistent and modelable reduction in their current gain (h_{FE}) under exposure to ionizing radiation. The implementation of a conservative oversizing in the hardware design stage—such as assuming a parametric reduction in the gain by a factor of five—ensures that circuits operate within nominal specifications under accumulated dose levels of up to 50–100 krad.
- **Control and mitigation of SEE:** The occurrence of catastrophic destructive events, such as SEB, is severely influenced by the test environment configuration, particularly using large parallel capacitances. While TID robustness was empirically measured at the assembled circuit level, it must be explicitly noted that system-level SEE tolerance has not been subjected to full assembly heavy-ion irradiation. In realistic smallsat architectures, where the collector-emitter voltage (V_{CE}) is rigidly clamped to low values and the stored energy is bounded, COTS BJTs exhibit a predictable SEE resilience inferred from direct component-level testing and topological derating. This underscores the critical need to apply the *Test as you fly* verification philosophy to avoid penalizing oversizing.
- **Validation of fault-tolerant architectures:** The evaluated topologies, specifically the Voltage Clamp stage and the proportional base driver (PBD), have proven to operate robustly under degraded parametric conditions corresponding to the worst-case scenario. Their optimal performance has been comprehensively evaluated through analytical modeling, SPICE simulations, dynamic bench measurements, and irradiation campaigns. It should be noted that the 100 krad irradiation campaigns were directly

performed on the Voltage Clamp circuit, with the PBD's radiation robustness inferred by topological analogy and shared design rules.

- **Maximum cost-risk efficiency alternative:** The use of discrete COTS BJTs, supported by a radiation-aware topological design, provides mission-level reliability comparable to traditional solutions, but at a fraction of the economic cost. Furthermore, the Keep It Simple, Stupid (KISS) philosophy associated with these components reduces integration complexity and mitigates obsolescence risks in the supply chain.
- **Strategic viability for resource-constrained enterprises:** This methodology is particularly well-suited for small and medium-sized companies lacking the financial capability to perform full radiation qualification or exhaustive component-by-component screening. This fault-tolerant approach enables significant improvements in design robustness, specifically when engineers opt for discrete component solutions rather than relying solely on commercial ICs. Furthermore, the implementation of the latest generation of BJT technologies allows for a high degree of miniaturization; while not achieving the absolute density of ICs, the resulting footprint is sufficiently compact to meet the stringent volumetric requirements of a wide range of space applications.

Ultimately, this study challenges the technical presumption that bipolar transistors are obsolete for power switching applications in space. Supported by strict control of the SOA and resilient circuit design, COTS BJTs offer a practical, robust, and technically predictable pathway to meet the stringent power demands of current small satellite constellations and future miniaturized interplanetary exploration missions.

Author Contributions: Conceptualization, P.H., D.M., A.G. and F.T.; methodology, P.H. and D.M.; validation, P.H. and D.M.; formal analysis, P.H. and D.M.; investigation, P.H. and D.M.; writing—original draft preparation, P.H. and D.M.; writing—review and editing, P.H., D.M., A.G. and F.T.; project administration, D.M.; funding acquisition, D.M. All authors have read and agreed to the published version of the manuscript.

Funding: This work has been funded by the Ministry of Science, Innovation and Universities through the "Proyectos de Gen-eración de Conocimiento" program of the 2023 call, under the project "Ultra-stable power conditioning and distri-bution unit for microsatellites (USuPCDU)" grant number [PID2023-148058OA-I00].

Data Availability Statement: The original contributions presented in this study are included in the article. Further inquiries can be directed to the corresponding author.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

BJT	Bipolar Junction Transistor
COTS	Commercial Off-The-Shelf
DC/DC	Direct Current to Direct Current
DCX	DC/DC transformer
DFN/QFN	Dual Flat No-lead/Quad Flat No-lead
DUT	Device Under Test
EOL	End-of-Life
ESA	European Space Agency
ESCC	European Space Components Coordination
GaN	Gallium Nitride
HEO	Highly Elliptical Orbits
Hi-Rel	High-Reliability
KISS	Keep It Simple, Stupid

LEO	Low Earth Orbit
LET	Linear Energy Transfer
LVDS	Low-Voltage Differential Signaling
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PBD	Proportional Base Driver
Rad-Hard	Radiation-Hardened
SEB	Single-Event Burnout
SEE	Single-Event Effects
SEGR	Single-Event Gate Rupture
SET	Single-Event Transients
SEU	Single-Event Upsets
SiC	Silicon Carbide
SOA	Safe Operating Area
TID	Total Ionizing Dose

References

1. *ECSS-Q-ST-60-15C*; Space Product Assurance Derating—EEE Components. ESA Requirements and Standards Division. European Coorporation for Space Standardization: Geneva, Switzerland, 2011.
2. Satellite Database | Union of Concerned Scientists. Available online: https://www.ucs.org/resources/satellite-database (accessed on 23 March 2026).
3. Weston, S.V. *Small Spacecraft Technology State of the Art 2024 Report*; NASA/TP—20250000142; NASA, Goddard Space Flight Center: Greenbelt, MA, USA, 2025.
4. Vogt, O. *BJT Bipolar Junction Transistor Application Handbook Design Engineer's Guide*; Nexperia: Nijmegen, The Netherlands, 2024.
5. Martín-Holgado, P.; Romero-Maestre, A.; de-Martín-Hernández, J.; Krimmel, F.; Borel, T.; Muschitiello, M.; Morilla, Y. Lot-to-Lot Variability and TID degradation of Bipolar Transistors Analyzed with ESA and PRECEDER Databases. In Proceedings of the 2023 IEEE Space Computing Conference (SCC), Pasadena, CA, USA, 18–21 July 2023; pp. 13–21. [CrossRef]
6. Messenger, G. *The Effects of Radiation on Electronic Systems*, 1st ed; Springer: Cham, Switzerland, 2014.
7. Johnston, A.H. Radiation effects in advanced microelectronics technologies. *IEEE Trans. Nucl. Sci.* **1998**, *45*, 1339–1354. [CrossRef]
8. Delepaut, C.; Siconolfi, S.; Mourra, O.; Tonicello, F. MOSFET Gate Open Failure Analysis in Power Electronics. In Proceedings of the 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 17–21 March 2013; pp. 189–196. [CrossRef]
9. Titus, J.L.; Johnson, G.H.; Schrimpf, R.D.; Galloway, K.F. Single-event burnout of power bipolar junction transistors. *IEEE Trans. Nucl. Sci.* **1991**, *38*, 1315–1322. [CrossRef]
10. Srour, J.R.; McGarrity, J.M. Radiation effects on microelectronics in space. *Proc. IEEE* **1988**, *76*, 1443–1469. [CrossRef]
11. George, J.S.; Clymer, D.A.; Turflinger, T.L.; Mason, L.W.; Stone, S.; Koga, R.; Sivertz, M. Response Variability in Commercial MOSFET SEE Qualification. *IEEE Trans. Nucl. Sci.* **2017**, *64*, 317–324. [CrossRef]
12. Faillace, F.; Gupta, V.; Borel, T.; Muschitiello, M.; Costantino, A.; Hernandez, P.; Heiskanen, P.; Tonicello, F. Single Event Effects of Power Bipolar Junction Transistors. In Proceedings of the RADiation and its Effects on Components and Systems Conference (RADECS), Antwerp, Belgium, 29 September–3 October 2025.
13. *ESCC Basic Specification No. 25100*; Single-Event Effects Test Method and Guidelines. European Space Agency (ESA): Noordwijk, The Netherlands, 2014.
14. Hernández, P.; Marroquí, D.; Garrigós, A.; Tonicello, F.; Costantino, A.; Gupta, V.; Faillace, F.; Borel, T.; Krimmel, F. COTS BJTs Uses Cases for Smallsats and Safe Operation Areas to Avoid Radiation Effects. In Proceedings of the ACCEDE_ESCCON, Sevilla, Spain, 25–27 March 2025.
15. Hernandez, P.; Mand, P.; Krimmel, F.; Tonicello, F. Do No Harm: A Novel Methodology to Protect Electrical Failure Propagation in Spacecraft by Applying Safety Barriers. In Proceedings of the 2023 13th European Space Power Conference (ESPC), Elche, Spain, 2–6 October 2023; pp. 1–14. [CrossRef]
16. Denzinger, W.; Baumel, S. Commercial Of-The Shelf DC/DC Converter. In Proceedings of the at the 9th European Space Power Conference, Saint-Raphaël, France, 6–10 June 2011; p. 40. Available online: https://ui.adsabs.harvard.edu/abs/2011ESASP.690E..40D (accessed on 24 March 2026).
17. Avant, R.L.; Michael, W.T.; Shortt, D.J.; Palma, R.E. Analysis of Magnetic Proportional Drive Circuits for Bipolar Junction Transistors. In Proceedings of the 1985 IEEE Power Electronics Specialists Conference, Toulouse, France, 24–28 June 1985; pp. 375–381. [CrossRef]

18. Avant, R.L.; Shortt, D.J.; West, G.E.; Palma, R.E. A Proportional Drive for Discontinuous Mode DC-to-DC Converters. In Proceedings of the IN^{TEL}EC '84—International Telecommunications Energy Conference, New Orleans, LA, USA, 4–7 November 1984; pp. 352–358. [CrossRef]
19. Weinberg, A.H.; Ghislanzoni, L. A new zero voltage and zero current power-switching technique. *IEEE Trans. Power Electron.* **1992**, *7*, 655–665. [CrossRef]

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.