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Modeling of a Multiconverter Power Distribution System for Space Applications Based on Standard Modules

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Abstract

The adoption of standardized modular converters is an emerging trend in space-qualified electrical power systems. This modular approach streamlines design and manufacturing processes, potentially reducing development lead times for new satellite platforms. Building on previous research that identified the four-switch buck-boost (FSBB) converter with double digital control loops as an effective solution for solar array and battery interfacing, this paper presents the small-signal analytical modeling of control loops within a modular multiconverter architecture operating in boost mode with resistive load. A model of a single- and two-module system is proposed and validated through both simulation and experimental measurements, providing a robust framework for assessing inter-module interactions and their impact on overall system stability.

Keywords: multiconverter system; bidirectional converters; dynamic modelling

1. Introduction

The satellite Power Distribution Subsystem (PDS) serves as the critical backbone for generating, storing, distributing, and managing electrical energy, ensuring the reliable operation of all onboard systems [1–3]. Historically, PDS architectures have relied on specialized converters: Solar Array Regulators (SARs) for photovoltaic energy processing and Battery Charge/Discharge Regulators (BCR/BDRs) for energy storage management. These components are typically custom-designed for specific missions, resulting in bespoke topologies, complex design cycles, and significant challenges regarding dynamic behavior and stability [4].

In response to the growing demand for spacecraft cost reduction [5], modular power converters [6–9] have emerged as a highly competitive solution. By utilizing standardized, interchangeable, and scalable power modules, this approach streamlines the development process and compresses project timelines. The core concept involves employing a unified converter module (or a standardized family of modules) to interface both the solar arrays and the battery with the main power bus. These modules can be configured in series or parallel, allowing for easy scaling of power and voltage capacity.

This work investigates this modular approach within a regulated bus voltage architecture [10], as illustrated in Figure 1. To eliminate single points of failure in the control stage, the designed modules are digitally controlled and operate without inter-module communication. Instead, the control strategy is based on DC Bus Signaling (DBS), a decentralized technique adapted from DC microgrids [11–16]. DBS enables a "plug-and-play"

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architecture where converters autonomously sense bus conditions and coordinate power flow based on the instantaneous DC bus voltage level.

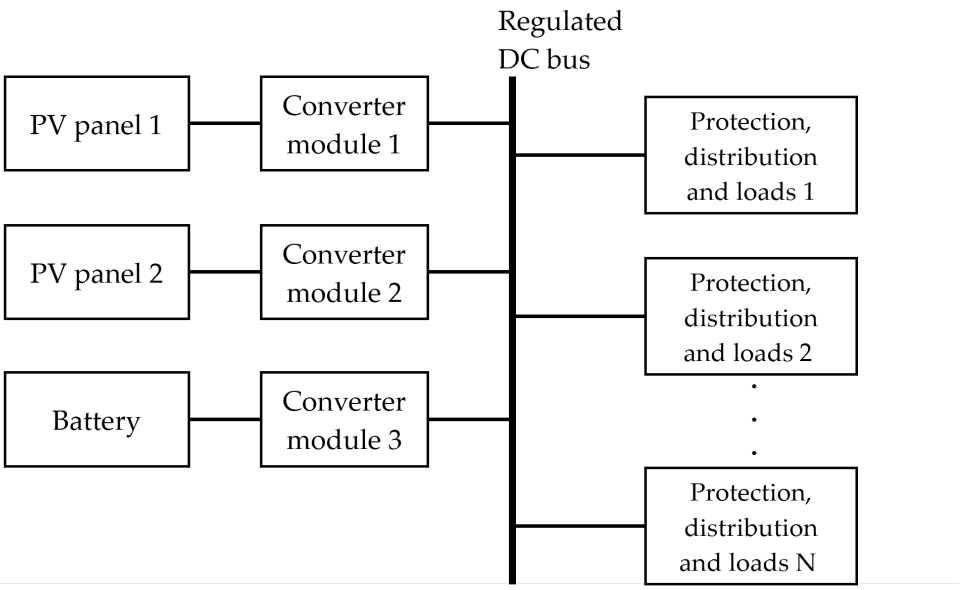


Figure 1. General overview of the architecture of the electrical power subsystem, as considered in this work.

Under this scheme, typically only one module actively regulates the bus voltage by operating within a predefined regulation range. Remaining modules either inject or withhold power depending on whether the bus voltage crosses specific internal thresholds. The regulation ranges for each module must be meticulously calibrated to maintain the energy balance throughout the orbit, specifically ensuring that:

- The battery charges whenever solar arrays provide surplus energy beyond the load requirements.
- The battery discharges seamlessly when solar arrays are inactive (e.g., during eclipse) or when load demands exceed solar generation.

Furthermore, to support robust parallel operation, each unit incorporates a droop control strategy [17–20], making the voltage reference dependent on the load current to ensure natural load sharing.

All converter modules in Figure 1 share an identical nested double-loop control structure consisting of an inner current loop and an outer voltage loop [19]. However, the collective dynamic response of multiple modules deviates from that of a single unit. This behavior is highly sensitive to the operating state—whether a module is idling, actively charging the battery, or operating at a maximum current limit without active voltage regulation.

These systems have been studied in previous works that focus on the design and description of the control strategy [19,20]; on the stability analysis of the bus voltage using criteria based on impedance ratios [19]; and on the time-domain analysis of system performance and proper power distribution during mode transitions [20]. This work complements these studies by focusing on the frequency-domain dynamic analysis of the voltage control loops in such systems.

This paper presents an analytical study of a two-module converter architecture, validated through both simulation and experimental testing. Accurately modeling these control loops is vital for predicting system-wide dynamic behavior and studying system stability across all possible operating regimes, particularly when multiple modules interact simultaneously.

2. Topology, Modulation, and Control Strategy

2.1. Topology

As previously noted, all power converter modules in Figure 1 are identical, regardless of whether they interface with a solar array or a battery. To meet this operational requirement, a 4-Switch Buck-Boost (FSBB) DC-DC topology was selected. Its inherent bidirectionality allows the module to manage both battery charging and discharging cycles [21]. The circuit schematic is shown in Figure 2, where the input V_{in} represents the solar panel or battery, and the output V_{bus} represents the regulated DC bus.

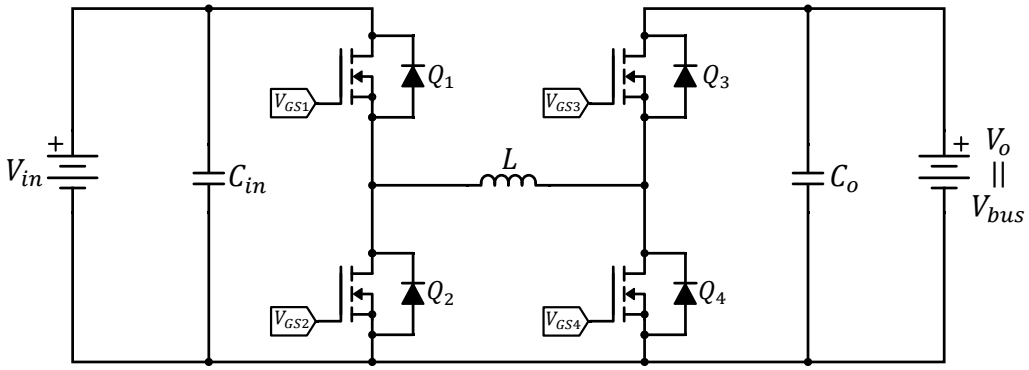


Figure 2. Schematic of the 4-Switch Buck-Boost DC-DC converter.

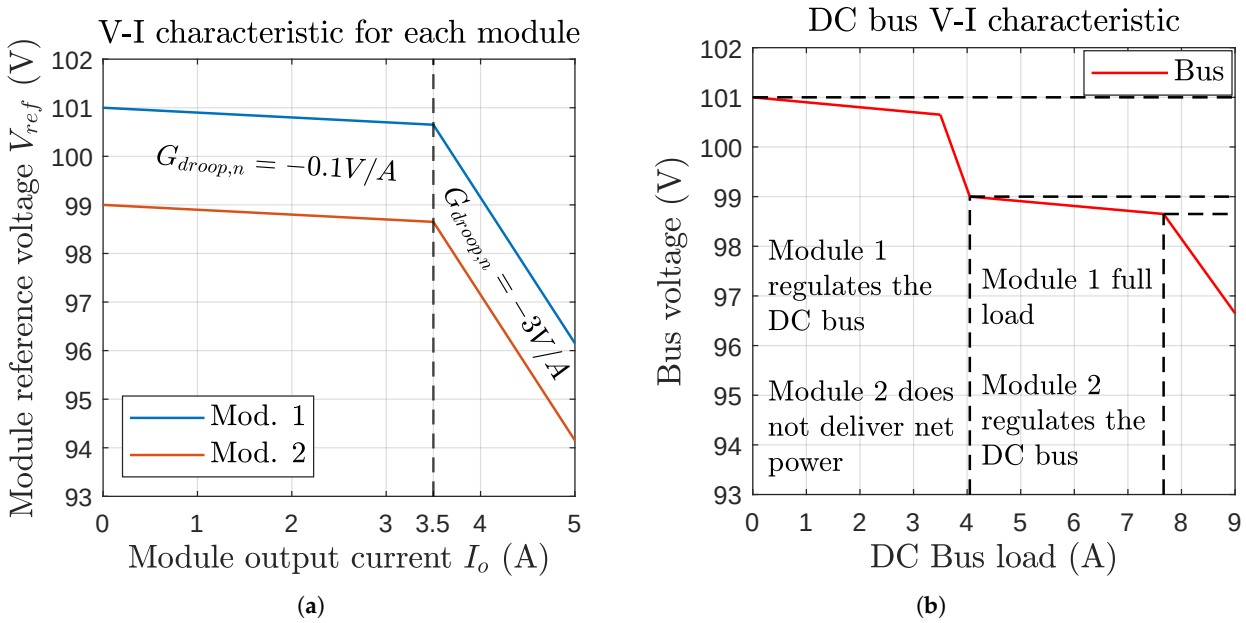
2.2. Modulation

Digital Pulse-Width Modulation (DPWM) using dual carriers is employed [20]. This technique allows the converter to operate independently in both buck and boost modes via two carrier signals, supporting a broad range of input voltages. Given the digital control implementation and the use of 10-bit ADCs, the digital signals range from -512 to 511. Consequently, the DPWM modulator is defined with a peak-to-peak carrier amplitude of $V_{pp} = 500$. The digital carrier for buck mode (input switches) ranges from -455 to 45, while the boost mode carrier (output switches) ranges from -45 to 455. Thus, the converter operates in buck mode when the digital modulating signal u is between -455 and -45, and in boost mode when it is between 45 and 455. The range between -45 and 45 represents the transition state between modes. This paper focuses specifically on the boost mode of operation.

2.3. Control Strategy

Since the power modules do not share direct control lines and the DC bus serves as the sole common connection point, a distributed control strategy based on DC Bus Signaling (DBS) is implemented. In this approach, the bus voltage level itself dictates the operating state of each module [20].

In essence, the V-I characteristic of each module (Figure 3a) comprises two regions depending on the module load current, I_o. The first region features a shallow V-I slope ($I_o < I_{elb}$), where the module actively regulates the bus voltage, referred to as "bus-mode" in [19]. The second region features a steep V-I slope ($I_o > I_{elb}$), where the module operates as a quasi-constant power source, described as "device-mode" in [19]. Each module is configured with a specific voltage offset in its V-I curve to implement the DBS strategy. Consequently, the overall V-I characteristic of the DC bus is the sequential superposition of the individual module characteristics, as depicted in Figure 3b.



(**a**) (**b**)

Figure 3. (**a**) V-I characteristic corresponding to two modules. (**b**) Aggregate V-I characteristic of the DC bus.

In this work, the droop control V-I characteristic is defined by the following slopes: $G_{droop,n} = -0.1$ V/A for bus-mode and $G_{droop,n} = -3$ V/A for device-mode, with an elbow current of $I_{elb} = 3.5$ A (the point at which the slope changes). In this case, due to the voltage sensor used and the ADC resolution (100 V/1024 = 0.1 V/bit), there are only 3 bits of resolution between 0 and 3.5 A. However, this does not affect the module's operation or dynamic performance.

Each module is governed by a nested double-loop control scheme: an outer voltage loop that senses the bus voltage and an inner current loop that regulates the inductor current. The control scheme for a module when the bus acts as a load is illustrated in Figure 4.

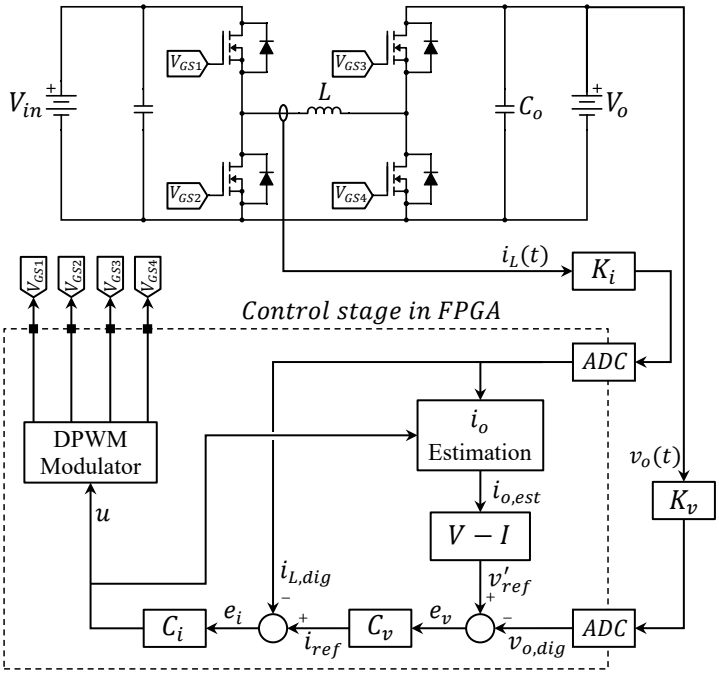


Figure 4. Detailed control scheme of a converter module.

Since the module output current is not directly measured, it is estimated using the inductor current and the duty cycle. This estimation is dependent on the specific operating mode (buck or boost) of the converter.

3. Single-Module System Model (Boost Mode)

The schematic diagram of a single-module converter operating in boost mode is shown in Figure 5.

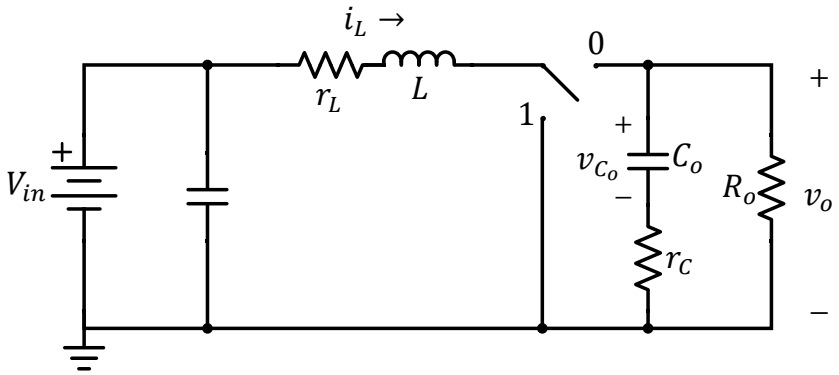


Figure 5. Schematic diagram of a module operating in boost mode.

While various load types can be interfaced with the DC bus, a resistive load is assumed in this work for simplicity. Furthermore, to focus on the control-to-output dynamics, the input voltage V_{in} is considered constant throughout the analysis.

3.1. Averaged Small-Signal State-Space Model of the Single-Module System

To derive the averaged small-signal state-space model of the single-module system, the modeling procedure described in [22] is followed. The Laplace transform of the averaged small-signal state-space equations yields the control transfer matrix $\mathbf{W}(s)$:

$$\mathbf{W}(s) = \frac{\hat{\vec{y}}(s)}{\hat{d}(s)} = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{F} + \mathbf{G} = \begin{bmatrix} \frac{\hat{i}_L}{\hat{d}} \\ \frac{\hat{v}_o}{\hat{d}} \end{bmatrix} = \begin{bmatrix} G_{id}(s) \\ G_{vd}(s) \end{bmatrix}, \tag{1}$$

which describes the influence of the control variable d on the open-loop converter outputs. The matrices $\mathbf{A}_i$, $\mathbf{B}_i$, $\mathbf{C}_i$, and $\mathbf{E}_i$, representing the state-space model for each topological state i, are provided in the Appendix A.

The state, output, and input vectors are defined as follows:

$$x(t) = \begin{bmatrix} i_L(t) \\ v_{C_o}(t) \end{bmatrix}, \quad y(t) = \begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix}, \quad v(t) = V_{in}. \tag{2}$$

3.2. Single-Module System Control Block Diagram

The control block diagram for the single-module system is illustrated in Figure 6. Despite the digital nature of the control stage, the block diagram is formulated in the Laplace domain (continuous time), initially neglecting non-linear and discrete-time effects. However, these digital effects are approximated as time delays in the Laplace domain to maintain analytical simplicity while ensuring high accuracy.

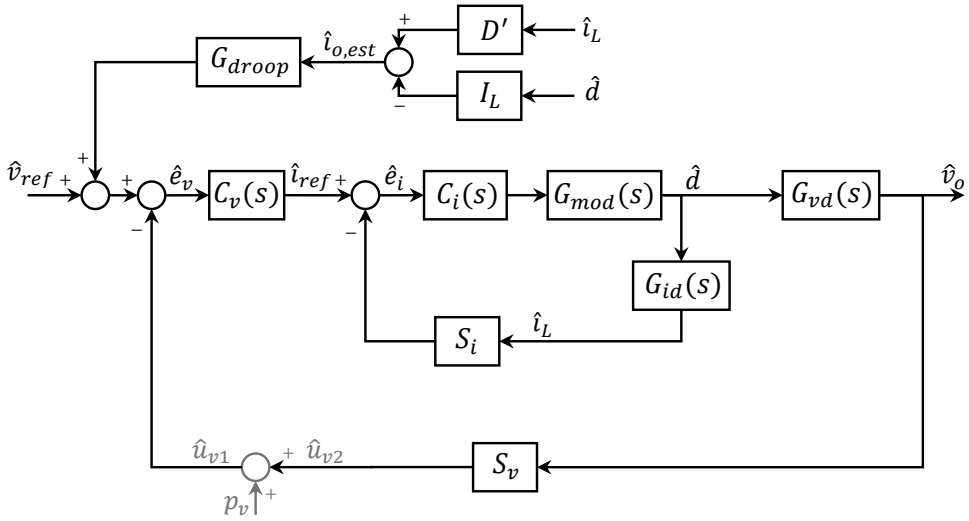


Figure 6. Control block diagram of the single-module system.

The G_{droop} block represents the V-I characteristic slope, which varies depending on whether the module operates in bus-mode or device-mode. Since the voltage reference is digital, G_{droop} relates to the natural V-I slope $G_{droop,n}$ (in V/A) as:

$$G_{droop} = S_v G_{droop,n}. \tag{3}$$

The output current estimation in boost mode is given by the small-signal expression:

$$\hat{\imath}_{o,est} = D'\hat{\imath}_L - I_L\hat{d}. \tag{4}$$

Digital control delays are modeled via the DPWM transfer function, $G_{mod}(s)$. In this implementation, sampling and control command execution coincide with the triangular carrier peaks. Therefore, triangular-carrier DPWM introduces a delay of half a switching period ($t_{DPWM} = T_{sw}/2$). The ADC conversion time causes a one-period delay ($t_{cntrl} = T_{sw}$). Thus, the total loop delay is $t_d = 1.5T_{sw}$, resulting in:

$$G_{mod}(s) = \frac{e^{-t_d s}}{V_{pp}}. \tag{5}$$

The sensors and ADCs for voltage and current are represented by S_v and S_i, with gains $K_v = 0.029$ and $K_i = 0.05$, respectively. Given a 10-bit resolution ($N = 10$) and a full-scale output $V_{FSO} = 3.3$ V, they are modeled as:

$$S_v = K_v\frac{2^N - 1}{V_{FSO}}, \quad S_i = K_i\frac{2^N - 1}{V_{FSO}}. \tag{6}$$

The voltage and current regulators, $C_v(s)$ and $C_i(s)$, are implemented as digital PI controllers but analyzed in the Laplace domain:

$$C_v(s) = \frac{K_{pv}(1 + T_{iv}s)}{T_{iv}s}, \quad C_i(s) = \frac{K_{pi}(1 + T_{ii}s)}{T_{ii}s}. \tag{7}$$

The designed parameters are $K_{pv} = 0.968$, $T_{iv} = 1.05 \cdot 10^{-4}$ s, $K_{pi} = 0.898$, and $T_{ii} = 3.90 \cdot 10^{-5}$ s. A relatively low crossover frequency was selected to guarantee stability during experimental measurements and to ensure robust operation across the entire operating range. This choice allows for a consistent validation of the control architecture without loss of generality.

3.3. Voltage Loop Gain

The voltage loop gain, $T_v(s) = \hat{u}_{v2}/\hat{u}_{v1}$, is derived to predict the bus voltage dynamics, including the effect of the droop control. By perturbing the loop as shown in Figure 6, the linearized system equations are:

$$\begin{cases} \hat{u}_{v2} = S_v \hat{v}_o \\ \hat{e}_v = G_{droop}\hat{i}_{o,est} - \hat{u}_{v1} \\ \hat{e}_i = C_v \hat{e}_v - S_i \hat{i}_L \\ \hat{d} = C_i G_{mod} \hat{e}_i \\ \hat{v}_o = G_{vd}\hat{d} \\ \hat{i}_L = G_{id}\hat{d} \\ \hat{i}_{o,est} = D'\hat{i}_L - I_L\hat{d} \end{cases} \tag{8}$$

Solving this system, the voltage loop gain for the single-module system is:

$$T_v(s) = \frac{-C_i C_v G_{mod} G_{vd} S_v}{1 + C_i G_{mod}\left(C_v G_{droop}(I_L - D'G_{id}) + G_{id}S_i\right)}. \tag{9}$$

Note that the negative sign associated with the feedback has been explicitly included in the loop gain definition. This convention is used throughout the paper; therefore, the phase margin must be evaluated with respect to 0° in all presented Bode diagrams, rather than -180° as in the conventional formulation.

4. Two-Module System Model (Boost Mode)

The schematic diagram of the two-module system, with both converters operating in boost mode and connected in parallel to a common DC bus, is shown in Figure 7.

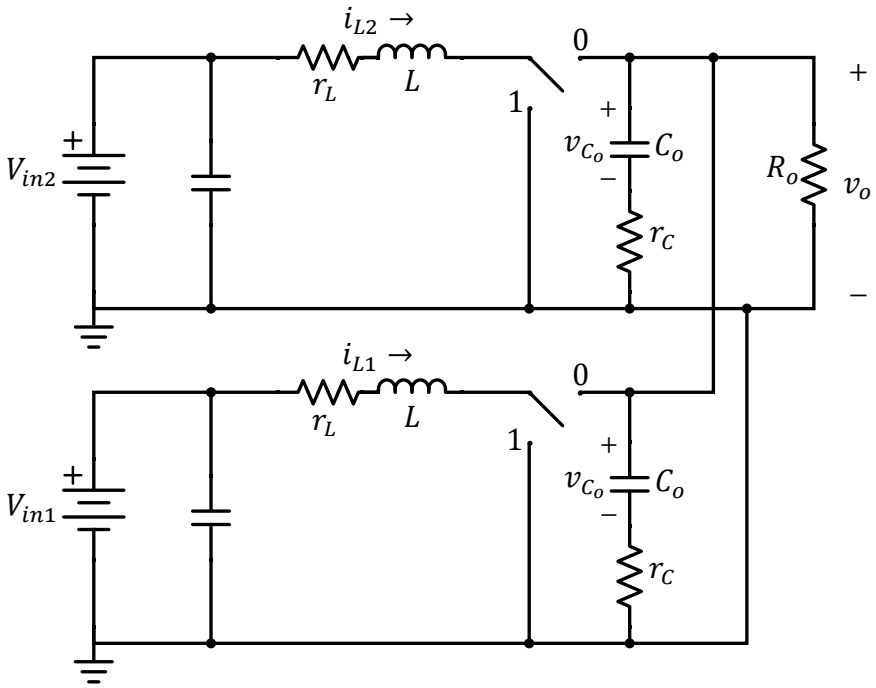


Figure 7. Schematic diagram of two modular boost converters in parallel.

In this configuration, the bus load is modeled as resistive. Since the output capacitors are connected in parallel, they are treated as a single lumped capacitance, ensuring the output voltage across both modules is identical.

4.1. Averaged Small-Signal State-Space Model of the Two-Module System

The state-space modeling for the two-module system follows a similar methodology to the single-module case. However, the parallel connection introduces up to four global topological states $ij = \{00, 01, 10, 11\}$ within each switching period, where $i, j \in \{0, 1\}$ represent the switching state of module 1 and module 2, respectively.

The duration of each state depends on the operating point, the modulation scheme, and the synchronization of the PWM carriers. In this work, triangular carrier signals are employed for both modules, and an arbitrary phase shift may exist between them because there is no communication among modules. Figure 8 illustrates the switching signals during one period for different possible cases.

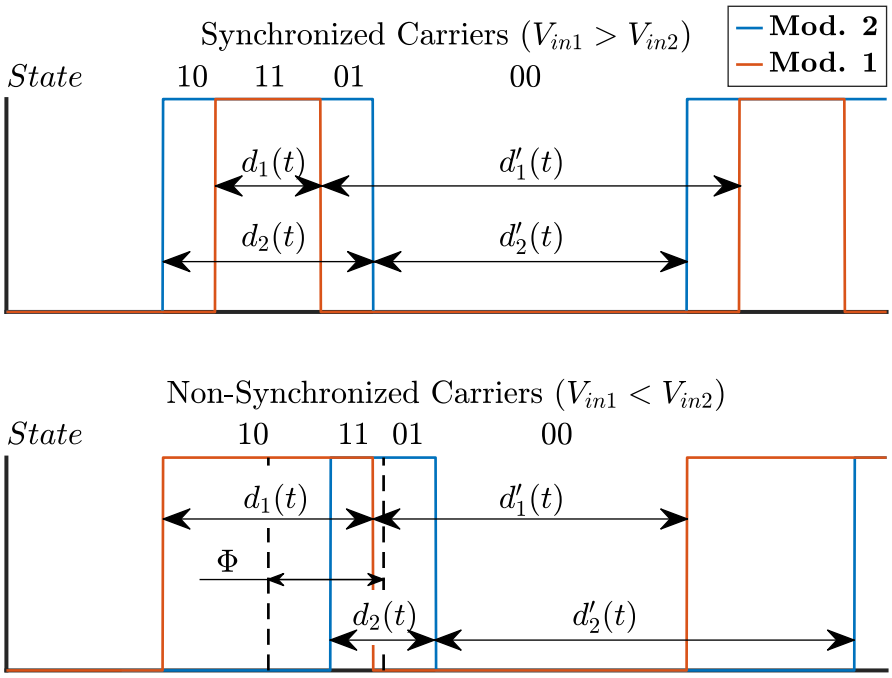


Figure 8. PWM trigger signals and resulting topological states under different carrier phase shifts and input voltages. Dashed lines indicate the center of the PWM trigger signals (carrier peaks).

For any operating point and phase shift, the state-space representation for each topological state ij is defined as:

$$\begin{aligned} \frac{dx(t)}{dt} &= \mathbf{A}_{ij}x(t) + \mathbf{B}_{ij}\mathbf{V}, \\ y(t) &= \mathbf{C}_{ij}x(t) + \mathbf{E}_{ij}\mathbf{V}, \end{aligned} \tag{10}$$

where the state, output, and input vectors are:

$$x(t) = \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C_o}(t) \end{bmatrix}, \quad y(t) = \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_o(t) \end{bmatrix}, \quad \mathbf{V} = \begin{bmatrix} V_{in1} \\ V_{in2} \end{bmatrix}. \tag{11}$$

The small-signal averaged model is obtained by linearizing the system around the steady-state operating point $\mathbf{X} = [I_{L1}, I_{L2}, V_o]^T$, accounting for the weighted transitions through the active topological states in each case. The resulting linearized system is:

$$\begin{aligned} \frac{d\hat{x}(t)}{dt} &= \mathbf{A}\hat{x}(t) + \mathbf{F}\hat{d}_1(t) + \mathbf{H}\hat{d}_2(t), \\ \hat{y}(t) &= \mathbf{C}\hat{x}(t) + \mathbf{G}\hat{d}_1(t) + \mathbf{J}\hat{d}_2(t). \end{aligned} \tag{12}$$

The matrices **A** and **F** for the case with synchronized carriers and $V_{in1} > V_{in2}$ shown in Figure 8 are:

$$\begin{aligned} \mathbf{A} &= D_1\mathbf{A}_{11} + D_2'\mathbf{A}_{00} + (D_2 - D_1)\mathbf{A}_{01}, \\ \mathbf{F} &= (\mathbf{A}_{11} - \mathbf{A}_{01})\mathbf{X} + (\mathbf{B}_{11} - \mathbf{B}_{01})\mathbf{V}, \end{aligned} \tag{13}$$

and for the case with non-synchronized carriers and $V_{in1} < V_{in2}$ are:

$$\begin{aligned} \mathbf{A} &= (\frac{1}{2}(D_1 - D_2) + \Phi)\mathbf{A}_{10} + (\frac{1}{2}(D_1 + D_2) - \Phi)\mathbf{A}_{11} \\ &\quad + (\frac{1}{2}(D_2 - D_1) + \Phi)\mathbf{A}_{01} + (1 - \frac{1}{2}(D_1 + D_2) - \Phi)\mathbf{A}_{00} \\ &= \Phi(\mathbf{A}_{10} - \mathbf{A}_{11} + \mathbf{A}_{01} - \mathbf{A}_{00}) + \frac{1}{2}[(D_1 + D_2)(\mathbf{A}_{11} - \mathbf{A}_{00}) + (D_1 - D_2)(\mathbf{A}_{10} - \mathbf{A}_{01})] + \mathbf{A}_{00}, \\ \mathbf{F} &= \frac{1}{2}(\mathbf{A}_{10} - \mathbf{A}_{00} + \mathbf{A}_{11} - \mathbf{A}_{01})\mathbf{X} + \frac{1}{2}(\mathbf{B}_{10} - \mathbf{B}_{00} + \mathbf{B}_{11} - \mathbf{B}_{01})\mathbf{V}. \end{aligned} \tag{14}$$

By manipulating these equations, it can be shown that the analytical solution is identical in both cases, as the following condition holds: $\mathbf{A}_{11} + \mathbf{A}_{00} = \mathbf{A}_{10} + \mathbf{A}_{01}$ (and similarly for $\mathbf{B}_{ij}$, $\mathbf{C}_{ij}$, and $\mathbf{E}_{ij}$). The same condition is obtained for the remaining matrices **H**, **C**, **G** and **J** in Equation (12). Therefore, the solution for any phase shift and any operating point is the same, which is a reasonable result due to the topological symmetry and the averaging of the dynamics over a switching period. The general solution can be derived from the solution for the case with synchronized carriers with $V_{in1} > V_{in2}$ as:

$$\begin{aligned} \mathbf{A} &= D_1\mathbf{A}_{11} + D_2'\mathbf{A}_{00} + (D_2 - D_1)\mathbf{A}_{01}, \\ \mathbf{C} &= D_1\mathbf{C}_{11} + D_2'\mathbf{C}_{00} + (D_2 - D_1)\mathbf{C}_{01}, \\ \mathbf{F} &= (\mathbf{A}_{11} - \mathbf{A}_{01})\mathbf{X} + (\mathbf{B}_{11} - \mathbf{B}_{01})\mathbf{V}, \\ \mathbf{G} &= (\mathbf{C}_{11} - \mathbf{C}_{01})\mathbf{X} + (\mathbf{E}_{11} - \mathbf{E}_{01})\mathbf{V}, \\ \mathbf{H} &= (\mathbf{A}_{01} - \mathbf{A}_{00})\mathbf{X} + (\mathbf{B}_{01} - \mathbf{B}_{00})\mathbf{V}, \\ \mathbf{J} &= (\mathbf{C}_{01} - \mathbf{C}_{00})\mathbf{X} + (\mathbf{E}_{01} - \mathbf{E}_{00})\mathbf{V}. \end{aligned} \tag{15}$$

Applying the Laplace transform, we derive the open-loop control-to-output transfer matrices for each control variable:

$$\mathbf{W}_1(s) = \frac{\hat{\tilde{y}}(s)}{\hat{d}_1(s)} = \begin{bmatrix} G_{id11}(s) \\ G_{id21}(s) \\ G_{vd1}(s) \end{bmatrix}, \quad \mathbf{W}_2(s) = \frac{\hat{\tilde{y}}(s)}{\hat{d}_2(s)} = \begin{bmatrix} G_{id12}(s) \\ G_{id22}(s) \\ G_{vd2}(s) \end{bmatrix}. \tag{16}$$

4.2. Two-Module System Control Block Diagram

The parallel connection introduces dynamic cross-coupling, as the duty cycle of one module (d_1) affects the state variables of the other (i_{L2}) and vice versa. This interaction is captured in the expanded control block diagram shown in Figure 9.

Based on the DC Bus Signaling strategy, two primary operating scenarios are analyzed:

(**a**) **Module 1** regulates the DC bus (bus-mode), while **Module 2** remains idle (zero power).
(**b**) **Module 2** regulates the DC bus (bus-mode), while **Module 1** operates as a constant power source (device-mode).

In scenario **a**, Module 2 does not supply power because its current reference is clamped to zero by the digital regulator's lower limit ($e_{v2} < 0 \implies i_{ref2} = 0$).

4.3. Voltage Loop Gain Analysis

Stability analysis focuses on the module actively regulating the bus in each scenario. When a module is in device-mode (saturated) or idle (passive), its relative influence on the transient bus voltage regulation is diminished.

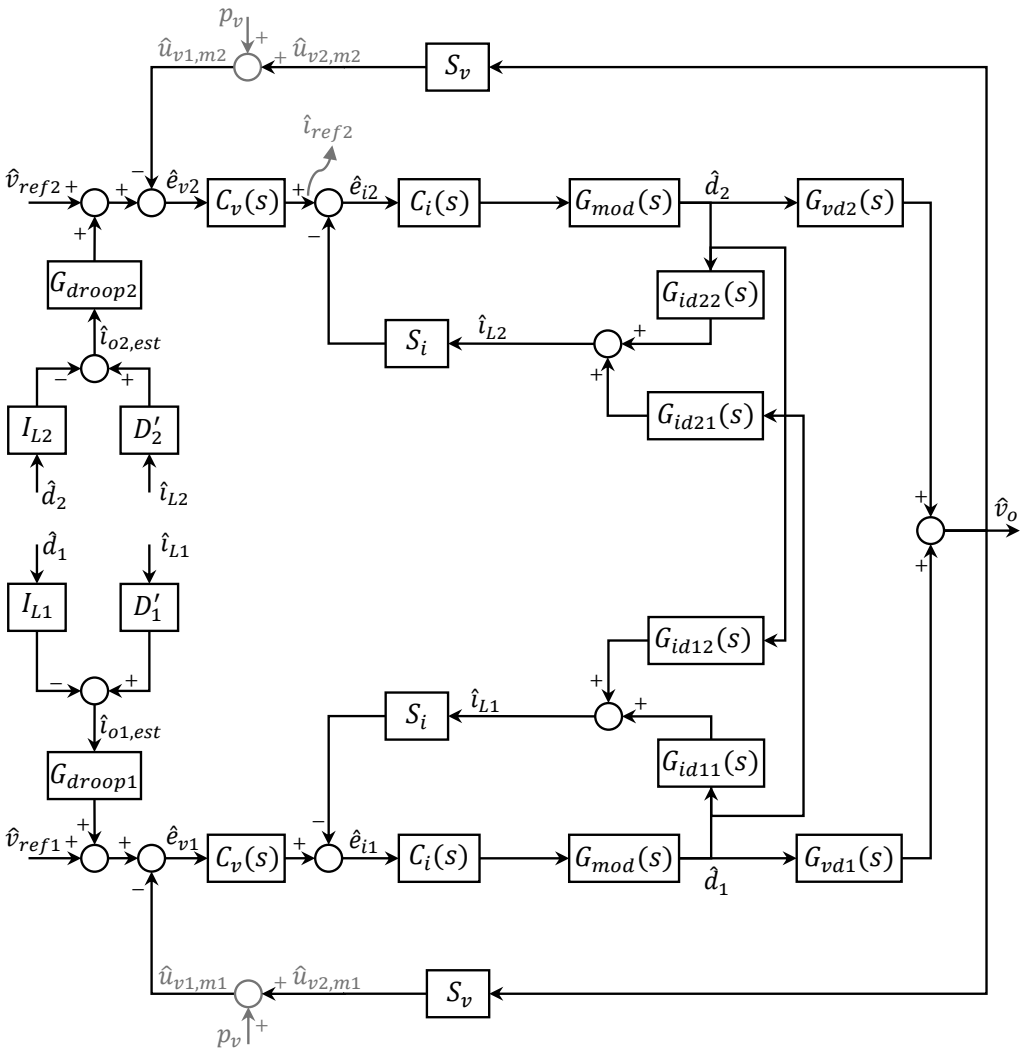


Figure 9. Control block diagram of the two-module system showing dynamic coupling.

For scenario **a**, the voltage loop gain $T_{v1(a)}(s)$ is obtained by perturbing the voltage loop of Module 1 while setting $\hat{i}_{ref2} = 0$:

$$T_{v1(a)}(s) = \left.\frac{\hat{u}_{v2,m1}}{\hat{u}_{v1,m1}}\right|_{\hat{i}_{ref2}=0}. \tag{17}$$

For scenario **b**, where Module 2 regulates the bus and Module 1 is in device-mode (steep V-I slope), the loop gain is:

$$T_{v2(b)}(s) = \frac{\hat{u}_{v2,m2}}{\hat{u}_{v1,m2}}. \tag{18}$$

Detailed matrix expressions for these loop gains are provided in the Appendix A.

5. Experimental Validation

This section validates the analytical models introduced in Sections 3 and 4 across various operating points in boost mode. The voltage loop gain for both single- and dual-module configurations was evaluated using three methods: analytical modeling, PSIM simulations (employing the ACSweep tool for frequency-domain analysis), and experimental measurements using a frequency response analyzer (FRA) on a laboratory prototype.

In all cases, the DC bus load was modeled as resistive. For the simulations, sample-and-hold blocks were incorporated to emulate digital sampling effects while avoiding ADC quantization noise to isolate the averaged dynamics. The fixed hardware parameters, corresponding to the laboratory prototype, are summarized in Table 1.

Table 1. Hardware Parameters of the Converter Module.

f_{sw}	L	r_L	C_o	r_C	V_o
200 kHz	84 µH	100 mΩ	180 µF	100 mΩ	100 V

The inductor used in the module was custom fabricated, and standard-grade electrolytic capacitors were employed. This choice reflects a practical implementation and allows the evaluation of the system under realistic, non-ideal conditions. Their value and the value of their parasitic resistances were measured using the FRA. These values were assumed to be the same for both modules in the model and the simulation, whereas this may not be the case in the laboratory prototype due to tolerances. However, this small mismatch between modules would only lead to minor differences in the open-loop dynamics, which become negligible once the loop is closed.

5.1. Single-Module System Validation

The single-module model was validated at the two operating points (OPs) defined in Table 2.

Table 2. Operating Points for Single-Module Validation.

Op. Point	V_{in}	I_o	I_L	D'	R_o
OP1	80 V	1 A	1.25 A	0.8	100 Ω
OP2	80 V	2 A	2.5 A	0.8	50 Ω

The resulting frequency responses are shown in Figure 10.

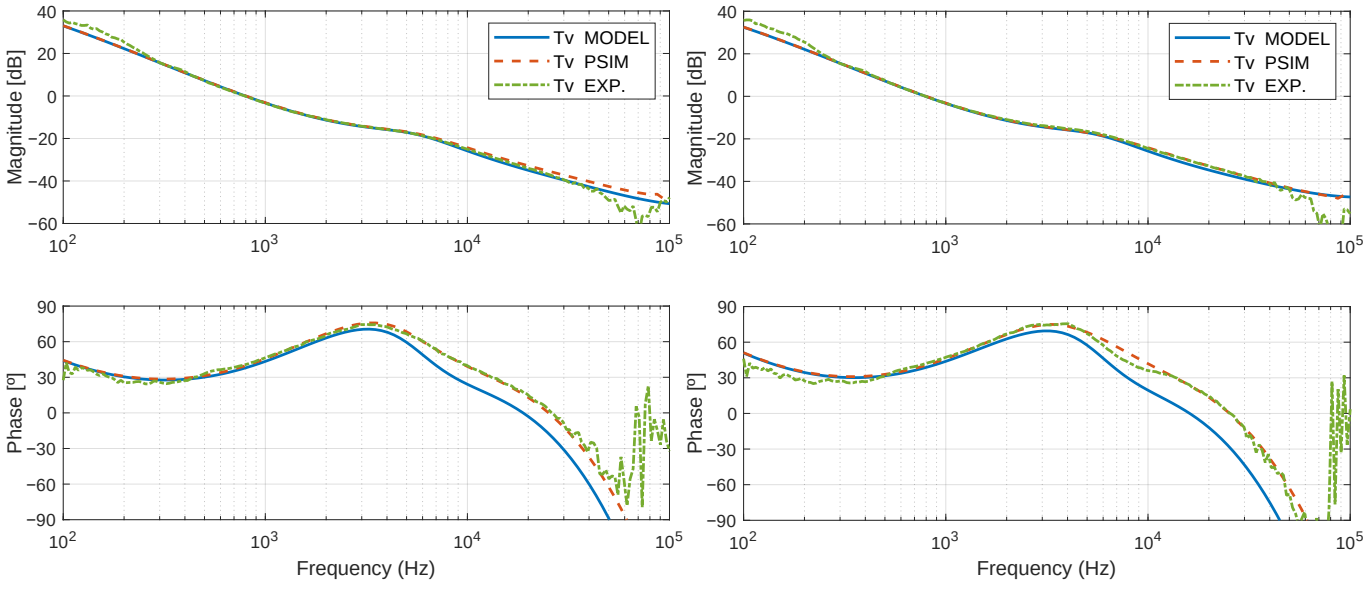


Figure 10. (**a**) Voltage loop gain for OP1. (**b**) Voltage loop gain for OP2.

For both operating points, a high degree of correlation is observed across a wide bandwidth. The simulation results closely match the experimental data over the entire

analyzed spectrum. The analytical model also demonstrates strong agreement, although the phase accuracy slightly diverges at frequencies above approximately 5 kHz. Crucially, the model remains highly accurate near the crossover frequency, confirming its utility for compensator design and stability assessment.

The observed discrepancy at high frequencies is primarily due to the continuous-time averaged modeling approach, which inherently simplifies the high-frequency dynamics introduced by the digital control and the switching ripple. As shown in Figure 11, the Equivalent Series Resistance (ESR) of the output capacitor significantly impacts this accuracy. Lower ESR values improve the model's fidelity, as high ESR values enhance the output voltage ripple, challenging the small-ripple approximation fundamental to state-space averaging [22].

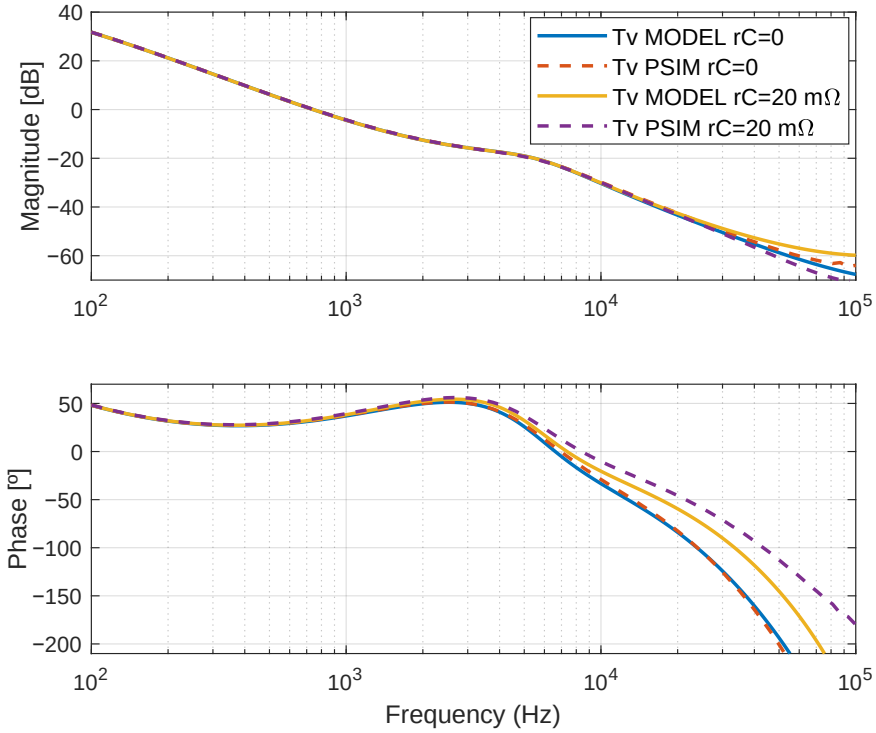


Figure 11. Model vs. simulation comparison for varying ESR values of the output capacitor.

5.2. Two-Module System Validation

The two-module system was validated under operating scenarios **a** and **b**, as detailed in Table 3.

The control strategy ensures a staggered power distribution between modules. Consequently, large disturbances might trigger non-linear behaviors (e.g., the V-I curve "elbow" or current saturation limits).

Table 3. Operating Points for Two-Module Validation.

Op. Point	V_{in1}	V_{in2}	I_{o1}	I_{o2}	D_1'	D_2'	R_o
$OP1_{(a)}$	80 V	80 V	2 A	0 A	0.8	0.8	50 Ω
$OP2_{(b)}$	80 V	80 V	4.2 A	2 A	0.8	0.8	16 Ω
$OP3_{(a)}$	70 V	80 V	2 A	0 A	0.7	0.8	50 Ω
$OP4_{(b)}$	80 V	70 V	4.2 A	2 A	0.8	0.7	16 Ω

In practice, these effects are mitigated by striking a balance between the disturbance amplitude required for frequency analysis and the design of the V-I characteristic. When a disturbance is introduced, a sufficiently large offset between the V-I curves ensures that idle

modules do not reach the lower limit of the voltage regulator (i.e., maintaining $i_{ref} = 0$), while a moderately pronounced elbow ensures that the modules in device-mode do not reach this region. In this case, the offset between curves is 2 V, the slope in device-mode is -3 V/A, and the maximum disturbance amplitude used for the measurements is 0.7% (20 mV applied to the output of the bus voltage sensor).

The loop gain results for $OP1_{(a)}$, $OP2_{(b)}$, $OP3_{(a)}$ and $OP4_{(b)}$ are presented in Figure 12.

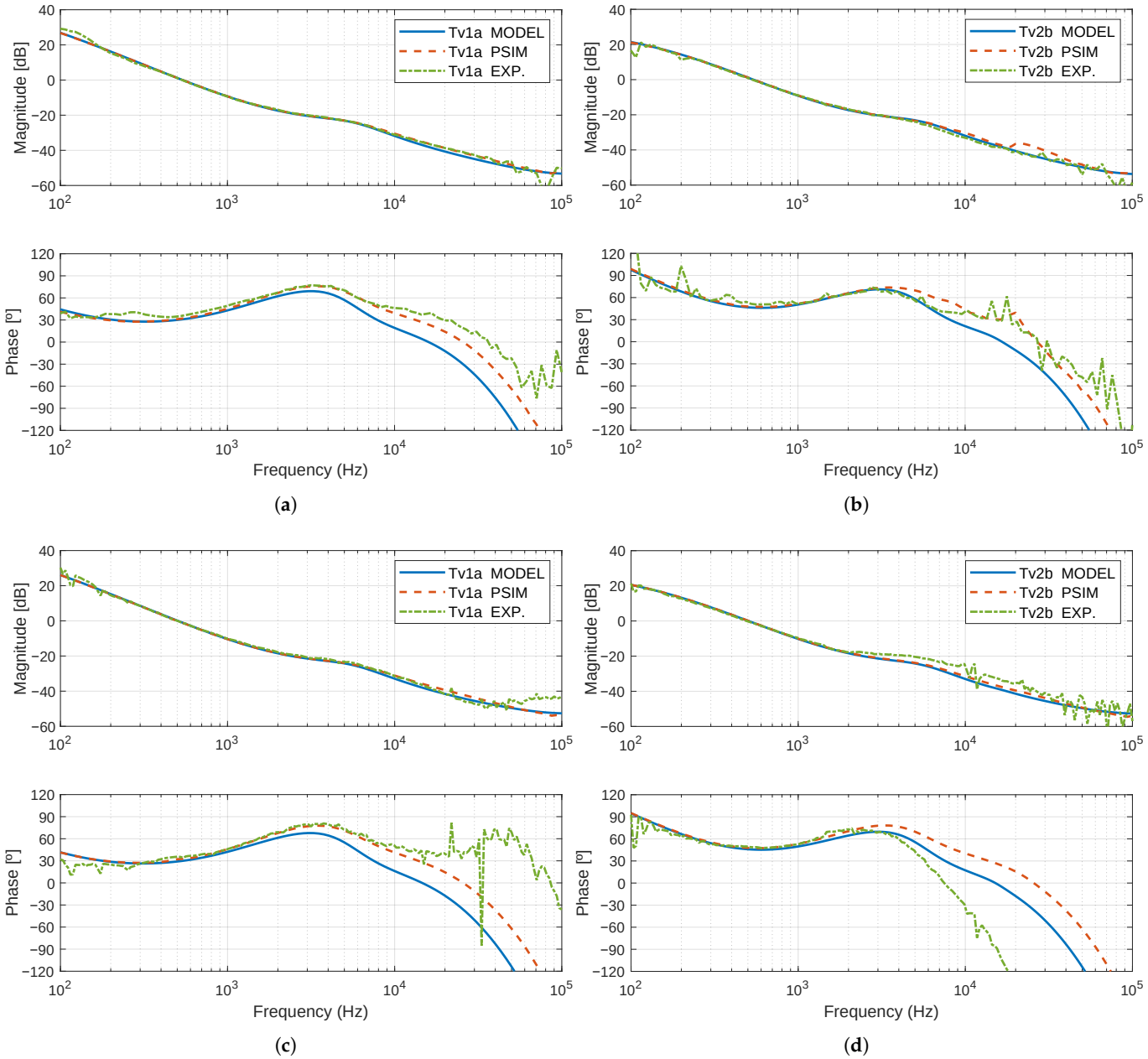


Figure 12. (**a**) Voltage loop gain for $OP1_{(a)}$. (**b**) Voltage loop gain for $OP2_{(b)}$. (**c**) Voltage loop gain for $OP3_{(a)}$. (**d**) Voltage loop gain for $OP4_{(b)}$.

Consistent with the single-module results, the analytical model aligns well with simulations but exhibits phase divergence above 5 kHz, primarily due to the limitations of averaged modeling in high-ESR scenarios. While the gain of the model and simulation matches the experimental data, the experimental phase is subject to minor ADC quantization effects not captured in simulation. Also, Figure 12d for $OP4_{(b)}$ shows that the phase of the experimental measurement at high frequency drops significantly, suggesting a variation

in the digital delay in the laboratory prototype at this operating point. Despite all this, the model's accuracy around the crossover frequency remains robust, validating its use for predicting the stability of the multi-module PDS.

Table 4 summarizes the crossover frequency and phase margin for the model, simulation, and experimental measurements across all validated operating points.

Table 4. Validation results.

Op. Point	Crossover Freq. [Hz]			Phase Margin [°]		
	MODEL	**PSIM**	**EXP.**	**MODEL**	**PSIM**	**EXP.**
OP1	796.20	802.60	790.81	37.88	39.89	40.52
OP2	794.15	800.45	793.93	38.62	40.65	41.92
$OP1_{(a)}$	539.28	540.22	536.48	30.95	32.08	35.77
$OP2_{(b)}$	540.97	542.72	531.95	46.29	47.59	51.28
$OP3_{(a)}$	504.86	498.45	501.34	29.18	32.13	35.61
$OP4_{(b)}$	504.55	507.02	490.88	45.86	47.74	49.69

It should be noted that large-signal dynamics associated with threshold-crossing transitions between operating and conversion modes are beyond the scope of this work and have been addressed in prior studies [20].

6. Impact of Modular Configuration on Voltage Loop Gain

This section analyzes how the modular architecture and the associated control strategies influence the system's dynamic performance. Specifically, it examines the effects of parallel module integration and the implementation of droop control on the voltage loop gain.

6.1. Impact of Module Connection on Voltage Loop Gain

The voltage loop response of a single-module system is compared with that of a two-module system operating in scenarios **a** and **b** under equivalent power and load conditions. The cases analyzed are summarized in Table 5.

Table 5. Comparison Cases for Single- and Multi-Module Configurations.

Single Module	Case	Two-Module System
Module supplies $I_o = 2$ A (bus-mode); [OP2].	Case 1 $\Longleftrightarrow$	Module 1 supplies $I_{o1} = 2$ A (bus-mode); Module 2 is idle (zero power); $[OP1_{(a)}]$.
	Case 2 $\Longleftrightarrow$	Module 1 operates in device-mode (constant power); Module 2 supplies $I_{o2} = 2$ A (bus-mode); $[OP2_{(b)}]$.

The impact on the loop dynamics of the bus-regulating module is illustrated in Figure 13. Case 1 highlights the effect of paralleling an idle module, while Case 2 isolates the impact of a module acting as a constant power source.

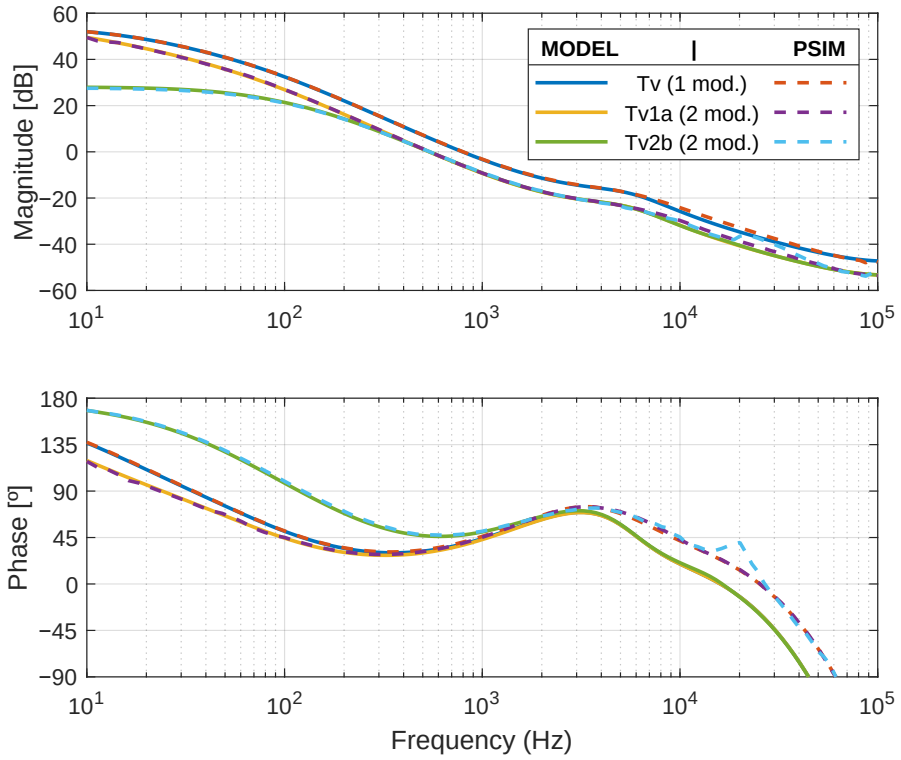


Figure 13. Comparison of voltage loop gains between single- and two-module systems under equivalent power conditions.

In **Case 1** (T_v vs. T_{v1a}), the parallel connection of an idle module reduces the loop gain by a nearly constant 5.9 dB above 10 Hz, while the low-frequency gain remains unchanged (54 dB) . This attenuation shifts the crossover frequency to a lower value (from 794.15 Hz to 539.28 Hz) and slightly reduces the passband gain, leading to a slower transient response. Additionally, the decrease in phase margin (from 38.62° to 30.95°) compromises the relative stability of the system, resulting in a less damped and more oscillatory time-domain response. This modification of the voltage loop arises because the passive module continues to regulate its inductor current, thereby affecting the bus voltage dynamics.

In **Case 2** (T_v vs. T_{v2b}), the presence of a module in device-mode causes a significant reduction in the low-frequency gain (54 dB to 28 dB), stabilizing to a constant reduction of 5.9 dB above 200 Hz. While this also decreases the crossover frequency (from 794.15 Hz to 540.97 Hz) and slows the response, the phase margin increases (from 38.62° to 46.29°), which enhances the system's stability by providing a more damped transient behavior compared to the single-module case. This occurs because the module in device-mode also directly influences the bus voltage dynamics, despite not actively regulating it.

These findings can be extrapolated to systems with a larger number of modules as follows. First, as the number of modules increases, the crossover frequency decreases compared to the single-module voltage loop, leading to a slower transient response. Second, the operating point with the highest number of passive modules results in the smallest phase margin, corresponding to the least damped response and representing the most critical condition for stability. Finally, as the number of modules operating in device-mode increases, the phase margin also increases, leading to a more damped transient response.

The analytical averaged model accurately predicts these phenomena at low-to-mid frequencies. Within the 10 Hz to 1 kHz range, the model exhibits only minor discrepancies with respect to the simulation, with a gain error of 0.08 dB and a phase error of 2° for T_v, and similarly low errors for T_{v1a} (0.75 dB, 2.7°) and T_{v2b} (0.46 dB, 2°).

6.2. Impact of Droop Control Strategy on Voltage Loop Gain

This section evaluates the influence of the droop control strategy by comparing the voltage loop gain with a resistive V-I slope ($G_{droop,n} = -0.1$ V/A) against a conventional zero-slope (null) characteristic.

As shown in Figure 14, implementing droop control introduces a load-dependent steady-state voltage deviation, as the effective reference is modified by the output current. In contrast, the zero-slope configuration maintains a fixed reference across the entire current range (0 A to I_{elb}), eliminating steady-state error. However, in modular architectures, this deviation is an intentional design trade-off to ensure load sharing. The use of PI regulators ensures that the error between the output voltage and the *modified* reference ($v'_{ref} = v_{ref} + G_{droop} i_{o,est}$) remains zero at any steady-state operating point.

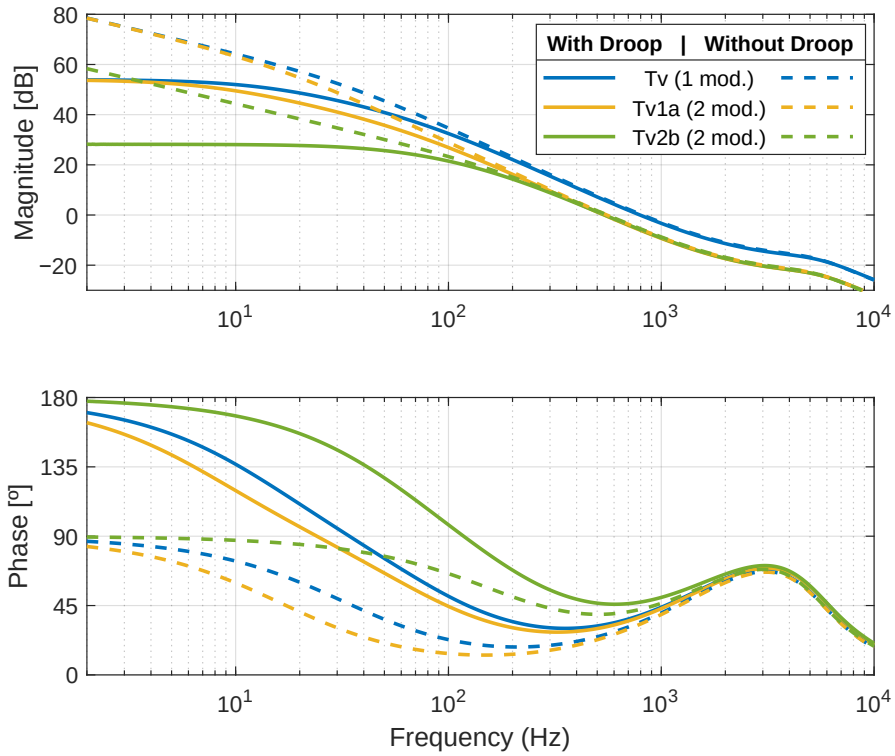


Figure 14. Voltage loop gains for single- and multi-module systems with and without droop control.

Furthermore, the results indicate that the inclusion of droop control enhances the phase margin of the voltage loop. This added phase lead results in a more damped and stable time-domain response, facilitating the integration of multiple modules into the DC bus.

7. Conclusions

In this work, analytical small-signal models for both single-module and two-module satellite power distribution systems, assuming boost mode operation and resistive bus load, have been developed and validated. The validation process, conducted through both high-fidelity simulations and experimental measurements with a frequency response analyzer, demonstrates a strong correlation across a wide bandwidth.

The results confirm that the continuous-time averaged modeling approach is highly effective for the analysis of voltage loop dynamics and the design of digital regulators. Specifically, the high degree of accuracy observed at low frequencies allows for a precise evaluation of how module integration modifies the voltage loop passband. Furthermore, the model's reliability near the crossover frequency ensures its suitability for practical

controller tuning in satellite power systems. It was also noted that the model's fidelity improves significantly in configurations utilizing output capacitors with low ESR values, where the small-ripple approximation is more robust.

The two-module system was characterized as a multi-state converter with four topological states and two control variables. A key finding of this study is that despite the implementation of a distributed control strategy, significant dynamic coupling exists between the control variables of parallel modules. This cross-coupling implies that the addition of parallel units inherently modifies the global system dynamics. This phenomenon was successfully demonstrated by comparing the voltage loop gains of single- and two-module configurations under equivalent operating and power conditions, and the results suggest that these conclusions can be extended to systems with a larger number of modules.

Moreover, this modeling approach is also applicable to the buck mode, where the only difference lies in the open-loop model, and in the estimation of the module's load current, which in this case is $i_{o,est} = i_L$. The proposed approach can also be applied to analyze scenarios in which a module charges a battery connected to its input. In this case, the control block responsible for battery charging sets the current reference to a specified value in the source direction, causing the module to exhibit dynamics equivalent to those of an idle module ($\hat{i}_{ref} = 0$).

Future work should address the extension and validation of the proposed model under non-resistive loading conditions, as space systems often include dynamic or nonlinear loads that may significantly influence the system dynamics. In this regard, a systematic analysis could be carried out by applying the Extra Element Theorem [23] to the derived model.

In summary, the proposed modeling framework provides a reliable and computationally efficient tool for designers to predict the interaction between modular converters in decentralized DC microgrids, facilitating the development of scalable and robust power architectures for space applications.

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Conflicts of Interest: The authors declare no conflicts of interest.

Appendix A

State-space matrices of the single-module system:

$$\mathbf{A}_0 = \begin{bmatrix} -\frac{r_L}{L} + \frac{R_o r_C}{L(R_o+r_C)} & -\frac{R_o}{L(R_o+r_C)} \\ \frac{R_o}{C_o(R_o+r_C)} & -\frac{1}{C_o(R_o+r_C)} \end{bmatrix} \quad \mathbf{A}_1 = \begin{bmatrix} -\frac{r_L}{L} & 0 \\ 0 & -\frac{1}{C_o(R_o+r_C)} \end{bmatrix}$$

$$\mathbf{B}_0 = \mathbf{B}_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad \mathbf{C}_0 = \begin{bmatrix} 1 & 0 \\ \frac{R_o r_C}{R_o+r_C} & \frac{R_o}{R_o+r_C} \end{bmatrix} \quad \mathbf{C}_1 = \begin{bmatrix} 1 & 0 \\ 0 & \frac{R_o}{R_o+r_C} \end{bmatrix} \quad \mathbf{E}_0 = \mathbf{E}_1 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

State-space matrices of the two-module system:

$$\mathbf{A}_{00}=\begin{bmatrix} -\frac{r_L+R_{eq}}{L} & -\frac{R_{eq}}{L} & -\frac{R_{eq}}{Lr_C/2} \\ -\frac{R_{eq}}{L} & -\frac{r_L+R_{eq}}{L} & -\frac{R_{eq}}{Lr_C/2} \\ \frac{R_{eq}}{C_o r_C} & \frac{R_{eq}}{C_o r_C} & -\frac{R_{eq}}{C_o R_o r_C} \end{bmatrix} \quad \mathbf{A}_{11}=\begin{bmatrix} -\frac{r_L}{L} & 0 & 0 \\ 0 & -\frac{r_L}{L} & 0 \\ 0 & 0 & -\frac{R_{eq}}{C_o R_o r_C} \end{bmatrix}$$

$$\mathbf{A}_{10}=\begin{bmatrix} -\frac{r_L}{L} & 0 & 0 \\ -\frac{R_{eq}}{L} & -\frac{r_L+R_{eq}}{L} & -\frac{R_{eq}}{Lr_C/2} \\ 0 & \frac{R_{eq}}{C_o r_C} & -\frac{R_{eq}}{C_o R_o r_C} \end{bmatrix} \quad \mathbf{A}_{01}=\begin{bmatrix} -\frac{r_L+R_{eq}}{L} & -\frac{R_{eq}}{L} & -\frac{R_{eq}}{Lr_C/2} \\ 0 & -\frac{r_L}{L} & 0 \\ \frac{R_{eq}}{C_o r_C} & 0 & -\frac{R_{eq}}{C_o R_o r_C} \end{bmatrix}$$

$$\mathbf{C}_{00}=\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ R_{eq} & R_{eq} & \frac{R_{eq}}{r_C/2} \end{bmatrix} \quad \mathbf{C}_{11}=\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & \frac{R_{eq}}{r_C/2} \end{bmatrix} \quad \mathbf{C}_{10}=\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & R_{eq} & \frac{R_{eq}}{r_C/2} \end{bmatrix} \quad \mathbf{C}_{01}=\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ R_{eq} & 0 & \frac{R_{eq}}{r_C/2} \end{bmatrix}$$

$$\mathbf{B}_{00}=\mathbf{B}_{11}=\mathbf{B}_{10}=\mathbf{B}_{10}=\begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \\ 0 & 0 \end{bmatrix} \quad \mathbf{E}_{00}=\mathbf{E}_{11}=\mathbf{E}_{10}=\mathbf{E}_{01}=\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \quad R_{eq}=\frac{R_o r_C/2}{R_o+r_C/2}$$

Equation (17):

$$T_{v1(a)}(s)=\left.\frac{\hat{u}_{v2,m1}}{\hat{u}_{v1,m1}}\right|_{\hat{i}_{ref2}=0}=\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} M^{-1} b$$

$$M=\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & -S_v & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & -G_{droop1} \\ 0 & -C_v & 1 & 0 & 0 & 0 & S_i & 0 & 0 \\ 0 & 0 & -C_i G_{mod} & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & C_i G_{mod} S_i & 0 \\ 0 & 0 & 0 & -G_{vd1} & -G_{vd2} & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -G_{id11} & -G_{id12} & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & -G_{id21} & -G_{id22} & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & I_{L1} & 0 & 0 & -D_1' & 0 & 1 \end{bmatrix} \quad b=\begin{bmatrix} 0 \\ -1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Equation (18):

$$T_{v2(b)}(s)=\frac{\hat{u}_{v2,m2}}{\hat{u}_{v1,m2}}=\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} M^{-1} b$$

$$M=\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & -S_v & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -G_{droop2} \\ 0 & -C_v & 1 & 0 & 0 & 0 & 0 & S_i & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & C_i G_{mod} C_v S_v & C_i G_{mod} S_i & 0 & -C_i G_{mod} C_v G_{droop1} & 0 \\ 0 & 0 & -C_i G_{mod} & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -G_{vd1} & -G_{vd2} & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -G_{id11} & -G_{id12} & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -G_{id21} & -G_{id22} & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & I_{L1} & 0 & 0 & -D_1' & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & I_{L2} & 0 & 0 & -D_2' & 0 & 1 \end{bmatrix} \quad b=\begin{bmatrix} 0 \\ -1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

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