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Switching Characteristics and Mechanism Using Al₂O₃ Interfacial Layer in Al/Cu/GdO_x/Al₂O₃/TiN Memristor

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Received: 19 July 2020; Accepted: 29 August 2020; Published: 7 September 2020

Abstract: Resistive switching characteristics by using the Al₂O₃ interfacial layer in an Al/Cu/GdO_x/Al₂O₃/TiN memristor have been enhanced as compared to the Al/Cu/GdO_x/TiN structure owing to the insertion of Al₂O₃ layer for the first time. Polycrystalline grain, chemical composition, and surface roughness of defective GdO_x film have been investigated by transmission electron microscope (TEM), X-ray photoelectron spectroscopy (XPS), X-ray diffraction (XRD), and atomic force microscopy (AFM). For bipolar resistive switching (BRS) characteristics, the conduction mechanism of high resistance state (HRS) is a space-charge limited current for the Al/Cu/GdO_x/TiN device while the Al/Cu/GdO_x/Al₂O₃/TiN device shows Schottky emission. However, both devices show Ohmic at a low resistance state (LRS). After the device has been SET, the Cu filament evidences by both TEM and elemental mapping. Oxygen-rich at the Cu/GdO_x interface and Al₂O₃ layer are confirmed by energy dispersive X-ray spectroscopy (EDS) line profile. The Al/Cu/GdO_x/Al₂O₃/TiN memristor has lower RESET current, higher speed operation of 100 ns, long read pulse endurance of >10⁹ cycles, good data retention, and the memristor with a large resistance ratio of >10⁵ is operated at a low current of 1.5 μA. The complementary resistive switching (CRS) characteristics of the Al/Cu/GdO_x/Al₂O₃/TiN memristor show also a low current operation as compared to the Al/Cu/GdO_x/TiN device (300 μA vs. 3.1 mA). The transport mechanism is the Cu ion migration and it shows Ohmic at low field and hopping at high field regions. A larger hopping distance of 1.82 nm at the Cu/GdO_x interface is obtained as compared to a hopping distance of 1.14 nm in the Al₂O₃ layer owing to a larger Cu filament length at the Cu/GdO_x interface than the Al₂O₃ layer. Similarly, the CRS mechanism is explained by using the schematic model. The CRS characteristics show a stable state with long endurance of >1000 cycles at a pulse width of 1 μs owing to the insertion of Al₂O₃ interfacial layer in the Al/Cu/GdO_x/Al₂O₃/TiN structure.

Keywords: GdO_x/Al₂O₃; Cu filament; complementary resistive switching; hopping conduction; nonvolatile memory

1. Introduction

Increasing demands on data storage in computing and mobile electronics are pushing the development of memories that continue to overcome the limits in scalability, storage-density, operation speed, and low power consumption [1,2]. Among several candidates of non-volatile memories, resistive random access memory (RRAM) has attracted much attention because of its potential to fulfill the above requirements [3–6]. Recently, cation migration based conductive bridging RAM [7,8] using several metal-oxides such as Al_2O_3 [9–13], Ta_2O_5 [12,14], SiO_2 [15–17], HfO_2 [18,19], Gd_2O_3 [20,21], ZrO_2 [22], and LSMO [23,24] have been reported. However, unstable and inferior switching uniformity with a higher RESET current of a single switching layer needs to be improved for future practical application [20,21].

In order to mitigate those difficulties, the bi-layer concept has been introduced which leads to filament stability by controlling the Cu ion migration and reducing the RESET current [7,8,21,22]. Although there are numerous advantages of RRAM, the sneak path current is affecting its use in practical applications. To resolve the sneak path leakage current, the CRS concept has been introduced in which two BRS devices are anti-serially connected to one another [25,26]. Soni et al. [27] have reported the CRS characteristics in two anti-serially connected $\text{Pt}/\text{SiO}_x/\text{Ge}_{0.3}\text{Se}_{0.7}/\text{Cu}$ structures as well as in serially connected $\text{Pt}/\text{SiO}_x/\text{Ge}_{0.3}\text{Se}_{0.7}/\text{Cu}$ and $\text{Pt}/\text{Ge}_{0.3}\text{Se}_{0.7}/\text{SiO}_x/\text{Cu}$ structures. In our previous study [28], we have reported CRS characteristics using the $\text{IrO}_x/\text{GdO}_x/\text{Al}_2\text{O}_3/\text{TiN}$ RRAM structure. Although there are some reports on BRS and CRS characteristics by using different structures [28,29], however, the Al_2O_3 interfacial layer in a $\text{Al}/\text{Cu}/\text{GdO}_x/\text{Al}_2\text{O}_3/\text{TiN}$ structure has been reported for the first time. A defective GdO_x film [30] will be formed, which will easily help the migration of Cu ions under external bias and impact of inserting a thin Al_2O_3 layer leads to control of Cu ions migration owing to its lower ionic mobility [31]. Hence, insertion of Al_2O_3 interfacial layer in the $\text{Al}/\text{Cu}/\text{GdO}_x/\text{Al}_2\text{O}_3/\text{TiN}$ structure helps control the metallic filament formation/dissolution. This will also help reduce the operation current in BRS/CRS performance as compared to the single Al_2O_3 switching layer [13]. In this new structure, the GdO_x is used as a Cu buffer layer, which easily helps the Cu filament forming/dissolving in the Al_2O_3 layer under low energy. As compared to other structures, this is very useful in the near future.

In this work, the BRS and CRS characteristics by using a new $\text{Al}/\text{Cu}/\text{GdO}_x/\text{Al}_2\text{O}_3/\text{TiN}$ device have improved performance as compared to the $\text{Al}/\text{Cu}/\text{GdO}_x/\text{TiN}$ devices. A small device size of $0.6 \times 0.6 \mu\text{m}^2$ with a polycrystalline grain and defective GdO_x films are confirmed by TEM, XPS, and XRD. The surface roughness of GdO_x film is also observed by AFM. The Cu filament is observed by using high-resolution TEM (HRTEM) and EDS mapping. The CRS characteristics are also observed. The current conduction mechanism is also explained. By inserting a thin Al_2O_3 interfacial layer in the $\text{Al}/\text{Cu}/\text{GdO}_x/\text{Al}_2\text{O}_3/\text{TiN}$ memristor, this shows excellent BRS and CRS characteristics owing to control the Cu ion migration.

2. Materials and Methods

Memristor Fabrication Process

First, a 200 nm-thick SiO_2 layer was grown by thermal oxidation on an 8-inch Si wafer. For a bottom electrode (BE), a 50 nm-thick TiN layer followed by a 150 nm-thick Ti was deposited on the SiO_2/Si substrate. Then, a 150 nm-thick SiO_2 as an insulating layer was deposited on the TiN/Ti/ SiO_2/Si stack. This SiO_2 layer was the patterned via-holes. Then, a thin Al_2O_3 interfacial layer with a thickness of 2 nm was deposited on TiN BE by the rf sputtering process. The Al_2O_3 target with a purity of 99.9% was used. Next, the Gd_2O_3 layer with a thickness of approximately 17 nm was deposited. During deposition, some amount of oxygen was removed and the Gd_2O_3 film became GdO_x ($x < 1.5$). In order to deposit a top electrode (TE), a Cu layer with a thickness of 40 nm and a 160 nm-thick Al as a capping layer were deposited in situ by thermal evaporation. Finally, the lift-off process was performed to obtain $\text{Al}/\text{Cu}/\text{GdO}_x/\text{Al}_2\text{O}_3/\text{TiN}$ (S2) memristors. The memory structure is shown by

the sketch (Supplementary Information). For comparison, the Al/Cu/GdO_x/TiN (S1) structure was also prepared without an Al₂O₃ interfacial layer. Microstructure, device size, and EDS mapping were observed by using the TEM-FEI Osiris system, which was operated at 200 kV. A crystalline Gd₂O₃ film was found by using the standard BRUKER XRD system with a Cu-K α source and wavelength was 1.541 Å. Non-stoichiometric GdO_x and stoichiometric Al₂O₃ films were investigated by XPS with an Al (K α) monochromatic X-ray and energy of 1486.6 eV was applied. The base vacuum pressure was 1×10^{-9} Torr. The crystalline film was confirmed by grazing incidence XRD (GIXRD), and the film was deposited on the Si substrate. AFM images were taken in tapping mode by using the Innova scanning probe microscope (AFM-SPM) system. Resistive switching characteristics were obtained by applying sweep voltage on the Al/Cu TE whereas the TiN BE was grounded. The electrical characterizations were performed by using both Agilent 4156C and B1500A semiconductor parameter analyzers.

3. Results and Discussion

3.1. Material Characteristics

3.1.1. TEM Image of Pristine Memristor

Figure 1a shows a typical TEM image of a S2 memristor. The device size is approximately $0.6 \times 0.6 \mu\text{m}^2$. Figure 1b,c represents a high-resolution TEM image of inside and outside of the via-hole device, respectively. Each layer is observed clearly and thicknesses of the GdO_x and Al₂O₃ layers are found to be 17 and 1.6 nm, respectively. The HRTEM image shows a polycrystalline GdO_x film whereas an Al₂O₃ film shows amorphous. A clear crystallinity of GdO_x film shows in the middle as compared to the GdO_x/Cu interface and this interface shows a white color than the middle. This indicates that oxygen content at the Cu/GdO_x interface is higher than the middle of the GdO_x layer, which has been explained later. The inset of Figure 1c shows the Fast Fourier Transform (FFT) image of the GdO_x film. The ring pattern of FFT indicates polycrystalline of the GdO_x film. The d-spacing of highly intensive dots is calculated to be 3.11 Å, which represents the d-spacing value (3.06 Å) of Gd₂O₃ (100) plane [32].

Figure 1. TEM characterization of the S2 memristors with a typical size of $0.6 \times 0.6 \mu\text{m}^2$. (a) Cross-sectional TEM image of a pristine memristor. HRTEM images show at (b) inside and (c) outside of the via-hole regions. The inset of (c) shows the fast Fourier transform (FFT) image of GdO_x film. The ring pattern in FFT indicates polycrystalline of GdO_x film.

3.1.2. XPS Analysis

The composition and chemical bonding of the $\text{GdO}_x/\text{Al}_2\text{O}_3$ bilayers on the SiO_2/Si substrate are analyzed by XPS spectra with their appropriate peak fitting (Figure 2). An XPS spectrum of Gd shows $3d_{3/2}$ and $3d_{5/2}$ doublet with a binding energy of 1220.5 and 1188.3 eV, respectively (not shown here), which correspond to the binding energy of $\text{Gd}3d_{3/2}$ and $3d_{5/2}$ spin-orbits at 1218 and 1186 eV for the Gd_2O_3 film, respectively [33]. The XPS spectrum of $\text{Gd}3d_{5/2}$ is shown in Figure 2a. The peak positions at 1188.71 and 1185.82 eV are identified to be Gd_2O_3 $3d_{5/2}$ and metallic $\text{Gd}3d_{5/2}$ peaks, respectively. The area ratio of $\text{Gd}/\text{Gd}_2\text{O}_3$ is approximately 0.69:1, which shows a higher percentage of Gd in the Gd_2O_3 film.

Figure 2. XPS analysis of the GdO_x and Al_2O_3 layers. (a) Gd_2O_3 $3d_{5/2}$ spectra and (b) $\text{O}1s$ spectra in Gd_2O_3 film, (c) $\text{Al}2p$ spectra and (d) $\text{O}1s$ spectra in Al_2O_3 film on the SiO_2/Si substrate.

Figure 2b shows the $\text{O}1s$ core-level spectra for the Gd_2O_3 films. This spectrum shows three distinct peaks. The strong peak at 531.6 eV corresponds to the oxygen in the Gd_2O_3 film, whereas lower and higher binding energy peaks at 529.4 eV ($\text{O}1s\text{ B}$) and 532.9 eV ($\text{O}1s\text{ A}$) are attributed to the hydroxyl and carbonate groups raised from the atmospheric exposure because of reactivity of Gd_2O_3 material [34,35]. Moreover, the lower binding energy peak at 529.4 eV can also correspond to the Gd-O bonding which indicates Gd-rich Gd_2O_3 [36]. On the other hand, oxygen can bind loosely with Gd on a polycrystalline grain or defective Gd_2O_3 switching material (SM), i.e., GdO_x film. The $\text{Al}2p$ and $\text{O}1s$ peaks in Al_2O_3 layer are shown in Figure 2c,d, respectively. The $\text{Al}2p$ and $\text{O}1s$ peaks are located at 75.8 and 532.5 eV, respectively. This indicates a strong Al-O bonding with a stoichiometric Al_2O_3 interfacial layer.

3.1.3. XRD Pattern and AFM Image

In addition, the crystalline Gd_2O_3 film is confirmed by XRD pattern (Figure 3a). The peak at 28.7° (2θ) corresponds to (100) plane of Gd_2O_3 [31] whereas the peak at 55.02° (2θ) corresponds to (311) plane of Si [37]. This low intensity (100) peak is owing to the thin and defective (or oxygen vacancy) polycrystalline GdO_x film. Figure 3b,c represents the AFM images on SiO_2/Si and GdO_x/Si substrates, respectively. The root-mean-square (R_q) and average (R_a) values of the GdO_x films are found to be 0.688 and 0.518 nm, and those values are higher than the values of 0.321 and 0.257 nm for the SiO_2 layer, respectively. This higher roughness of the GdO_x films comes from the polycrystalline grains.

An explanation of higher defective GdO_x film is as follows. During deposition of Al_2O_3 , the film will contain some defects because of plasma. After Gd_2O_3 deposition on AlO_x layer, the underneath layer took oxygen (O^{2-}) from the Gd_2O_3 layer resulting in higher defective GdO_x and stoichiometric Al_2O_3 layers that can be formed. In the case of the $\text{GdO}_x/\text{Al}_2\text{O}_3$ bilayers, the Gd_2O_3 SM can be defective by two ways: (1) During deposition by electron beam evaporation and (2) oxygen consumption by the Al_2O_3 layer. Therefore, this higher defective GdO_x layer or oxygen vacancy will easily help the migration of Cu ions whereas the Al_2O_3 layer will help in formation/dissolution of the filaments under an external electric field, which has a benefit for improvement of resistive switching memory characteristics as discussed later.

Figure 3. XRD and AFM characterization. (a) XRD pattern of the GdO_x/Si stack which represents the crystalline GdO_x film. Three-dimensional (3D) AFM images of (b) SiO_2/Si and (c) GdO_x/Si stacks with a scan area of $500 \times 500 \text{ nm}^2$ are shown.

3.2. Bipolar Resistive Switching Characteristics

3.2.1. Current-Voltage Switching and Transport Mechanism

Bipolar current-voltage (I–V) characteristics and transport mechanism of the S1 and S2 memristors are shown in Figure 4. Typical forming voltages (V_{form}) are 2.4 and 2.1 V for the S1 and S2 devices, respectively (Figure 4a). However, the S2 devices have shown a lower and uniform V_{form} value as compared to the S1 devices (2.44 vs. 2.62 V at 50% probability) because of $\text{GdO}_x/\text{Al}_2\text{O}_3$ bilayers (not shown here). Hundred devices for each structure have been measured randomly.

Typical bipolar I–V characteristics of the S1 and S2 devices after forming are shown in Figure 4b. The sweeping voltage direction is shown in arrow marks 1 to 4 ($0 \rightarrow +2 \rightarrow 0 \rightarrow -1 \rightarrow 0 \text{ V}$). The SET voltage (V_{SET}) is approximately 0.7 V. The S2 device has a lower RESET current (I_{RESET}) than the S1 devices

(630 μA vs. 2.85 mA), which is due to the Al_2O_3 interfacial layer. Similarly, the average I_{RESET} value of S2 devices at 50% probability is approximately 540 μA from 100 devices (not shown here). Figure 4c depicts the cumulative probability of leakage current for both the S1 and S2 devices. It is known that the leakage current increases by decreasing the switching layer thickness or by increasing the number of defects [38]. Even though the $\text{GdO}_x/\text{Al}_2\text{O}_3$ bilayer has a larger thickness of 19 nm than a single GdO_x layer (17 nm), however, the S2 devices show a higher leakage current than the S1 devices (8.09×10^{-10} A vs. 3.05×10^{-11} A at 50% probability). This is due to a higher defective GdO_x as explained in XPS characteristics (Figure 2).

Considering the device-to-device distribution, the HRS/LRS values at 50% probability are 8.2/0.64 and 9.7/1.4 k Ω for the S1 and S2 devices, respectively. The LRS value of the S2 devices is higher than the S1 devices because of the smaller CF diameter. During formation, Cu atoms can be stored into the GdO_x layer (or buffer layer) and a small diameter of conducting filament (CF) could be formed/dissolved in the Al_2O_3 layer under SET/RESET. However, transport mechanism is one of the key issues to understand the switching characteristics for both the devices as follows. For the S1 devices, the HRS currents for both positive and negative bias regions are plotted in a log-log scale (Figure 4d). The slope values are found to be 1.03–1.11 and 1.85–2.15, which have confirmed the space-charge-limited current (SCLC) conduction mechanism. Sun et al. [39] have also reported the SCLC conduction mechanism even if they have used the Au/CuO-DNA-Al/Au/Si structure. However, both S1 and S2 devices show Ohmic conduction at LRS currents.

Figure 4. Current-voltage and current transport characteristics of the S1 and S2 devices. (a) Formation, (b) typical bipolar resistive switching, (c) cumulative probability of leakage current. (d) Space-charge-limited current (SCLC) conduction of the S1 devices, (e) Schottky conduction of the S2 memristor. (f) Schottky conduction at a high resistance state (HRS) is represented by the energy band diagram. Cu migration is also shown.

To find the HRS current conduction, the HRS currents of the S2 devices are plotted in $\ln(J/T^2)$ vs. $\sqrt{E}$ (Figure 4e). The result is well fitted with Schottky emission (SE) at low field region [40]. By solving the equation of Schottky conduction, the dielectric constant (ϵ_{SE}) and barrier height (Φ_B) are obtained as follows:

$$\epsilon_{SE} = \frac{q^3}{4\pi\epsilon_0(k_B T S)^2} \quad (1)$$

$$\Phi_B = \frac{k_B T I}{q} \quad (2)$$

where k_B is the Boltzmann's constant, T is the absolute temperature, q is the electronic charge, and ϵ_0 is the permittivity of free space, S is the slope, and I is the intercept of linear plot in $\ln(J/T^2)$ vs. $\sqrt{E}$ plot. However, an interesting point to be noted is that when we consider the pristine device thickness, i.e., approximately 19 nm the obtained ϵ_{SE} value is quite low approximately 2. This does not follow the $\epsilon_{SE} = n^2$ (n = refractive index) relation because the reported n value of GdO_x film is <2 within the visible wavelength [41]. If we consider the effective thickness 7.5 nm (dissolution gap after RESET) then the ϵ_{SE} value becomes approximately 3.9, which is within the considerable range and follows the $\epsilon_{SE} = n^2$. This conflict signifies that after the RESET process some of the Cu atoms accumulate inside the GdO_x switching material and reduce the effective thickness of dissolution gap. From Equations (1) and (2), the corresponding Φ_B value at HRS is approximately 0.48 eV.

By considering electron affinities of GdO_x (2.05 eV [42]) and Al_2O_3 (1 eV [43]), energy gaps of GdO_x (5.4 eV [41]) and Al_2O_3 (7.1 eV [44]), and work functions of Cu (4.46 eV [45]) and TiN (4.6 eV [46]), the energy bands are shown in dotted lines under thermal equilibrium at 300 K (Figure 4f). To emit the electron, it is found that the barrier height at the Al_2O_3 /TiN interface is higher than the GdO_x /Cu interface (2.5 vs. 0.94 eV). Under a positive bias on the Cu TE, the energy gap of GdO_x is reduced owing to the Cu migration. After RESET, a dissolution gap at the GdO_x / Al_2O_3 interface and the Al_2O_3 layer is observed, which represents the HRS. Then, Schottky emission is obtained under a positive bias before SET because the electron conducts from the TiN BE and crosses the Al_2O_3 conduction barrier. Furthermore, we can speculate that the filament formation-and dissolution is controlled by the Al_2O_3 interfacial layer. However, the Cu ion migration under an external field is responsible to change HRS to LRS or vice versa, which has been evidenced below.

3.2.2. Evidence of Cu Migration

To find an evidence of Cu ion migration under SET, the S2 memristor with a typical size of $0.6 \times 0.6 \mu m^2$ switches with two consecutive cycles at a high CC of 10 mA. After that, this device was kept at LRS and the device was used for TEM observation, elemental depth profile, and EDS mapping (Figure 5). All layers are observed (Figure 5a), which are seen in a fresh device (Figure 1), except a Cu filament in the GdO_x / Al_2O_3 bilayers. Figure 5b shows the HRTEM image, where a few nanometer size of the dark spots (or Cu filament) are clearly observed in the marked region. To know the elemental composition with and without Cu filament regions, the same device is characterized by the scanning transmission electron microscope (STEM) and corresponding images are shown in Figure 5c,d. The EDS depth profiles with and without Cu filament regions are shown in Figure 5e,f, respectively. The EDS line scans of Ti, N, Gd, O, Al, and Cu elements are taken from the Ti BE to Al capping layer, as shown with arrows in Figure 5c,d.

From the EDS depth profiles of nitrogen (Figure 5f), it is found that the TiN layer with a thickness of approximately 30 nm is shown on Ti. The thickness of GdO_x layer is approximately 17 nm. A low atomic concentration (5.5%) of the Al peaks at the GdO_x /TiN interface is observed because of a thin (2 nm) Al_2O_3 interfacial layer. It is interesting to note that the atomic concentration of O at the TiN BE/ GdO_x interface is higher than the value at the GdO_x /Cu TE interface (20.3 vs. 13.2%), which indicates the oxygen consumption at the Al_2O_3 interfacial layer. Therefore, the Gd_2O_3 layer becomes more defective, which is consistent with XPS results (Figure 2). The EDS line scan profile along the Cu filament is marked at four positions 1, 2, 3, and 4, as shown in Figure 5c,e. The sequence 1, 2, 3, and 4 positions indicates the TiN, Al_2O_3 , GdO_x , and GdO_x /Cu interface layers, respectively. The elemental concentrations of Gd at positions 1, 2, 3, and 4 are 6.5, 11.6, 36.9, and 19.3%, while those values of Cu are 29, 57.5, 16, and 41.9%, respectively. A large amount of Cu at position 2 is diffused into the TiN electrode owing to the high CC of 10 mA. It is noted that this observation is reported for the first time. This suggests that joule heating may help diffuse Cu into TiN. At position 1, a small amount of Gd appears, which is originated during Cu migration. A small amount of Cu at position 3 is observed, which suggests a neck of this CF. Some amount of Cu at position 4 is observed, where Cu

starts to diffuse or this position demonstrates that the CF is formed during the SET operation at the GdO_x/Cu interface.

Figure 5. TEM images, EDS depth profile, and elemental mapping of the S2 devices after SET. TEM image of (a) $0.6 \times 0.6 \mu\text{m}$ sized S2 device and (b) Cu filament. STEM images of (c) with Cu filament and (d) without Cu filament regions are also shown. Elemental depth profiles are measured from Ti to Cu, (e) with Cu filament and (f) without Cu filament regions. Color mapping images of (g) Al, (h) Cu, (i) Gd, (j) O, (k) Ti, and (l) N elements.

EDS elemental mappings of Al, Cu, Gd, O, Ti, and N elements are shown in Figure 5g–l. All elements in these layers are observed clearly. In Figure 5h, the Cu elemental mapping represents a beautiful Cu filament. Thanks to the Cu migration mechanism for real non-volatile memory applications. A hump-like shape of Cu at the Cu/GdO_x interface is observed under the SET operation, which initiates the formation of CF.

Figure 6a shows the HRTEM image of Cu/GdO_x interface without the Cu filament region. The inset in Figure 6a shows the FFT image of marked region. The d-spacing values from the FFT image are found to be $d_1 = 1.99 \text{ \AA}$, $d_2 = 3.08 \text{ \AA}$, and $d_3 = 3.91 \text{ \AA}$. The value of $1.99 \text{ \AA}$ is much closer to the reported value ($2.088 \text{ \AA}$) of Cu (111) plane [47]. However, values of 3.08 and $3.91 \text{ \AA}$ are higher due to overlapping of two Cu crystals, where the d-spacing of moiré fringes is increased [48]. As further investigation of Cu diffusion in TiN BE we have analyzed the HRTEM, as shown in Figure 6b. The Cu filament region is marked as a conical shape with a dotted line. We can clearly observe the diffused Cu in the TiN BE.

The mass percentage values from the EDS depth profile (Figure 5e) of Ti and N are approximately 50 and 20, respectively, which shows non-stoichiometric TiN_x ($x < 1$). Under the high current, this TiN_x BE can allow the Cu diffusion through grain boundaries or defects. Olowolafe et al. [49] have

reported the diffusion of Cu through the TiN_x layer at high temperatures in the Cu/TiN_x/Si structure. Mühlbacher et al. [50] have reported Cu diffusion in a single crystalline TiN layer at high temperatures. Wu et al. also reported the diffusion of Ni in Ni/HfO₂/SiO₂/Si [51] and NiSi/HfO₂/SiO₂/Si [52] structures. The d-spacing value in TiN BE is 2.71 Å, which is similar to the reported value (2.45 Å) of TiN (111) plane [53]. The d-spacing value in the Cu filament region is large 5.43 Å owing to the moiré fringes because diffused Cu crystals and TiN (111) plane are overlapped. To understand the moiré fringes of diffused Cu in TiN, a further study needs to continue in future.

Figure 6. HRTEM images of the S2 devices after SET. (a) Cu TE/GdO_x interface without Cu filament and (b) with Cu filament region. Inset of (a) shows the FFT image of Cu, and corresponding d-spacing values.

Other researchers have reported the Cu or Ag migration in different oxide or solid-electrolyte materials [54,55]. The CF with nanocrystals (NCs) are also reported in the Ag/a-Si/Pt structure by Yang et al. [54] and Cu protrusion in Cu/HfO₂/Pt devices is observed by Lv et al. [19]. Vianello et al. [55] have shown the evidence of the Ag filament using the Ag/Sb-doped GeS₂/W structure. Liu et al. have observed the localized and controllable Ag nano-filament growth in the Ag/ZrO₂/Cu NC/Pt structure by using an in situ TEM technique [56]. The Cu NC was decorated on Pt BE. The superior uniformity of resistive switching properties is obtained, which is owing to enhance and concentrate the electric field on Cu NC sites. This will control the location and orientation of the Ag CFs. On the other hand, the Ag nano-filament is formed by a mass transfer from Ag nano clusters in the Au nano-tip/SiO₂/Ag NC/p-Si structure [16]. The discrete CF is observed by in situ TEM. However, proper decoration of nanocrystals/clusters on the nanoscale device is one of the critical tasks. Yuan et al. have reported the Cu tip size dependent CF nature in the Cu tip/SiO₂/W structure by an in situ TEM [57]. For a smaller Cu tip size, the CF shows as thin and in the shape of discrete clusters owing to the limited ion supply. On the other hand, a wide CF in continuous is observed for the larger Cu tip owing to sufficient ion injection and lower surface energy. This suggests that the discrete CF under nano-ampere operation may be not sufficient for a reliable non-volatile memory application. Further investigation is still needed of nano-ionic memristive switching dynamics at higher resolution and dimensions for experimental study [58,59]. The switching mechanism evolution in greater resolution is a key part for the real non-volatile memory and memory in computing applications. In our study, it is possible to say that the Cu filament formation/dissolution in the Al₂O₃ interfacial layer, which is observed by ex situ HRTEM, will control the resistive switching performance. This has been discussed below.

3.2.3. Device Performance and Low Current Operation

Figure 7a represents program/erase (P/E) endurance of the S1 and S2 devices with a high-speed operation. The P/E voltage and pulse width are applied +1.5 V/−0.8V and 100 ns/1 μs, respectively. The S2 devices show longer P/E cycles as compared to the S1 devices. After a few P/E cycles (~30), the S1 devices show failure because of uncontrolled Cu migration whereas the Cu filament

formation/dissolution is controlled by the Al_2O_3 interfacial layer. Figure 7b shows read pulse endurance of the S1 and S2 devices with a small pulse width of 1 μs . The S1 devices show failure after 5×10^8 cycles whereas the S2 devices show a long read endurance of $>10^9$ cycles even at low current operation of 100 μA . The values of HRS/LRS are approximately 27/260 Ω and 348/379 Ω for the S1 and S2 devices at CC of 500 μA , respectively. The S2 device shows higher resistance ratio of 900 than the value of 100 for the S1 devices owing to the narrower Cu filament formation/dissolution in the Al_2O_3 layer. The HRS (~ 259 k Ω) and LRS (~ 1.57 k Ω) of the S2 devices at a CC of 100 μA also show good stability with a resistance ratio of >150 . Figure 7c represents a stable data retention of about 20,000 s of our S2 memory device at CC of 100 μA .

Figure 7d shows typical bipolar resistive switching (BRS) characteristics of the S2 devices under at a very low CC of 1.5 μA . A high resistance ratio of $>10^5$ at a V_{read} of 0.5 V is achieved, even a low RESET current of <1 nA is observed. Therefore, the S2 device can have a high speed (100 ns) and low current operation of 1.5 μA . Further, the S2 devices has the possibility to exhibit a multi-level cell operation. However, proper controlling of the operation voltage of these devices will have complementary resistive switching (CRS) characteristics in a single cell, which have been reported for the first time in this study below.

Figure 7. Bipolar resistive switching performance of the S1 and S2 devices. (a) Comparison of P/E endurance for the S1 and S2 devices with a high speed of 100 ns. The S1 device has shown failure after a few cycles while the S2 device show longer endurance because of Al_2O_3 interfacial layer. (b) Read endurance of $>10^9$ cycles of the S2 devices at a low current of 100 μA . (c) The S2 device also shows longer retention time about 20,000 s with a good stability at low current compliance of 100 μA . (d) The S2 device shows a low current operation of 1.5 μA with a large HRS/LRS ratio of 10^5 at a read voltage of 0.5 V.

3.3. CRS Phenomena

3.3.1. I–V and Transport Characteristics

Although there are numerous advantages of BRS memory, the sneak path current is affecting its use in practical three-dimensional (3D) cross-point applications. Recently, the CRS phenomena has been proposed to resolve the sneak path effect by using two anti-serially cells [25,26]. In our study,

both S1 and S2 memristors show CRS characteristics after adjusting the sweeping voltage (Figure 8). The voltage sweeping direction is indicated by arrow 1–2. The resistance states are denoted as “0”, “ON” and “1”, respectively.

The electroforming process is applied under a negative bias for both pristine S1 and S2 memristors. The values of V_{SET1} , V_{SET2} , V_{RESET1} , and V_{RESET2} for the S1 devices (Figure 8a) are found to be 0.88, −0.88, −1.4, and 1.3 V, while those values are found to be 0.78, −0.76, −1.3, and 1.1 V for the S2 devices (Figure 8b), respectively. Both devices have been operated under a low voltage of ± 1.5 V. However, the operation current ($\sim 300 \mu A$) of the S2 devices is about 11 times lower than that of the S1 devices (3.1 mA), which is very useful for low power operation of the cross-point memory arrays. Therefore, the Al_2O_3 layer has been beneficial.

Figure 8. Complementary resistive switching characteristics of the S1 and S2 memristors with a size of $8 \times 8 \mu m^2$. Typical CRS characteristics of the (a) S1 and (b) S2 memristors. The S2 device shows a low current operation as compared to the S1 devices because of the Al_2O_3 interfacial layer. Hopping conduction of the S2 devices under (c) larger hopping distance at the Cu/GdO_x interface and (d) smaller hopping distance in the Al_2O_3 layer. (e) Long read pulse endurance of 1000 cycles at a small pulse width of 1 μs is obtained.

To understand the current transport characteristics, the I–V curves of the S2 devices are fitted, as shown in Figure 8c,d. Both “0” and “1” states at low field of negative and positive bias regions confirm the Ohmic conduction with slope values from 1.06 to 1.15. The high field region is plotted in $\ln(J)$ vs. E for the hopping conduction [28], which is expressed below:

$$J_{\text{hopping}} = qanv \exp \left[\frac{qaE}{kT} - \frac{E_a}{kT} \right] \quad (3)$$

where J_{hopping} is the current density due to the hopping conduction, ‘ a ’ is the mean hopping distance, n is the electron concentration in the conduction band of dielectric, v is the frequency of thermal

vibration of electrons at trap sites, and E_a is the activation energy. From Equation (4), we have obtained an equation for hopping distance (a) below:

$$a = \frac{k_B T S}{q} \quad (4)$$

where S is the slope. By using Equation (4), the hopping distance values for both “0” state at a positive bias and “1” state at a negative bias are found to be 1.80 and 1.82 nm (Figure 8c), while those values for both “0” state at a negative bias and “1” state at a positive bias are found to be 1.14 and 1.41 nm (Figure 8d), respectively. Yan et al. [60] have also reported the hopping distance of approximately 2 nm by using the TiW/Cu₂O/Cu structure. Figure 8e shows read stable endurance of 1000 cycles with a small pulse width of 1 μ s. The “ON” state and “1” state are read at a V_{read} of -1 V, whereas the “0” state is read at a $1/2V_{\text{read}}$ of -0.5 V. The non-linearity factor is approximately 6, which is useful for 3D cross-point arrays in the near future.

3.3.2. Memristor Mechanism

The switching mechanism of the CRS characteristics is demonstrated schematically in Figure 9. From this model, the CRS depends on Cu ions' migration through the GdO_x/Al₂O₃ bilayer. Initially, both the Al₂O₃ layer and GdO_x/Cu TE interface are less defective than GdO_x layer, as we can see from the oxygen-rich layer (Figure 5f). When a negative bias is applied on the Cu TE, Gd-O bonds at grain boundary break easily and O²⁻ ions are migrated towards the GdO_x/TiN interface. On the other hand, O²⁻ ions are accumulated at the Cu/GdO_x interface because of the inert Cu electrode or repel O²⁻ ions by Cu electrode, which results in oxygen vacancy filament formation at the Cu/GdO_x interface (Figure 9a).

Figure 9. Schematic demonstration of Cu filament formation/dissolution of CRS characteristics for the Al/Cu/GdO_x/Al₂O₃/TiN structure. (a) Oxygen formation under a negative bias on the TE of a pristine device, (b) “ON” state at $>V_{\text{SET1}}$, (c) “1” state at $>V_{\text{RESET2}}$, (d) “ON” state at $<V_{\text{SET2}}$, and (e) “0” state at $<V_{\text{RESET1}}$. The switching mechanism is due to Cu ions' migration under controlling an external bias of $V_{\text{RESET1}}/V_{\text{RESET2}}$ and the Cu filament is formed/dissolved at the Cu/GdO_x interface and in Al₂O₃ layer.

When a positive voltage is applied on the Cu TE ($>V_{\text{SET1}}$), the Cu ions are generated by oxidation method ($\text{Cu}^0 \rightarrow \text{Cu}^{z+} + ze^-$, $z = 1, 2$) [5] and these Cu ions migrate towards the Al₂O₃/TiN interface through oxygen vacancy under an electric field as well as a Cu filament can be formed in the Al₂O₃ layer and current increases (Figure 9b). Due to more oxygen vacancies in the GdO_x grain boundaries, the Cu ions arrange accordingly and those neutralize by taking the electron from the BE through reduction process ($\text{Cu}^{z+} + ze^- \rightarrow \text{Cu}^0$). At V_{SET1} , the “0” state changes to “ON” state. Further increment of a positive voltage up to 1 V leads to a larger filament diameter in the Al₂O₃ layer. However, if the

positive voltage is more than 1 V then the electric field is developed across the Cu/GdO_x interface and the filament is dissolved (Figure 9c). Maximum dissolution of the filament is observed up to $V_{\text{RESET}2}$ and the “ON” state changes to “1” state of “OFF” state.

Similarly, when a negative voltage ($<V_{\text{SET}2}$) is applied on the TE, the Cu ions migrate towards the Cu/GdO_x interface from GdO_x grain boundaries and the Cu filament is formed at the Cu/GdO_x interface as current increases (Figure 9d). The “1” state changes to “ON” state. By decreasing the negative voltage up to -1.06 V the filament diameter is becoming thicker at the Cu/GdO_x interface. If the negative voltage is less than -1.06 V the dissolution of filament is started in the Al₂O₃ layer and it has a maximum dissolution up to $V_{\text{RESET}1}$ as well as “ON” state changes to “0” state or “OFF” state (Figure 9e). In our study, we did not fabricate the back to back memristor structure. Two cells are the Cu/GdO_x interface and Al₂O₃ layer where the Cu incorporated GdO_x layer is a virtual common electrode in a single Al/Cu/GdO_x/Al₂O₃/TiN memristor, which is equivalent to the back to back memristor structure. The Cu filament formation/dissolution happens at the Cu/GdO_x interface and Al₂O₃ layer alternately by optimizing the RESET voltage and the CRS mechanism explained as well.

Similarly, the CRS mechanism of the Al/Cu/GdO_x/TiN structure can be explained because of TiN_xO_y layer formation at the GdO_x/TiN interface during a negative bias applied on the pristine device (Figure 8a). From Figure 8, it is observed that the Cu ions are transported by hopping. The hopping distance at the Cu/GdO_x interface is higher than the Al₂O₃ layer (1.80 to 1.82 nm vs. 1.14 to 1.41 nm). Therefore, the filament length at the Cu/GdO_x interface is longer than the Al₂O₃ layer. These CRS characteristics show a stable and long endurance of >1000 cycles and are promising for next generation 3D cross-point memory applications.

4. Conclusions

Improved BRS and CRS characteristics of the Al/Cu/GdO_x/Al₂O₃/TiN memristors have been reported as compared to the Al/Cu/GdO_x/TiN devices, for the first time, owing to insertion of Al₂O₃ interfacial layer. The defective polycrystalline grain and composition of the GdO_x film are observed by TEM, XPS, and XRD. The Al/Cu/GdO_x/Al₂O₃/TiN devices show stable BRS characteristics with lower RESET current, stable P/E endurance with a high speed of 100 ns, long read endurance of $>10^9$ cycles with a pulse width of 1 μ s, good data retention, and good device-to-device uniformity. This is due to the Cu filament formation/dissolution in the Al₂O₃ interfacial layer under external bias, which evidences by TEM, EDS elemental mapping, and line scan. The S1 device shows SCLC while the S2 device shows Schottky emission with a barrier height of 0.48 eV. However, both devices show Ohmic conduction at LRS. The S2 devices can be operated at low current of 1.5 μ A with a large resistance ration of $>10^5$, which is very useful for a multi-level operation with low power non-volatile memory applications.

It is found that the CRS characteristics of the S2 memristor are observed at low current operation as compared to the S1 (300 μ A vs. 3.1 mA) because insertion of the Al₂O₃ layer has been beneficial. Transport mechanism of the CRS characteristics is Ohmic at low field and hopping conduction at high field regions. The hopping distance of Cu ion migration is 1.82 nm at the Cu/GdO_x interface while it is 1.14 nm in the Al₂O₃ layer. The CRS characteristics have been explained by using the schematic model. Therefore, the Al/Cu/GdO_x/Al₂O₃/TiN memristor is very useful in the future 3D cross-point memory architecture. This memristor can be extended to an artificial synapse, bio-sensing with a Cu reduction-oxidation mechanism, as well as artificial intelligence (AI) in the future.

Supplementary Materials: The following are available online at <http://www.mdpi.com/2079-9292/9/9/1466/s1>.

Author Contributions: Both C.-F.C. and S.G. wrote the first draft under instruction of S.M.; S.G. measured the memristors; both C.-F.C. and A.S. analyzed and modified the manuscript; Y.-P.C. suggested and discussed to modify the manuscript; S.M. finalized the manuscript. All authors have read and agreed to the published version of the manuscript.

Funding: Ministry of Science and Technology (MOST) Taiwan, under contract numbers: MOST-107-2221-E-182-041 and MOST-108-2221-E-182-026.

Acknowledgments: The authors are grateful to the Ministry of Science and Technology (MOST) Taiwan, under contract numbers: NSC-102-2221-E-182-057-MY2, MOST-107-2221-E-182-041, and MOST-108-2221-E-182-026. The authors are also grateful to MSSCORPS CO., LTD., Hsinchu, Taiwan for their support on TEM, EDS mapping, and EDS depth profile.

Conflicts of Interest: The authors declare no conflict of interest.

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