



Article MFMIS Negative Capacitance FinFET Design for Improving Drive Current

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Abstract: The effect of remnant polarization (P_r), coercive electric-field (E_c), and parasitic capacitance of baseline device on the drive current (I_{ON}) of a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) negative capacitance FinFET (NC FinFET) was investigated. The internal gate voltage in the MFMIS structure was simulated considering gate leakage current. Using technology computer aided design (TCAD) tool, the device characteristic of 7 nm FinFET was quantitatively estimated, for the purpose of modeling the baseline device of MFMIS NC FinFET. The need for appropriate parasitic capacitance to avoid performance degradation in MFMIS NC FinFET was presented through the internal gate voltage estimation. With an appropriate parasitic capacitance, the effect of P_r and E_c was investigated. In the case of E_c engineering, it is inappropriate to improve the device performance for MFMIS NC FinFET without threshold voltage degradation. Rather than E_c engineering, an adequate P_r value for achieving high I_{ON} in MFMIS NC FinFET is suggested.

Keywords: negative capacitance; steep switching; MOSFET

1. Introduction

The negative capacitance field effect transistor (NCFET) was introduced as one of the steep switching devices [1]. The NCFET enables effectively lowering of the power supply voltage of conventional metal oxide semiconductor field effect transistor (MOSFET) because of its super steep switching feature, i.e., sub-60-mV/decade subthreshold swing at room temperature. Unlike the other steep switching devices (e.g., Tunnel FET [2] and nano-electro-mechanical (NEM) relay [3,4]), the NCFET requires an additional ferroelectric layer in its gate stack. Recent studies demonstrated some conspicuous characteristics of NCFET, e.g., improved subthreshold slope, hysteresis-free behavior, and improved DIBL (drain-induced barrier lowering) effect [5–10]. There are several factors which play an important role in determining the performance of NCFET. Those factors include electrical properties, such as coercive electric field (E_c) , remnant polarization (P_r) , and parasitic capacitance of baseline device without ferroelectric layer. E_c and P_r represent the electrical properties of the ferroelectric layer in NCFET. It is known that a hafnium-based ferroelectric material can have various values of E_c and P_r in a certain range, depending on fabrication conditions or dopants [11,12]. Therefore, the impact of E_c , P_r , and parasitic capacitance on NCFET performance was widely investigated [13,14]. Those studies have shown that the NCFET can improve its subthreshold slope and threshold voltage, by taking appropriate values of E_c , P_r , and parasitic capacitance. Additionally, the gate stack structure in NCFET affects the device performance of NCFET. As a gate stack structure for NCFET, a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure was suggested. It was expected that the intermediate metal layer in the MFMIS structure can act as an equipotential layer that alleviates multi-domain effects, so that it generates a higher voltage gain than in a metal-ferroelectric-insulator-semiconductor (MFIS) structure [15,16]. However, Khan et al. [17]

showed that, if there exists a leakage current in the MFMIS structure, it is impossible for the polarization of ferroelectric material to stably exist in the negative capacitance (NC) region (i.e., where dP/dV < 0). This is because the polarization of ferroelectric material slips toward either positive or negative P_r , so that a stabilized voltage gain cannot be expected. There is little study of the impact of those parameters on the device performance of MFMIS NCFET (which is affected by the leakage of intermediate metal). To benefit the performance improvement in MFMIS NCFET, the impact of E_c , P_r , and parasitic capacitance should be investigated. In this work, the impact of E_c , P_r , and parasitic capacitance on MFMIS NC FinFET was investigated through the framework of Khan and 7 nm technology node fin-shaped field effect transistor (FinFET). In addition, we suggest how to design the MFMIS NC FinFET to obtain better device performance.

2. Simulation Method for MFMIS NC FinFET

The MFMIS structure for NCFET was used in this work (see Figure 1a). Due to the leakage current through the internal gate, the ferroelectric layer cannot stay in the negative capacitance region (i.e., negative slope region in polarization-vs.-electric field plot of ferroelectric material), and thereby, the MFMIS NCFET cannot be expected to benefit the stable voltage amplification of the ferroelectric layer. In order to take advantage of using the voltage amplification of the ferroelectric layer in MFMIS NCFET, the dynamic response should be considered. From the perspective of time-dependency, we have used the framework of [17] to estimate the voltage amplification in MFMIS NCFET. In reference [17], the metal-ferroelectric-metal-insulator-metal (MFMIM) structure was modeled as the series-connected circuit network (see Figure 1b). The ferroelectric and dielectric thin film can be modeled as the parallel connection of the capacitor and resistor, and the intermetal layer was modeled as the internal node because the intermetal layer acts as the equipotential surface between the ferroelectric and dielectric film. The polarization-vs.-electric-field behavior of ferroelectric material is analytically described with the Landau-Khalatnikov (LK) Equation (1) as below.

$$V_F = T_F \cdot \left(\alpha \cdot P_F + \beta \cdot P_F^3 \right), \tag{1}$$

where T_F indicates the thickness of ferroelectric layer, and the coefficients (i.e., α and β) are defined as below. $lpha = -rac{3\sqrt{3}}{2} \cdot (E_c/P_r)$, $eta = rac{3\sqrt{3}}{2} \cdot \left(E_c/P_r^3
ight)$

Figure 1. (a) Cross-sectional schematic of MFMIS NC FinFET. (b) Circuit configuration of MFMIM structure. C_D, C_F, C_{para}, R_F, R_D indicates the capacitance of dielectric, ferroelectric layer, and parasitic capacitance; and the resistance of the dielectric and ferroelectric layer, respectively. V_G and V_{INT} represents the gate voltage and internal metal voltage, respectively.

(2)

Applying the Kirchhoff's current law at the internal metal of the series network, we can derive the equation below.

$$\frac{dQ_F}{dt} = \frac{C_D \frac{dV_G}{dt} + \frac{V_G}{R_D} - \left(\frac{1}{R_F} + \frac{1}{R_D}\right) \left(\alpha Q_F + \beta Q_F^3\right)}{1 + C_D \left(\alpha + 3\beta Q_F^2\right)} ,$$
(3)

where R_F , R_D are computed as $V_{app}/(J_L \times A)$, where J_L is the leakage current that is approximately 10^{-2} A/cm² for an applied bias of 1 V [18]. The equation shows the amount of charge in the ferroelectric layer over time. Thus, applying a triangular pulse, the amount of charge in the ferroelectric layer can be estimated, and thereby, it turned out that the MFMIM structure can show the voltage amplification across the ferroelectric layer. Note that the equation is derived from the MFMIM structure, but it is applicable to MFMIS NCFET [19].

Although the MFMIS NCFET can use the negative slope region of ferroelectric layer, the performance degradation of the MFMIS NCFET was expected. The work function engineering was suggested to prevent the performance degradation as well as to enhance the on-state drive current of NCFET [19]. Using metal materials with two different work function values to wrap around the ferroelectric layer, the S-curves in polarization versus voltage plot can be shifted along the voltage axis. The voltage shift can put the ferroelectric into the negative capacitance state (i.e., a smaller amount of V_G can put the ferroelectric into the negative capacitance state). In this simulation work, 0.2 V of V_{offset} is applied through the work function engineering between two metal layers (see Figure 2a). It is noteworthy that the I_D -vs.- V_G and C_G -vs.- V_G of baseline FinFET without MFM layer are estimated using Sentaurus TCAD tool (see Figure 3). The FinFET is modeled in accordance with 7 nm technology of IRDS 2017 roadmap [20]. The physical device dimensions of the FinFET are shown in Table 1. With the estimated I_D -vs.- V_G and C_G -vs.- V_G of baseline FinFET, and the Equation (3), the I_D -vs.- V_G of MFMIS NC FinFET was estimated. In this work, the capacitance condition was well satisfied in all V_G sweep regions [1], so that there is no hysteresis in the I_D -vs.- V_G of MFMIS NC FinFET.



Figure 2. (a) Two S-curves are drawn in polarization versus voltage plot. The red-colored one is the S-curve with work function engineering. The black-colored one is the reference S-curve, for comparison. Note that P_r and E_c of the reference S-curve are 10 μ C/cm² and 0.7 MV/cm, respectively. V_{INT}-vs.-time for (b) various parasitic capacitances, (c) E_c , and (d) P_r . Note that the reference line (black-colored dotted line) indicates the 100 MHz 1 V triangular pulse.



Figure 3. (a) Estimated current-vs.-voltage (I_D -vs.- V_G) of baseline FinFET in log (left) and linear (right) scale. (b) Estimated capacitance-vs.-voltage (C_G -vs.- V_G) of baseline FinFET.

Table 1. The important device parameters for MFMIS NC FinFET.

Device Parameter	Quantity	Device Parameter	Quantity
Gate Length, L _G	18 nm	Oxide Thickness ¹ , T _{OX}	3 nm
Spacer Thickness, L _{SP}	7 nm	Channel Doping, N _{SP}	$10^{15} { m cm}^{-3}$
Fin Height, H _{Fin}	50 nm	Source/Drain Doping, N _{SD}	10^{20} cm^{-3}
Fin Width, W _{Fin}	7 nm	Ferroelectric Thickness, T_F	3 nm

¹ Hafnium oxide was used as the gate oxide.

3. Effect of E_c , P_r , and Parasitic Capacitance on MFMIS NC FinFET

Using (1) 100 MHz 1 V triangular pulses, (2) the parameter of hafnium oxide ferroelectric material, and (3) C_G -vs.- V_G of baseline device, we can find out the voltage-vs.-time characteristic of MFMIS NC FinFET. Note that E_c and P_r used for the S-curve in Figure 2a was 0.7 MV/cm and 10 μ C/cm², respectively [12–14]. The S-curve of ferroelectric material (in which the work function is engineered) is shown in Figure 2a. We used the 100 MHz frequency because if the frequency of sweeping V_G is faster than the "effective time constant" [17], the impact of the leakage current should be neglected.

The impact of varied E_c and P_r of ferroelectric material is shown in Figure 2c,d. As shown in the figures, the internal voltage decreased and was lower than the reference voltage over the whole time. The internal voltage decreases more with increasing E_c . In the case of decreasing P_r , the internal voltage increases but is still lower than the reference voltage over the whole time. The reason for the internal voltage lowering comes from the fact that C_G in the baseline FinFET increases at about 0.3 V (see Figure 3b) due to the inversion layer, and thereby, the internal amplification deteriorates. In this case, an appropriate parasitic capacitance can alleviate the internal voltage lowering, and therefore, it induces a proper voltage amplification in MFMIS structure (see Figure 2b). Total device capacitance (C_{TOT}) can be calculated as (C_G + C_{para}). In the case of 100 aF of parasitic capacitance, V_{INT} of \approx 1.2 V can be implemented by applying a V_G of 1 V. By applying 100 aF of parasitic capacitance to obtain a proper voltage amplification, the impact of E_c and P_r was investigated again. First, increasing E_c makes the amount of voltage amplification (at 1 V of reference voltage) become higher (see Figure 4a). However, at a low reference voltage, the lowering of internal voltage becomes severe. This is because a higher E_c needs additional voltage to put ferroelectric material into the negative slope region. In the case of higher E_c , the lowering of internal voltage can be compensated using different metal (which makes V_{offset} more than 0.2 V) [8].



Figure 4. V_{INT}-vs.-time for a few E_c (**a**) and P_r (**b**). The black-colored dotted reference line indicates the 100 MHz 1 V triangular pulse. The estimated drain current-vs.-gate voltage (I_D -vs.- V_G) of baseline FinFET (see the black-colored solid line) and MFMIS NC FinFET (see the blue/red/purple-colored solid lines) for a few E_c (**c**) and P_r (**d**).

When P_r is increased, the reference voltage (at which the internal voltage is amplified) is pushed to a higher voltage (see Figure 4b). Low P_r (i.e., $5 \,\mu\text{C/cm}^2$) can derive the voltage amplification at a much lower reference voltage. However, the internal voltage at a high reference voltage will be degraded. Additionally, even if P_r becomes lower, it is hard to expect performance enhancement at the deep subthreshold region. In the case of high P_r (i.e., $15 \,\mu\text{C/cm}^2$), the internal voltage loses the voltage amplification in all regions of the reference voltages. Using the internal voltages of various conditions, I_D -vs.- V_G of NC FinFETs were estimated (see Figure 4c,d). In the I_D -vs.- V_G of NC FinFETs, the on-state drive current (I_{ON}) and threshold voltage (V_T) were extracted (see Figure 5). Note that V_T was extracted at the constant current of 100 nA/um. Higher E_c enables the MFMIS NC FinFET to achieve the highest I_{ON} , but, at the same time, it increases V_T significantly. If Pr is in-between 5 μ C/cm² and 10 μ C/cm², I_{ON} and V_T have a trade-off relationship to each other. However, the trade-off is not found in the case of 15 μ C/cm². Even using a low P_r in MFMIS NC FinFET, a significant improvement in V_T is hard to expect.



Figure 5. Scatter plot of extracted I_{ON} and V_T of various MFMIS NC FinFETs.

4. Conclusions

The impact of E_c , P_r , and parasitic capacitance on the performance of MFMIS NC FinFET was investigated. To find out the voltage of intermediate metal in the MFMIS structure, Landau-Khalatnikov model with the gate leakage current was used. Investigating the effect of parasitic capacitance on the MFMIS structure, the parasitic capacitance can be the key knob to control the internal voltage. With 100 aF of parasitic capacitance, E_c and P_r in ferroelectric material were varied between 5–15 μ C/cm² and 0.7–1.2 MV/cm, respectively. In order to design MFMIS NC FinFET to achieve high drive current, E_c of 1.2 MV/cm can induce the highest drive current (i.e., 1.5 times higher drive current than in baseline device). However, the threshold voltage of the NC FinFET was increased (by ≈0.12 V) than that of baseline device. On the other hand, the NC FinFET with an appropriate value of P_r (i.e., 10 μ C/cm²) can achieve 1.4 times higher drive current than baseline device with little V_T degradation.

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Conflicts of Interest: The authors declare no conflict of interest.

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