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Robust Offset-Cancellation Sense Amplifier for an Offset-Canceling Dual-Stage Sensing Circuit in Resistive Nonvolatile Memories

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Abstract: With technology scaling, achieving a target read yield of resistive nonvolatile memories becomes more difficult due to increased process variation and decreased supply voltage. Recently, an offset-canceling dual-stage sensing circuit (OCDS-SC) has been proposed to improve the read yield by canceling the offset voltage and utilizing a double-sensing-margin structure. In this paper, an offset-canceling zero-sensing-dead-zone sense amplifier (OCZS-SA) combined with the OCDS-SC is proposed to significantly improve the read yield. The OCZS-SA has two major advantages, namely, offset voltage cancellation and a zero sensing dead zone. The Monte Carlo HSPICE simulation results using a 65-nm predictive technology model show that the OCZS-SA achieves 2.1 times smaller offset voltage with a zero sensing dead zone than the conventional latch-type SAs at the cost of an increased area overhead of 1.0% for a subarray size of 128 × 16.

Keywords: nonvolatile memory (NVM); offset voltage; offset-canceling dual-stage sensing circuit (OCDS-SC); read yield; sense amplifier (SA); sensing dead zone; time-difference inputs

1. Introduction

Although resistive nonvolatile memories (NVMs) such as spin-transfer-torque random access memory (RAM) and resistive RAM promise higher density and lower power than conventional memories such as static RAM, dynamic RAM, and Flash memory [1–3], they suffer from degraded read yield following technology scaling due to the increased process variation, reduced supply voltage, and decreased read cell current (I_{read}) [4–6].

In general, two output voltages of a sensing circuit (SC), namely, $V_{\mathrm{SA\_data}}$ and $V_{\mathrm{SA\_ref}}$, are introduced into a sense amplifier (SA) to generate a digital signal (zero or one) [7]. Considering the offset voltage in the SA ($V_{\mathrm{SA\_OS}}$) and assuming that the statistical distributions of the input voltage difference (ΔV) between $V_{\mathrm{SA\_data}}$ and $V_{\mathrm{SA\_ref}}$ as well as $V_{\mathrm{SA\_OS}}$ are modeled by a Gaussian distribution, the read yield can be statistically expressed as the read-access pass yield for a single cell ($RAPY_{\mathrm{CELL}}$) [8], i.e.,

$$RAPY_{\mathrm{CELL}} = \frac{\mu_{\Delta V} - \mu_{\mathrm{SA\_OS}}}{\sqrt{{\sigma_{\Delta V}}^2 + {\sigma_{\mathrm{SA\_OS}}}^2}}, \quad (1)$$

where $\mu_{\Delta V}$ ($\mu_{\mathrm{SA\_OS}}$) and $\sigma_{\Delta V}$ ($\sigma_{\mathrm{SA\_OS}}$) are the mean and standard deviation of ΔV ($V_{\mathrm{SA\_OS}}$), respectively.

The recently proposed offset-canceling dual-stage SC (OCDS-SC) has improved $RAPY_{\mathrm{CELL}}$ by reducing $\sigma_{\Delta V}$ due to the offset voltage cancellation in the SC and by increasing $\mu_{\Delta V}$ due to the double-sensing-margin structure [6]. Figure 1a shows an example of the ΔV distribution of the OCDS-SC with $\mu_{\Delta V}$ = 200 mV and $\sigma_{\Delta V}$ = 23 mV. Figure 1b shows that $RAPY_{\mathrm{CELL}}$ can be significantly improved by developing a novel SA with much smaller $\sigma_{\mathrm{SA\_OS}}$ than the typical $\sigma_{\mathrm{SA\_OS}}$ value of 20 mV [7]. If the improved $RAPY_{\mathrm{CELL}}$ value is greater than a target $RAPY_{\mathrm{CELL}}$ value, the read energy can be significantly saved by trading-off the improvement in $RAPY_{\mathrm{CELL}}$ [9,10].

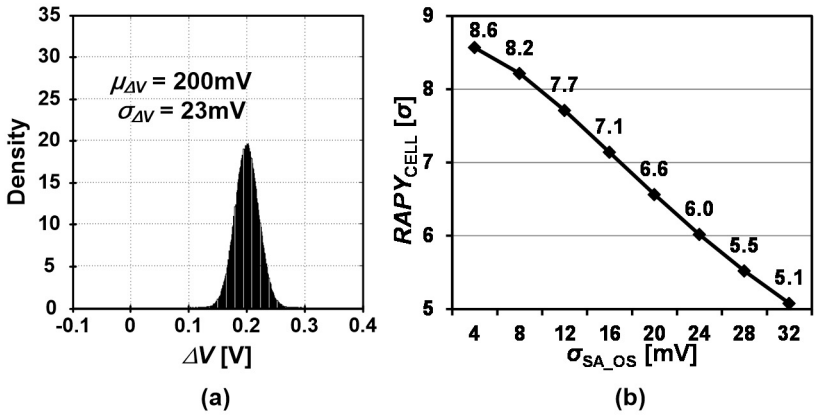

Figure 1. (**a**) Example of ΔV distribution of the offset-canceling dual-stage sensing circuit (OCDS-SC) at $\mu_{\Delta V}$ = 200 mV and $\sigma_{\Delta V}$ = 23 mV. (**b**) $RAPY_{\mathrm{CELL}}$ according to $\sigma_{\mathrm{SA\_OS}}$.

In this paper, we propose an offset-canceling zero-sensing-dead-zone SA (OCZS-SA) that is capable of significantly reducing $\sigma_{\mathrm{SA\_OS}}$ by offset-voltage cancellation with a zero-sensing-dead-zone characteristic. The proposed OCZS-SA achieves 2.1 times smaller $\sigma_{\mathrm{SA\_OS}}$ of 9.62 mV without any sensing dead zone at the cost of an increased area overhead of 1.0% for a subarray size of 128 × 16. The remainder of this paper is organized as follows: Section 2 describes the problems in conventional latch-type SAs; Section 3 introduces the proposed OCZS-SA; Section 4 presents the simulation results and comparison; and Section 5 presents the conclusions drawn from our study.

2. Problems in Conventional Latch-Type SAs

In the OCDS-SC, two SA input voltages, $V_{\mathrm{SA\_data}}$ and $V_{\mathrm{SA\_ref}}$, are generated with a time difference due to the dual-stage sensing operation, as shown in Figure 2. In the first stage, *SS1* is activated, and $V_{\mathrm{SA\_data}}$ generated in the OCDS-SC is introduced into the SA. In the second stage, *SS2* is activated, and $V_{\mathrm{SA\_ref}}$ generated in the OCDS-SC is introduced into the SA. However, because of the time-difference input, a capacitive-coupling problem occurs when a conventional voltage-latched SA (VLSA) is used. Figure 3 shows the capacitive-coupling problem in the VLSA in which $V_{\mathrm{SA\_ref}}$ changes $V_{\mathrm{SA\_data}}$ to some extent (Δ) through parasitic capacitors. This problem increases $\sigma_{\mathrm{SA\_OS}}$ from 20 mV to 30–50 mV, depending on the ratio of the output loading capacitance to the parasitic capacitance. Thus, the SA for the OCDS-SC should not be a VLSA type to avoid the capacitive-coupling problem.

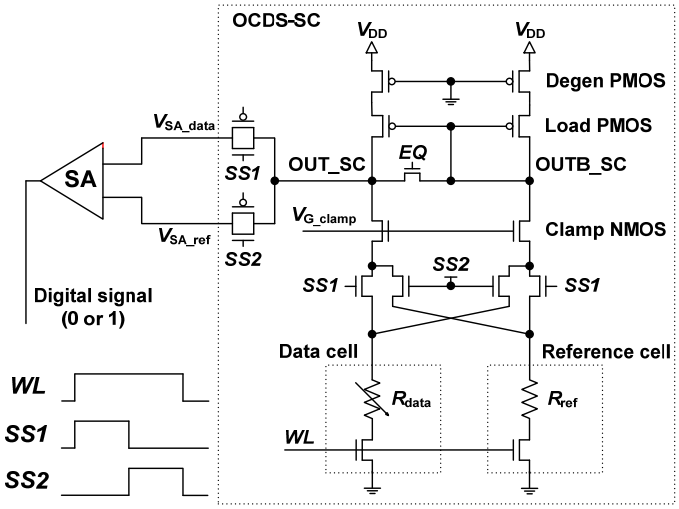

Figure 2. Schematics of the OCDS-SC and symbolized sense amplifier (SA).

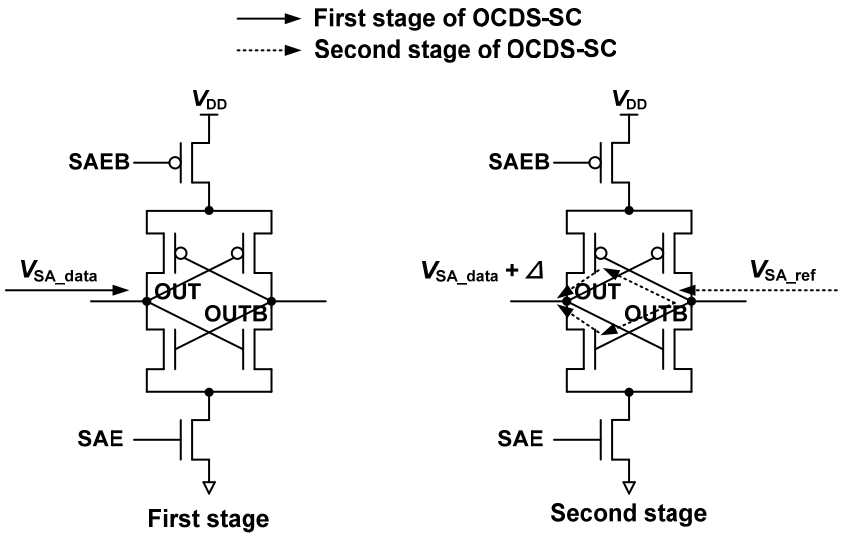

Figure 3. Capacitive coupling problem when voltage-latched SA (VLSA) is used.

Because V_{SA_data} is generated at the operating point between a load PMOS and a clamp NMOS [11,12], the voltage range of V_{SA_data} is from almost GND (in state 0) to almost V_{DD} (in state 1), depending on the sensing time and process variation. Thus, a conventional current-latched SA (CLSA) with a sensing dead zone cannot be applied to the OCDS-SC to achieve a supply-rail sensing capability. Figure 4 shows the sensing-dead-zone problem in a CLSA with an NMOS footswitch (FS-CLSA) and a CLSA with a PMOS headswitch (HS-CLSA) [7]. In the FS-CLSA, the input transistors (MN3 and MN4) should be turned on for correct operation, which means that V_{SA_data} should be greater than V_{THN}, where V_{THN} is the NMOS threshold voltage. Thus, the sensing dead zone of the FS-CLSA becomes $V_{SA\_data} < V_{THN}$. In the same manner, the sensing dead zone of the HS-CLSA becomes $V_{SA\_data} > V_{DD} - |V_{THP}|$, where V_{THP} is the PMOS threshold voltage.

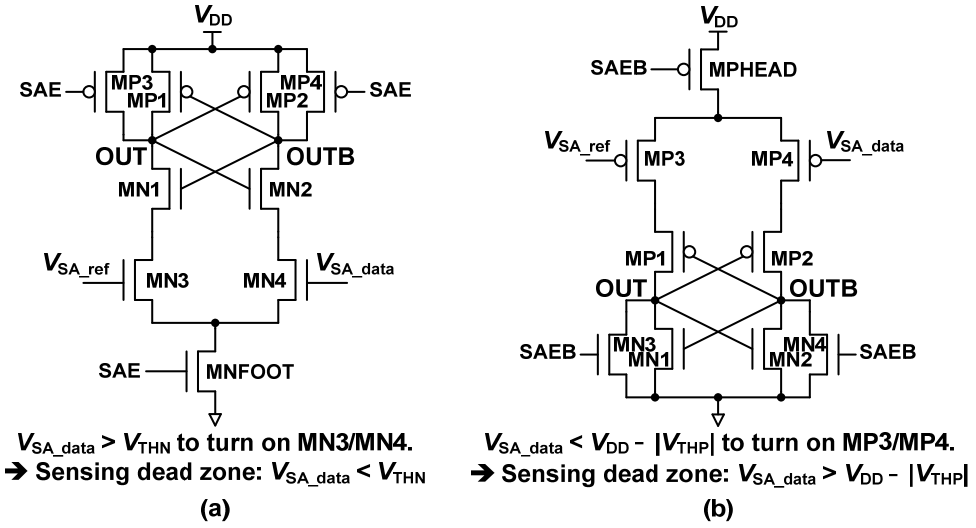

Figure 4. Sensing-dead-zone problem when current-latched SAs (CLSAs) are used in cases of (**a**) footswitch (FS)-CLSA and (**b**) headswitch (HS)-CLSA.

3. Proposed OCZS-SA

In this section, we propose the OCZS-SA that offers two major advantages of offset voltage cancellation and zero sensing dead zone.

3.1. Circuit Diagram and Operation

Figure 5 shows the schematic and timing diagrams of the proposed OCZS-SA. Before we explain the OCZS-SA operation in detail, we should note that the OCZS-SA operation is fully pipelined with the OCDS-SC operation, as shown in the timing diagram in Figure 5. Phases 1 and 2 of the OCZS-SA are pipelined during *SS1*, and phases 3 and 4 are pipelined during *SS2*. Thus, the OCZS-SA does not incur any sensing delay penalty.

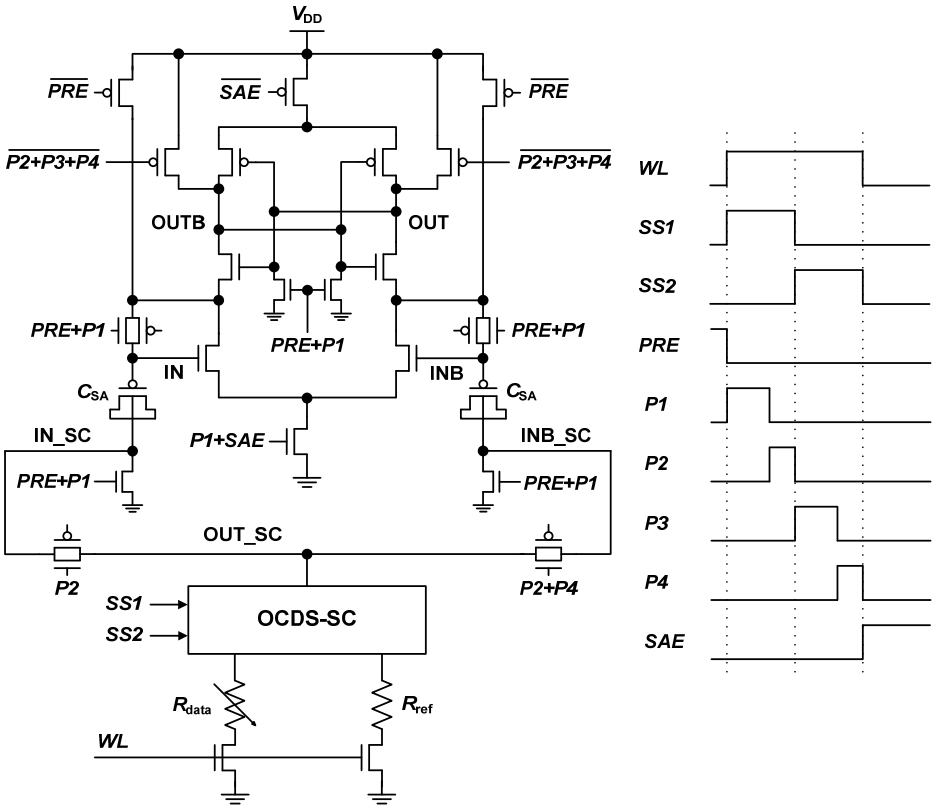

Figure 5. Schematic and timing diagrams of the proposed offset-canceling zero-sensing-dead-zone SA (OCZS-SA).

Figure 6 shows the detailed operations of the OCZS-SA. Before phase 1, the *PRE* signal is high, and the gates of the input NMOSs (IN and INB) are precharged to V_{DD}. During phase 1 (Figure 6a), the *P1* signal is activated, and the IN and INB nodes are discharged to threshold voltages V_{TH1} and V_{TH2} of the input NMOSs, respectively, by the diode-connected configuration. The OUT and OUTB nodes remain GND to isolate the IN and INB nodes. In phase 2 (Figure 6b), the *P2* signal is activated, and V_{SA_data} is captured at both the IN and INB nodes by the capacitive coupling of C_{SA}s. As a result, the voltages in the IN and INB nodes become V_{TH1} + V_{SA_data} and V_{TH2} + V_{SA_data}, respectively. Simultaneously, the OUT and OUTB nodes are precharged to V_{DD} for reliable sensing operation. In phase 3 (Figure 6c), the *P3* signal is activated, and the OCZS-SA waits for V_{SA_ref} to be generated in the OCDS-SC. In phase 4 (Figure 6d), the *P4* signal is activated, and V_{SA_ref} is captured at the INB node. Thus, the voltages in the IN and INB nodes V_{IN} and V_{INB} become V_{TH1} + V_{SA_data} and V_{TH2} + V_{SA_ref}, respectively. After phase 4, the *SAE* signal is activated, and a digital signal (zero or one) is generated by the voltage difference between V_{IN} (= V_{TH1} + V_{SA_data}) and V_{INB} (= V_{TH2} + V_{SA_ref}). We note that the operation after phase 4 is the same as that in the FS-CLSA.

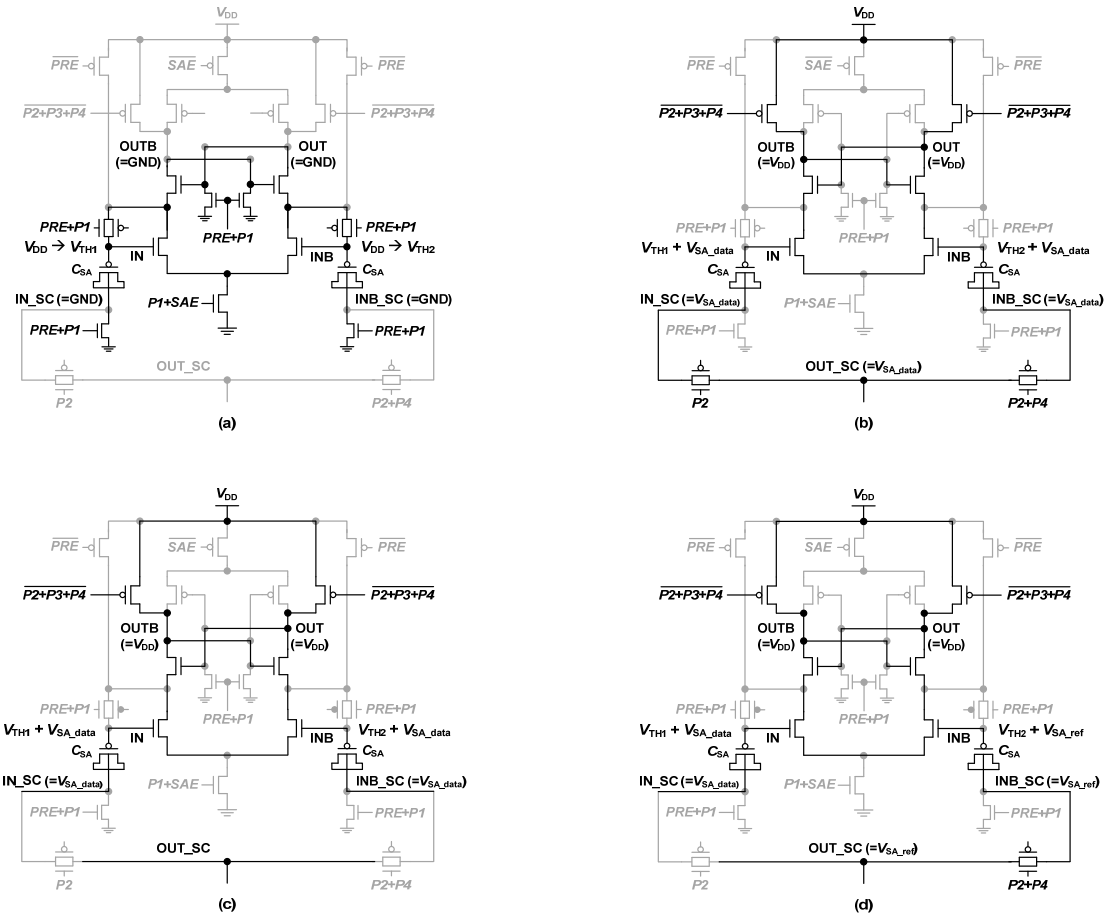

Figure 6. Operations of the OCZS-SA in (**a**) phase 1, (**b**) phase 2, (**c**) phase 3, and (**d**) phase 4.

3.2. First Advantage: Offset Voltage Cancellation

The first advantage of the OCZS-SA is the offset voltage cancellation of the two input NMOSs. As mentioned earlier, in phase 4, V_{IN} and V_{INB} become $V_{TH1} + V_{SA\_data}$ and $V_{TH2} + V_{SA\_ref}$, respectively. Because the overdrive voltage (= $V_{GS} - V_{TH}$) of the input NMOS, where V_{GS} is the input NMOS gate-to-source voltage, does not depend on the V_{TH} variation, a V_{TH} mismatch between the two input NMOSs does not influence σ_{SA_OS}.

In addition, in the FS-CLSA (Figure 4a), because σ_{SA_OS} is dominantly determined by the input NMOSs, σ_{SA_OS} can be effectively reduced by canceling only the offset in the input NMOSs. Figure 7 shows σ_{SA_OS} of the FS-CLSA according to the SA input voltage (V_{SA_data}) when process variation is applied only to the input NMOSs (MN3 and MN4), only to the latch NMOSs (MN1 and MN2), only to the latch PMOSs (MP1 and MP2), and to all the transistors. Figure 7 clearly shows that σ_{SA_OS} is more sensitive to the input NMOSs than to the transistors because the input NMOSs operate in the saturation region, whereas the latch NMOSs operate in the linear region. Thus, the V_{TH} mismatch between MN1 and MN2 becomes less sensitive. Meanwhile, the latch PMOSs do not operate at the initial sensing period. Thus, the V_{TH} mismatch between MP1 and MP2 becomes negligible. The variation in the latch NMOSs of the FS-CLSA has more effect on the σ_{SA_OS} as V_{SA_data} increases because the initial voltage in the small parasitic capacitance between MN1 (MN2) and MN3 (MN4) is discharged much faster with increasing V_{SA_data}, resulting in the latch NMOSs operating in the saturation region.

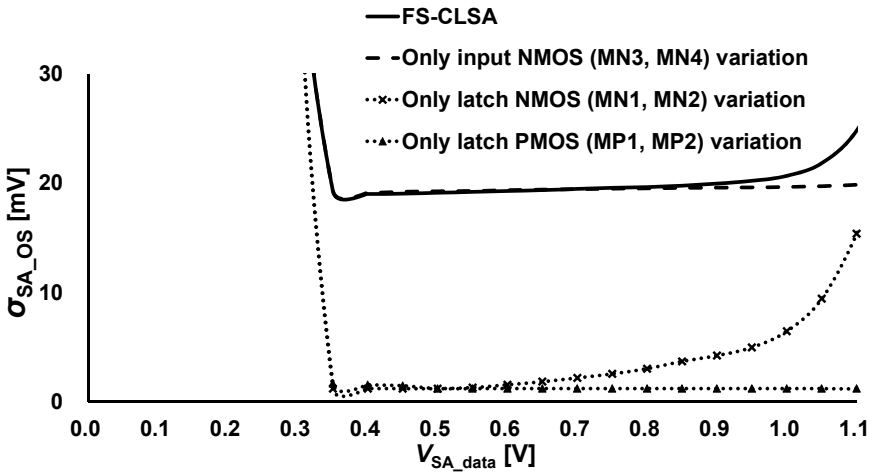

Figure 7. σ_{SA_OS} of the FS-CLSA according to the SA input voltage (V_{SA_data}) when the process variation is applied only to the input NMOSs (MN3 and MN4), only to the latch NMOSs (MN1 and MN2), only to the latch PMOSs (MP1 and MP2), and to all transistors.

3.3. Second Advantage: Zero Sensing Dead Zone

Unlike the FS-CLSA with a sensing dead zone in the region of $V_{SA\_data} < V_{THN}$, as shown in Figure 7, the OCZS-SA does not have any sensing dead zone because in phase 4, V_{IN} and V_{INB} are always greater than V_{TH1} and V_{TH2}, respectively, even if V_{SA_data} and V_{SA_ref} are 0 V. Thus, supply-rail sensing capability is achieved.

4. Simulation Results and Comparison

HSPICE Monte Carlo simulations were performed using a 65-nm predictive technology model at V_{DD} = 1.1 V. To fully pipeline the operation with the OCDS-SC, each phase operation time (T_{P1}, T_{P2}, T_{P3}, and T_{P4} for phases 1–4, respectively) was set to 0.5 ns.

Figure 8 shows σ_{SA_OS} according to the SA input voltage (V_{SA_data}) of the FS-CLSA, HS-CLSA, VLSA with double switches and transmission gate access transistors (DSTA-VLSA) without time-difference inputs, DSTA-VLSA with time-difference inputs, and OCZS-SA. Among the various VLSAs such as the VLSA with an NMOS footswitch and PMOS access transistors, VLSA with a PMOS headswitch and NMOS access transistors, and DSTA-VLSA, only the latter is compared in this paper because only the DSTA-VLSA can achieve a zero sensing dead zone [7]. As mentioned in Section 2, the capacitive-coupling problem increases σ_{SA_OS} of the DSTA-VLSA when time-difference inputs are applied to the DSTA-VLSA. The FS-CLSA and HS-CLSA suffer from the sensing-dead-zone problem. On the other hand, Figure 8 clearly shows that the OCZS-SA achieved 2.1 times smaller σ_{SA_OS} of 9.62 mV on average (minimum σ_{SA_OS} = 5.07 mV at V_{SA_data} = 0.3 V; maximum σ_{SA_OS} = 25.41 mV at V_{SA_data} = 1.1 V) with a zero sensing dead zone. In the same manner as that of the FS-CLSA, the variation in the latch NMOSs of the OCZS-SA significantly affected σ_{SA_OS} as V_{SA_data} increased. Thus, σ_{SA_OS} tended to increase with V_{SA_data}.

Figure 9 shows the average σ_{SA_OS} of the OCZS-SA according to the width of the PMOSCAP for C_{SA} (W_{CSA}) when the PMOSCAP length (L_{CSA}) was 0.2 µm. By considering the area overhead, a W_{CSA} value of 2.0 µm was selected. We note that the effect of the C_{SA} size on the loading of the OCDS-SC is negligible because C_{SA} was serially coupled to the input capacitance (C_{IN}) at nodes IN and INB (total loading capacitance = $C_{SA}//C_{IN} \approx C_{IN}$).

Figure 10 shows normalized σ_{SA_OS} of the OCZS-SA according to T_{P1}. Because σ_{SA_OS} is saturated at T_{P1} of approximately 0.2 ns, the OCZS-SA can be fully pipelined without any problem.

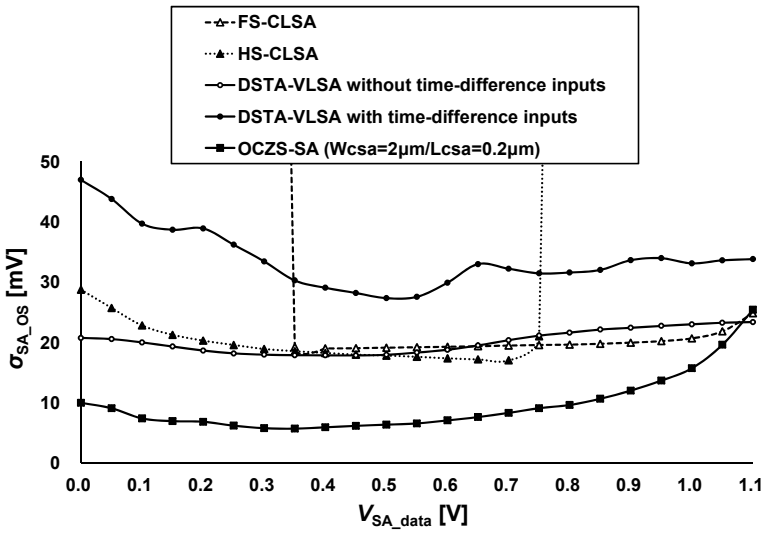

Figure 8. σ_{SA_OS} according to the SA input voltage (V_{SA_data}) for FS-CLSA, HS-CLSA, DSTA-VLSA without time-different inputs, DSTA-VLSA with time-difference inputs, and OCZS-SA. The OCZS-SA achieves σ_{SA_OS} of 9.62 mV on average (minimum σ_{SA_OS} = 5.07 mV at V_{SA_data} = 0.3 V; maximum σ_{SA_OS} = 25.41 mV at V_{SA_data} = 1.1 V).

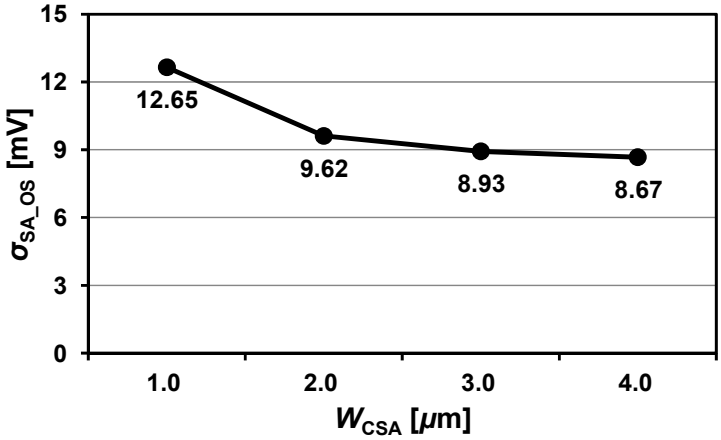

Figure 9. Average σ_{SA_OS} of the OCZS-SA according to W_{CSA} when L_{CSA} = 0.2 μm.

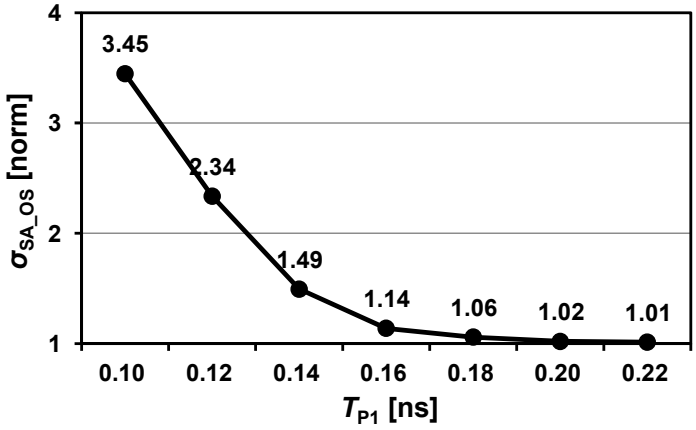

Figure 10. Normalized σ_{SA_OS} of the OCZS-SA according to T_{P1}.

Table 1 lists the performance summary and comparison between the proposed OCZS-SA and the conventional latch-type SAs. The OCZS-SA achieved a zero sensing dead zone and a 2.1 times

smaller σ_{SA_OS} of 9.62 mV, on average, than the FS-CLSA. From the SA viewpoint, owing to the additional transistors and phases, the OCZS-SA requires 37% more layout area (Figure 11a) and 125% more read energy compared with the FS-CLSA. From the array architecture viewpoint, however, the area overhead is only 1.0% when the subarray size is 128 × 16 (Figure 11b), and it decreases as the subarray size increases. In addition, the read-energy consumption of the SC part is much greater (>70 fJ [6]) than that of the SA part. As a result, if $RAPY_{CELL}$, which is improved by employing the OCZS-SA, is greater than a target $RAPY_{CELL}$, the total read energy in the SC and SA can be saved by reducing the SC operation time (T_{SC}) and/or I_{read}. This result can be achieved in spite of the higher read energy of the OCZS-SA, which sacrifices some of the improvement in $RAPY_{CELL}$ but satisfies target $RAPY_{CELL}$. By employing the OCZS-SA together with the OCDS-SC, $RAPY_{CELL}$ increases from 6.0σ to 8.7σ. The $RAPY_{CELL}$ values of 6.0σ and 8.7σ correspond to sensing error rates of 9.87×10^{-10} and 1.66×10^{-18}, respectively. Therefore, the OCZS-SA yields an eighth-order improvement in the read yield relative to the conventional SAs.

Table 1. Performance summary and comparison between the proposed OCZS-SA and conventional latch-type SAs.

	DSTA-VLSA	FS-CLSA	OCZS-SA
Average σ_{SA_OS} (mV)	33.8 [1)]	20.0 [2)]	9.62
Sensing dead zone	None	$V_{SA\_data} < V_{THN}$	None
Normalized area overhead (SA viewpoint)	0.95	1	1.37
Normalized area overhead (Array viewpoint)	0.999	1	1.010
Normalized read energy/bit (SA viewpoint)	0.94	1	2.25
Normalized read energy/bit [3)] (SC + SA viewpoint)	1.43	1	0.84

[1)] Due to the capacitive coupling problem. [2)] Sensing dead zone is not included. [3)] Read energy when the minimum I_{read} that satisfies a target $RAPY_{CELL}$ of 6σ is applied at T_{SC} = 2 ns.

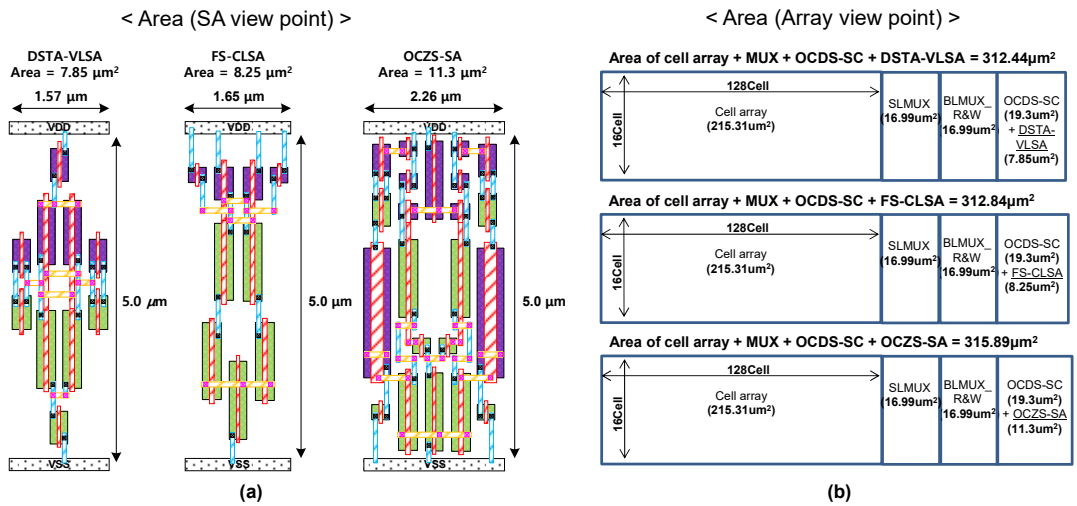

Figure 11. (**a**) Simplified layouts of DSTA-VLSA, FS-CLSA, and OCZS-SA. (**b**) Estimated array architecture areas when DSTA-VLSA, FS-CLSA, and OCZS-SA are employed.

Figure 12 shows that the minimum I_{read} that satisfies a target $RAPY_{CELL}$ value of 6σ is reduced by 21–32% by sacrificing the improvement in $RAPY_{CELL}$. Figure 13 shows that the read energy in the SC and SA is accordingly reduced by approximately 13–16%.

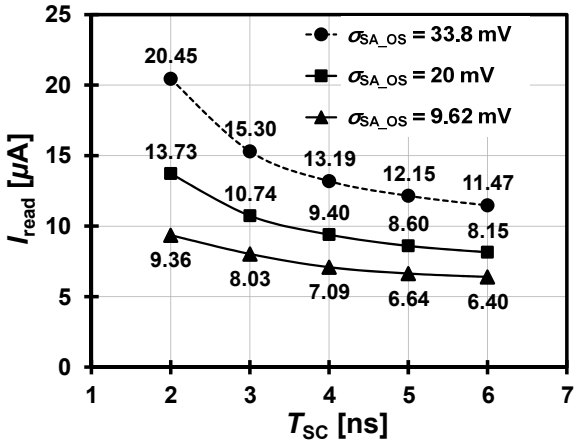

Figure 12. Minimum I_{read} of the OCDS-SC that satisfies a target $RAPY_{CELL}$ of 6σ according to T_{SC} at σ_{SA_OS} values of 33.8 mV, 20 mV, and 9.62 mV.

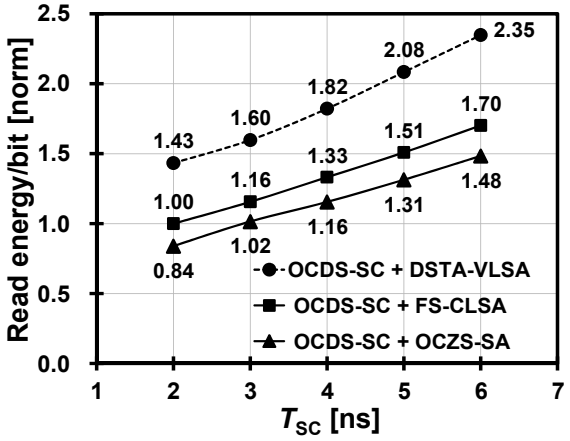

Figure 13. Normalized read energy per bit according to T_{SC} in cases of OCDS-SC + DSTA-VLSA, OCDS-SC + FS-CLSA, and OCDS-SC + OCZS-SA.

5. Conclusions

The conventional latch-type SAs cannot be applied to the OCDS-SC due to the capacitive-coupling and sensing-dead-zone problems. In this paper, we have proposed the OCZS-SA, which offers two major advantages: offset voltage cancellation and zero sensing dead zone. The simulation results prove that the OCZS-SA can achieve a 2.1 times smaller σ_{SA_OS} value of 9.62 mV without any sensing dead zone at the cost of an increased area overhead of 1.0% for a subarray size of 128 × 16. Furthermore, a 13–16% read-energy saving is achieved due to the 21–32% reduction in I_{read}. Thus, the OCZS-SA can be a compelling candidate for the OCDS-SC in deep submicrometer resistive NVMs.

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Conflicts of Interest: The author declares no conflict of interest.

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