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Mismatch Insensitive Voltage Level Shifter Based on Two Feedback Loops

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Abstract: This paper presents a voltage level shifter (VLS) based on two feedback loops. The complementary feedback signals in the high voltage domain are re-used to assist voltage conversion and the complementary phase in the low voltage domain is not required. Unlike the conventional VLS, which depends on the pull-up network and pull-down network to achieve level shift, the transitions of both high-to-low and low-to-high of the proposed VLS are undertaken by two different feedback loops, respectively. Implemented in a standard 180 nm CMOS process, post-layout Monte Carlo (MC) simulations from 4000 points under mismatch variation show that the dynamic power (DP) and the propagation delay (PD) of the proposed VLS are 105.3 nW and 2.0 ns, respectively, at an input voltage $V_{IN} = 0.4$ V with input frequency $f_{in} = 0.1$ MHz. Meanwhile, the excellent normalized standard deviation of DP and PD is obtained with the proposed scheme. The temperature range for normal operation is from -20 °C to 85 °C.

Keywords: level shifter; propagation delay; current mirror; high-to-low transition; low-to-high transition; pull-up network; pull-down network

1. Introduction

With the development of integration technology, aggressive supply voltage (V_{DD}) scaling is one of the main streams to reduce dynamic power consumption, short-circuit power dissipation, and leakage current for digital circuits and systems. However, for RF and analog circuit, a low voltage supply may deteriorate their performance, such as the bandwidth, the intrinsic gain, and linearity [1]. In order to obtain a satisfying tradeoff, the multi-supply voltage domain (MSVD) technique [2,3] is becoming a popular method in today's system-on-chip (SoC), as shown in Figure 1. For MSVD systems, VLSs are indispensable and employed to convert the logic level in a low supply voltage (V_{DDL}) to the logical level in a high supply voltage (V_{DDH}), as shown in Figure 1.

Conventional voltage level shifters (VLSs) can be categorized into two main types: the differential cascade voltage switch (DCVS)-based architecture [4–7] and the current mirror (CM)-based architecture [3,8–14], as shown in Figure 2. For the DCVS-based architecture, indicated in Figure 2a, a cross-coupled pair constituting by MP1 and MP2 as a pull-up network enables the nodes Q1 and Q2 to switch faster. Thus, the standby power is close to zero owing to the complementary pull-up and pull-down network. However, the major drawback is the strong contention between the two networks during the switching period. When the input voltage V_{IN} and V_{DDL} reduces to less than the threshold voltage of transistors, the strength of the pull-up network remains unchanged, while the strength of the pull-down network constituted by MN1 and MN2 is aggressively declined owing to the reduction of the voltage difference between the gate and the source of the pull-down network. Although the

strength of the pull-down network can be enhanced by upsizing the pull-down transistors (MN1 and MN2), it will deteriorate the propagation delay (PD) and dynamic power (DP) as the sizing ratio can be extremely large [8,9]. For the CM-based architecture, as shown in Figure 2b, the cross-coupled pair is replaced by a basic current mirror, thus the strength of the pull-up network is weakened for wide range voltage conversion and lower contention between pull-up and pull-down networks is obtained. However, the major drawback of the CM-based architecture is the large static current flowing through MP1 and MN1.

Figure 1. Multi-supply voltage domain (MSVD) design for system-on-chip (SoC) [2,3]. VLS, voltage level shifter.

Figure 2. The main two types of the level shifters: (a) differential cascade voltage switch (DCVS)-based level shifter; (b) current mirror (CM)-based level shifter.

Both of the above architectures achieve the voltage shift based on the strength between the pull-up network and pull-down network. Thus, the complementary phase of V_{IN} in the low voltage domain is inevitable. In this paper, a novel VLS without the complementary phase in the low voltage domain is proposed. The conversion of the logic level from the low voltage domain to the high voltage domain is achieved by two feedback loops.

The rest of the paper is organized as follows. Section 2 introduces the proposed circuit scheme, including the detailed operations. Section 3 presents the post-layout simulation results and comparison with prior arts. Finally, the conclusion is drawn in Section 4.

2. Proposed Circuit Scheme

The complementary phase in high voltage domain is re-used to assist the voltage level shift in the low voltage domain. As shown in Figure 3a, two complementary feedback signals from the high voltage domain are injected into the low voltage domain. The corresponding transistor-level scheme is presented in Figure 3b, where V_{IN} controls the gate of MN1, which can pull down the node A when V_{IN} is high. MP5 acts as a current-limit resistor. MP2, MN2, MP3, and MN3 form two cascaded inverters, INV1 and INV2. C_L represents the load capacitor. Thus, the complementary phases are generated in the high voltage domain, which are re-used to assist the operation of VLS. Owing to the feedback signal from node C, MP1, INV1, and INV2 are connected like a three-stage ring oscillator. MP4 and INV1 form a positive feedback in order to achieve the high-to-low transition.

Figure 3. Proposed VLS: (a) concept of the proposed solution; (b) detailed transistor-level scheme of the proposed solution.

The detailed operations for the low-to-high transition and the high-to-low transition are presented in Figure 4a,b, respectively. As shown in Figure 4a, for the initial moment, the voltage of the node A is high, which is larger than the switching threshold of INV1. The voltage of node B is low in the high voltage domain. When V_{IN} is low-to-high, MN1 is on and the parasitic capacitors in the node A are discharged at this moment. As the MOS MP4 is small enough, finally, the node A is pulled down to GND. The voltage of node B is converted to high in the high voltage domain. Thus, the high level in the low voltage domain is shifted into the high voltage domain at node B.

As for the high-to-low transition, shown in Figure 4b, at the initial moment, the voltage of node A is low and the voltage of the node B is high. When V_{IN} is high-to-low, MN1 and MP1 are off. Node A starts to rise up through the leakage path V_{DDH} –MP5–MP1–MN1–GND. Once the voltage of node A reaches the switching threshold of INV1, MN2 is on. The voltage of node B will be pulled down to GND by MN2 in the high voltage domain and the voltage of node A will be aggressively lifted up to V_{DDH} by the positive feedback loop. This positive feedback accelerates the voltage setting of node A. Thus, the low level in the low voltage domain is shifted into the high voltage domain at node B.

On the basis of the above analysis, it is clear that the proposed VLS conducts the level shift by the assistance of the feedback signals from the high voltage domain. The complementary phases in the

high voltage domain are re-used to achieve the voltage shift. The whole process does not depend on any PMOS-only or NMOS-only networks and the conversion of the logic level from the low voltage domain to the high voltage domain is achieved by two feedback loops.

Figure 4. Operations of the proposed VLS: (a) the level shift process of low-to-high; (b) the level shift process of high-to-low.

Properly designing the size for MN1, MP1, MP4, and MP5 can guarantee the normal operation of the proposed VLS at five process corners (TT, SS, FF, SNFP, and FNFP) under $-20\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$. In order to ensure the normal operation under $V_{DDL} = 0.3\text{ V}$, the medium threshold voltage transistor is chosen as MN1 to enhance the current injection efficiency at low input voltage. The size of the transistors used for the proposed VLS is listed in Table 1.

Table 1. Transistor dimensions of the proposed voltage level shifter (VLS).

Transistor	Width (μm)	Length (μm)	Transistor	Width (μm)	Length (μm)
MN1	12	0.3	MP2	0.5	0.18
MN2	0.25	0.18	MP3	1	0.18
MN3	0.5	0.18	MP4	0.55	10
MP1	5.5	0.18	MP5	0.55	10

3. Simulation Results

In order to verify the performance of the proposed VLS, it was implemented in a standard 180 nm CMOS process and the physical layout is shown in Figure 5, where each transistor is enclosed by guard rings. It consumes an area of $25\text{ }\mu\text{m} \times 15\text{ }\mu\text{m}$. Owing to the introduction of guard rings, the layout of

the proposed VLS consumes more area than in [4,11,14], but it features more reliability. Meanwhile, as the area of a system is usually dominated by other core circuits, the area increase of the proposed VLS is almost negligible.

The Cadence Spectre simulator is used for the post-layout verification. The parasitic parameters are extracted by Calibre xRC (Mentor Graphics Corporation, Wilsonville, AL, USA). The extraction netlist includes the parasitic capacitors, the parasitic resistors, and the parasitic diodes in the physical layout. It is noteworthy that the loading condition is assumed as an inverter at the output.

Figure 5. Layout of the proposed VLS.

The simulated performance of the proposed VLS in terms of static power consumption, DP, and PD is presented. As shown in Figure 6, the static power consumption is illustrated including five process corners. The static power consumption is less than 1 nW at the TT corner under 27 °C when $V_{DDL} = 0$ V and the process corner FF features the highest static power, as shown in Figure 6a. Figure 6b presents the static power consumption when $V_{DDL} = 0.3$ V. Comparing Figure 6a with Figure 6b, it is obvious that the static power consumption increases with the increase of temperature and the static power under $V_{DDL} = 0.3$ V is much larger. This is because the static power is contributed by the leakage current. With the increase of temperature, the threshold of transistors becomes smaller, thus larger static power is observed under both $V_{DDL} = 0$ V and $V_{DDL} = 0.3$ V. The reason larger static power is observed under $V_{DDL} = 0.3$ V is that resistance between V_{DDH} and ground becomes smaller when MN1 and MP1 are on. Figure 6c shows the static power under different V_{DDL} at 27 °C. Once MN1 and MP1 are on, larger V_{DDL} hardly influences the static power.

Figure 7 shows the simulated transient behavior of proposed VLS under different V_{DDH} with $f_{in} = 0.1$ MHz. As high V_{DDH} means large power consumption and low V_{DDH} may cause performance deterioration, $V_{DDH} = 1$ V is chosen as the typical operation mode, as indicated in Figure 1. As shown in Figure 7a, for the rise transient, more time is required in order to reach higher V_{DDH} . For the fall transient, a large delay occurs, as shown in Figure 7b. This is because the charging current contributed by the leakage current at node A is much smaller when both MN1 and MP1 are off, as indicated in Figure 4b. This can be mitigated by higher V_{DDH} . However, when the input frequency is lower than 0.1 MHz, such as the audio application, the fall delay causes little damage to the input signal. When the input frequency is much higher than 0.1 MHz, such as 10 MHz, the proposed scheme fails. For the case of 1 MHz, the proposed scheme works well for most cases except for the change in duty cycle. This issue can be overcome with the duty cycle calibration circuit if 50% duty cycle is required.

Figure 6. Post-layout simulated static power versus temperature and V_{DDL} under five corners: (a) static power versus temperature at $V_{DDL} = 0$ V; (b) static power versus temperature at $V_{DDL} = 0.3$ V; (c) static power versus V_{DDL} at 27 °C.

Figure 7. Simulated transient behavior of the proposed VLS under different V_{DDH} with $f_{in} = 0.1$ MHz, $V_{DDL} = 0.3$ V at 27 °C: (a) rise transient behavior under different V_{DDH} ; (b) fall transient behavior under different V_{DDH} .

Figure 8 illustrates the performance of the proposed VLS versus V_{DDL} in terms of DP and PD, including five process corners. Figure 8a shows that the process corners have a direct influence on

DP, while V_{DDL} has no effect on DP as DP is a threshold-dependent performance metric. Figure 8b indicates that both V_{DDL} and process corners have little influence on PD when V_{DDL} is above 0.4 V.

Figure 8. Post-layout simulated performance of the proposed VLS versus V_{DDL} under five process corners: (a) dynamic power (DP) versus V_{DDL} with $f_{in} = 0.1$ MHz at 27 °C; (b) propagation delay (PD) versus V_{DDL} with $f_{in} = 0.1$ MHz at 27 °C.

Figure 9 shows the performance of the proposed VLS versus temperature in terms of the DP and PD, including five process corners. Figure 9a indicates that DP is linearly proportional to the increase of temperature over the range from -20 °C to 85 °C. PD declines in inverse proportion to temperature, as shown in Figure 9b.

Figure 9. Post-layout simulated performance of the proposed VLS versus temperature under five process corners: (a) DP versus temperature at $f_{in} = 0.1$ MHz, $V_{DDL} = 0.3$ V; (b) PD versus temperature at $f_{in} = 0.1$ MHz, $V_{DDL} = 0.3$ V.

In order to verify the robustness of the proposed VLS to mismatch, Monte Carlo (MC) simulation is conducted. In the setup form of MC simulation, the statistical variation includes three choices: process, mismatch, and both. The term ‘process’ means that only the process variation is considered. The corresponding statistical sigma $\sigma_{process}$ is 1/3. The term ‘mismatch’ means that only the mismatch variation is considered. The corresponding statistical sigma $\sigma_{mismatch}$ is 1/1, which indicates the mismatch variation follows the standard normal distribution. The term ‘both’ indicates the above two variations are considered in the MC simulation. In order to evaluate the performance of the proposed VLS, the MC simulations were conducted under ‘mismatch’.

Figure 10 shows the post-layout simulated MC results for 4000 points to evaluate DP of the proposed VLS under different V_{DDL} with mismatch variation. The simulation is conducted under

$f_{in} = 0.1$ MHz and 1 MHz, respectively. As shown in Figure 10a, the mean DP ($\mu_{DP_0.1\text{ MHz}}$) and the standard deviation ($\sigma_{DP_0.1\text{ MHz}}$) for 0.1 MHz at $V_{DDL} = 0.3$ V are 104 nW and 2.97 nW, respectively. The results for $\mu_{DP_1\text{ MHz}}$ and $\sigma_{DP_1\text{ MHz}}$ when f_{in} is 1 MHz are shown in Figure 10b, which are 565 nW and 29.15 nW, respectively, although five points fail in the simulation owing to the larger fall delay. Figure 10c shows the results for $\mu_{DP_0.1\text{ MHz}}$, $\sigma_{DP_0.1\text{ MHz}}$, $\mu_{DP_1\text{ MHz}}$, and $\sigma_{DP_1\text{ MHz}}$ under different V_{DDL} . It indicates that V_{DDL} contributes no effects on $\mu_{DP_0.1\text{ MHz}}$, $\sigma_{DP_0.1\text{ MHz}}$, $\mu_{DP_1\text{ MHz}}$, and $\sigma_{DP_1\text{ MHz}}$.

Figure 10. Post-layout simulated Monte Carlo (MC) results for DP of the proposed VLS with mismatch variation: (a) $V_{DDL} = 0.3$ V, $f_{in} = 0.1$ MHz; (b) $V_{DDL} = 0.3$ V, $f_{in} = 1$ MHz; (c) results for $\mu_{DP_0.1\text{ MHz}}$, $\sigma_{DP_0.1\text{ MHz}}$, $\mu_{DP_1\text{ MHz}}$, and $\sigma_{DP_1\text{ MHz}}$ under different V_{DDL} .

Figure 11 presents the post-layout simulated MC results for 4000 points to evaluate PD of the proposed VLS under different V_{DDL} and mismatch variation. The simulation is conducted under $f_{in} = 0.1$ MHz and 1 MHz. As shown in Figure 11a, the mean propagation delay ($\mu_{PD_0.1\text{ MHz}}$) and the standard deviation ($\sigma_{PD_0.1\text{ MHz}}$) for 0.1 MHz and $V_{DDL} = 0.3$ V are 5.90 ns and 0.166 ns, respectively. When f_{in} is 1 MHz and V_{DDL} is 0.3 V, $\mu_{PD_1\text{ MHz}}$ and $\sigma_{PD_1\text{ MHz}}$ are almost equal to the case of $f_{in} = 0.1$ MHz, although five points fail during the MC simulation. This is because the delay is decided by the capacitance and resistance of nodes in the circuit, thus both the rise delay and the fall delay are almost irrelevant to the input frequency. Figure 10b shows the change of $\mu_{PD_0.1\text{ MHz}}$ and $\sigma_{PD_0.1\text{ MHz}}$ under different V_{DDL} . Because higher V_{DDL} indicates that the discharging time of node is faster, the rise delay becomes smaller with the increase in V_{DDL} .

Figure 11. Post-layout simulated MC results for DP of the proposed VLS with mismatch variation: (a) $V_{DDL} = 0.3$ V, $f_{in} = 0.1$ MHz and 1 MHz; (b) results for $\mu_{DP_0.1}$ MHz and $\sigma_{DP_0.1}$ MHz under different V_{DDL} .

Table 2 tabulates the performance comparison of the proposed VLS with the prior designs. The following figure of merit termed power-delay product (PDP) is used to evaluating the performance of all works proposed in literature, as shown in (1):

$$PDP = DP \times PD \quad (1)$$

As indicated in Table 2, the performance comparison is presented. Because the area of the proposed VLS is larger than other works, it achieves the minimal normalized standard deviation (σ/μ) of DP and PD. The corresponding σ_{DP}/μ_{DP} and σ_{PD}/μ_{PD} for $f_{in} = 0.1$ MHz and $V_{DDL} = 0.4$ V are 0.02 and 0.028, respectively. Compared with [3], when V_{DDL} is 0.4 MHz and f_{in} is 1 MHz, although DP of the proposed scheme is larger, a competitive PDP is obtained by excellent PD. As there is no circuit powered by V_{DDL} in the proposed VLS, DP is almost irrelevant to V_{DDL} and is mainly decided by f_{in} and V_{DDH} . Meanwhile, because the delay is mainly contributed by the capacitance and the resistance of corresponding nodes, PD is almost irrelevant to f_{in} .

Table 2. Performance comparison. DP, dynamic power; PD, propagation delay; DCVS, differential cascade voltage switch; CM, current mirror; PDP, power-delay product.

Ref.	Tech. (nm)	Type	Load	V_{DDL} (V)	V_{DDH} (V)	f_{in} (MHz)	DP (nW)	σ_{DP}/μ_{DP}	PD (ns)	σ_{PD}/μ_{PD}	PDP (nW•ns)	Area (μm^2)
[4] ¹	180	DCVS	INV	0.45	1.8	1	175	0.24	12	0.503	2100	120.90
[7] ¹	180	DCVS	INV	0.4	1.8	1	123.1	0.27	23.69	0.25	2916	63.00
[3] ¹	90	CM	100 fF	0.4	1	1	218.3	0.42	28.83	0.24	6293	81.40
[8] ²	180	CM	10 fF	0.3	1.2	1	250	—	7.5	0.39	1875	7.45
[11] ²	180	CM	—	0.4	1.8	0.1	10	—	167	—	1670	229.50
[13] ²	65	CM	—	0.4	1.2	0.01	631.4	—	29.59	—	18,683	90.00
[14] ^{1,3}	180	CM	INV	0.4	1.8	1	76.34	0.14	6.1	0.16	465.7	35.25
This work ^{1,3}	180	Two feed-back loops	INV	0.3	1	0.1	104.9	0.02	5.90	0.028	618.91	375.00
				0.4			105.3		2.00	0.028	210.60	
				0.5			105.4		1.65	0.034	173.91	
				0.3			565.0		5.90	0.028	3333.50	
				0.4			567.1		2.00	0.028	1134.20	
				0.5	1	1	568.1	0.052	1.65	0.034	937.37	

¹ Simulation results. ² Measurement results. ³ Only mismatch is considered.

4. Conclusions

A VLS based on two feedback loops is reported. The complementary phase in the high voltage domain is re-used to assist the voltage conversion and no complementary phase is required in the low voltage domain. The results indicate that considerably lower PDP and minimum PD can be obtained

with the proposed VLS. It features potential application in audio application for its excellent PDP. It can ensure normal operation from $-20\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$ under five different corners at $f_{in} = 0.1\text{ MHz}$.

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