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A Ku-Band GaAs Multifunction Transmitter and Receiver Chipset

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Abstract: This paper presents a Ku-band monolithic multifunction transmitter and receiver chipset fabricated in 0.25-μm GaAs pseudomorphic high-electron mobility transistor technology. The chipset achieves a high level of integration, including a 4-bit 360° digital phase shifter, 5-bit 15.5-dB digital attenuator, amplifier and 9-bit digital serial-to-parallel converter for digital circuit control. Since the multifunction chipset includes a medium power amplifier and a low-noise amplifier, it features high P1dB and low noise figures over the full Ku-band frequencies. The multifunction transmitter shows a peak gain of 16.5 dB with output P1dB of 19.2 dBm at 15 GHz. The multifunction receiver shows a peak gain of 17.3 dB with noise figure of 2.5 dB at 15 GHz. The attenuation range is 15.5 dB with a step of 0.5 dB and the phase shift range is 360° with a step of 22.5°. Each chip area of the transmitter and receiver is 4.2×2.8 mm^2.

Keywords: multifunction; transmitter; receiver; attenuator; phase shifter; medium power amplifier; low-noise amplifier; serial-to-parallel converter

1. Introduction

Demand for phased-array systems has continued to increase for satellite/military communications and radars [1]. In the past, multiple individual modules were assembled to implement each channel element in the phased array, which increases the size, weight, complexity and cost of the system [2]. However, a multifunction chip integrates most of the functionalities required for the array element in a single chip, including the phase and amplitude control, signal amplification and digital control. This significantly reduces the system complexity and cost [3]. In particular, as the array size increases to a large scale, the benefit of the multifunction chip becomes more prominent. For this purpose, the chip should retain high integration level and compact size.

In recent years, several multifunction chips have been reported in GaAs or silicon technologies [1,4–13]. Silicon-based multifunction chips are favorable for their easy integration with digital circuits and low cost in the case of mass chip production [4]. However, GaAs technologies offer superior noise figures and output power over silicon technologies. In addition, digital circuits can be integrated even in GaAs technologies using a combination of enhancement-mode (E-mode) and depletion-mode (D-mode) transistors [14]. Therefore, it is more attractive to use GaAs technology for broadband multifunction chips with high gain, high output power and low noise figures. There are several articles which have reported on GaAs multifunction chips [1,8–13]. Nevertheless, many chips

integrate only some, and not all, of the essential circuit blocks required for phased arrays, including a phase shifter, attenuator, amplifier and digital control circuit [1,8,9]. Other reports show narrowband operation [8,10] or relatively limited output power and high noise figures [11,13].

In this paper, a GaAs multifunction transmitter and receiver chipset operating over the full Ku-band (12–18 GHz) frequency is presented. A 4-bit digital phase shifter, 5-bit digital attenuator and 9-bit serial-to-parallel converter (SPC) are all integrated with a medium power amplifier (MPA) or a low-noise amplifier (LNA). This high integration level enables high output power and low noise figure and thus makes this chipset suitable for a large-scale phased-array system. This paper is organized as follows. In Section 2, the architecture of the multifunction transmitter and receiver are described. The design and measurement of each circuit building block are presented in Section 3. In Section 4, the measurement of the multifunction transmitter and receiver chipset is presented. The conclusion is presented in Section 5.

2. Ku-Band Multifunction Chip Architecture

The Ku-band multifunction chipset was designed using a commercial 0.25-μm GaAs pseudomorphic high-electron mobility transistor (pHEMT) technology. The process offers a 0.25-μm E-mode HEMT with f_T = 75 GHz and a 0.5-μm D-mode HEMT with f_T = 33 GHz. It also provides two metal layers, two types of capacitor (metal-insulator-metal capacitor and stack capacitor), three types of resistor (thin-film resistor, mesa resistor and epi resistor) and two types of inductor (spiral inductor and square inductor).

Figure 1 shows block diagrams of the Ku-band multifunction transmitter (a) and receiver (b). The multifunction transmitter consists of a 5-bit attenuator, 4-bit digital phase shifter, MPA and 9-bit SPC. The attenuator offers a total of 15.5 dB attenuation with a step of 0.5 dB. The phase shifter fulfills a 360° phase shift with a step of 22.5°. Both attenuator and phase shifter are digitally controlled by the SPC. The SPC converts a 9-bit serial digital code into a parallel code, which is loaded onto the attenuator and phase shifter for setting the desired attenuation and phase shift. This reduces the number of bonding pads for digital control. The attenuator is placed ahead of the phase shifter for broadband input matching. The MPA is placed in the final stage to enhance the output power and linearity of the transmitter.

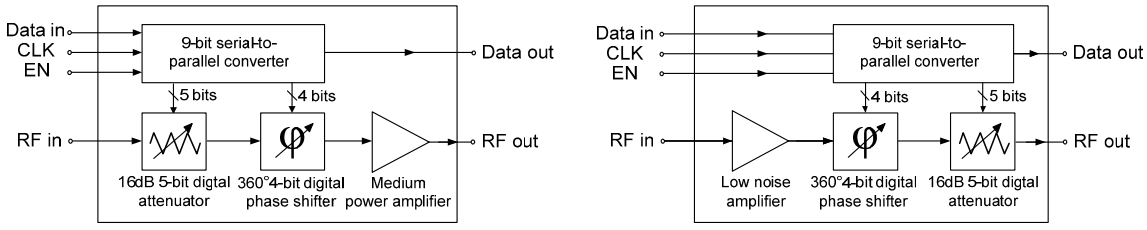


Figure 1. Block diagram of (**a**) the Ku-band multifunction transmitter and (**b**) receiver.

The multifunction receiver is composed of an LNA, 4-bit digital phase shifter, 5-bit digital attenuator and 9-bit SPC. Similar to the transmitter, 15.5-dB attenuation and 360° phase shift are implemented in the receiver and are controlled by the SPC. The LNA is placed at the input stage for providing high gain and low noise figures.

3. Circuit Blocks of the Ku-Band Multifunction Chipset

3.1. 5-Bit Digital Attenuator

The attenuator is designed in a passive type for zero DC power consumption. This is beneficial in allowing the multifunction chip to be used in a large-scale phased array system. To achieve a

15.5-dB attenuation range, five-unit attenuator cells with binary-weighted attenuation are connected in cascade. The least significant bit (LSB) and the most significant bit (MSB) are 0.5 dB and 8.0 dB, respectively. In Figure 2, the topologies of the unit attenuator cells are presented. For 0.5-dB and 1.0-dB attenuation, a switched-T structure shown in Figure 2a is adopted for low insertion loss and small chip area. A 2 × 50-µm D-mode HEMT with on-resistance of 12.2 Ω and off-capacitance of 27.3 fF is used for switching devices (M_s and M_p). As the attenuation increases, the conventional switched-T structure presents a larger phase imbalance between the reference and attenuation states. Therefore, a 2.0-dB attenuator cell is designed using the structure shown in Figure 2b. An additional capacitor, C_{P1}, compensates for the phase imbalance by adjusting the insertion phase in the attenuation state without degrading the insertion loss and matching performance in the reference state [15]. Finally, 4.0-dB and 8.0-dB attenuator cells are designed with the structure shown in Figure 2c, where a capacitor, C_{P2}, is connected in parallel with R_{P2}. This not only reduces the phase imbalance but also prevents the bandwidth reduction occurring in high attenuation cells [16–18].

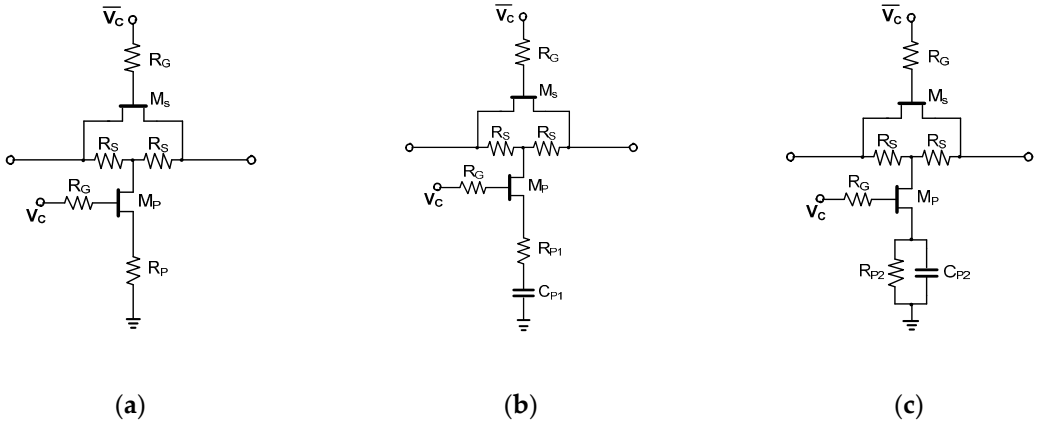


Figure 2. Topologies of the unit attenuator cells. (**a**) 0.5-dB and 1-dB attenuator cell, (**b**) 2-dB attenuator cell, (**c**) 4-dB and 8-dB attenuator cell.

Figure 3 shows a full schematic and micrograph of the 5-bit digital attenuator. The placement order of each unit attenuator cell is determined, such that the operation bandwidth is maximized. A shunt resistor (R_{11}) provides the attenuator with DC ground. The 5-bit digital attenuator occupies an area of 0.9 × 0.4 mm^2, excluding probing pads. The parameter value of each component is presented in Table 1.

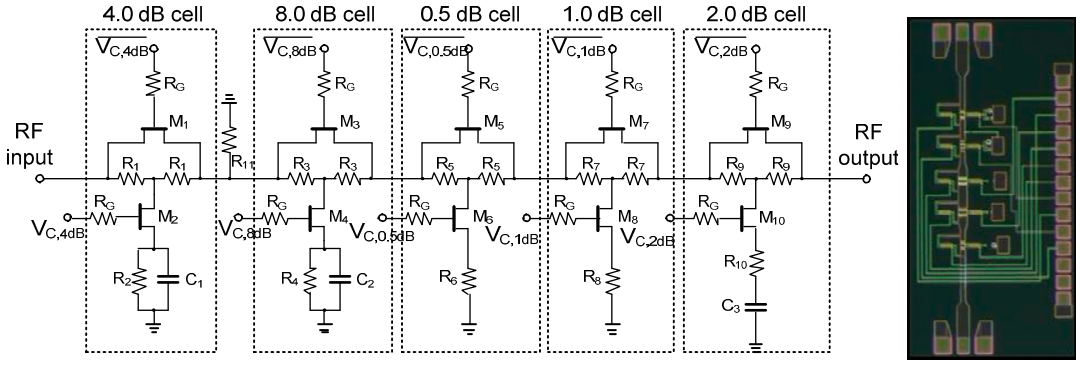


Figure 3. Schematic and chip micrograph of the 5-bit digital attenuator.

Table 1. Design parameters of the 5-bit digital attenuator.

Parameter	Design Value	Parameter	Design Value	Parameter	Design Value
M_1–M_{10}	2 × 50-μm	R_5	5.1 Ω	R_{10}	498.9 Ω
R_1	16.4 Ω	R_6	627.0 Ω	R_{11}, R_G	6.7 kΩ
R_2	102.3 Ω	R_7	7.6 Ω	C_1	65.3 fF
R_3	31.5 Ω	R_8	371.2 Ω	C_2	133.9 fF
R_4	96.9 Ω	R_9	18.4 Ω	C_3	122.8 fF

The measurement results of the 5-bit digital attenuator are shown in Figure 4. The insertion loss and matching performance in the reference state are depicted in Figure 4a. The insertion loss ranges from 4.9 to 6.6 dB over the entire Ku-band frequency. The input and output matching are below −14.2 and −23.8 dB, respectively. Figure 4b shows the measured insertion loss for all 32 attenuation states. It can be seen that the total attenuation of 13.8 to 15.5 dB is achieved with a step of 0.5 dB. Figure 4c shows the input and output matching performance for all 32 attenuation states, which are below −11.5 and −15.6 dB, respectively, in the entire Ku-band. The root mean square (RMS) attenuation and parasitic phase errors, shown in Figure 4d, are less than 1 dB and 2°, respectively.

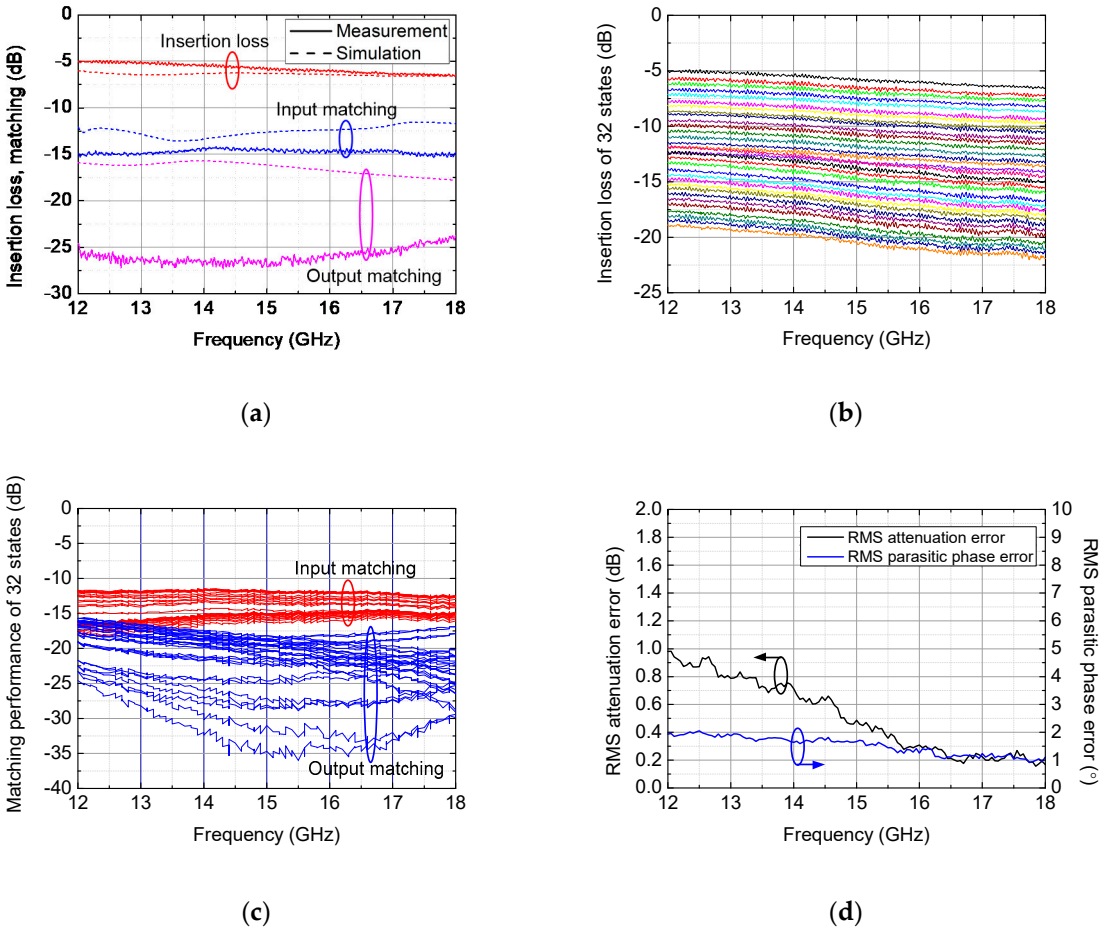


Figure 4. Measurement results of the 5-bit digital attenuator: (**a**) insertion loss and matching performance in the reference state, (**b**) insertion loss for all 32 attenuation states, (**c**) input and output matching for all 32 attenuation states, (**d**) root mean square (RMS) attenuation and parasitic phase errors.

3.2. 4-Bit Digital Phase Shifter

The phase shifter is designed with a passive switched topology to reduce the DC consumption and to facilitate the digital phase control. Four unit cells, each accomplishing phase shifts of 22.5°, 45°, 90° and 180°, are connected in cascade for a full 360° shift.

The 22.5°, 45° and 90° cells adopt a bridged-T structure, as shown in Figure 5a. In the reference state, the transistors, M_S and M_{P1}, are turned on while M_{P2} is turned off, simplifying to the equivalent circuit of Figure 5b. The off-capacitance of M_{P2} (C_{MP2}) resonates with parallel-connected L_P at the operation frequency, giving an open circuit. On the other hand, in the phase-shift state, M_S and M_{P1} are turned off while M_{P2} is turned on, as shown in Figure 5c. Therefore, the off-capacitance of M_{P1} (C_{MP1}) and L_S provide a designated phase shift. The component values are determined by the following equations [19].

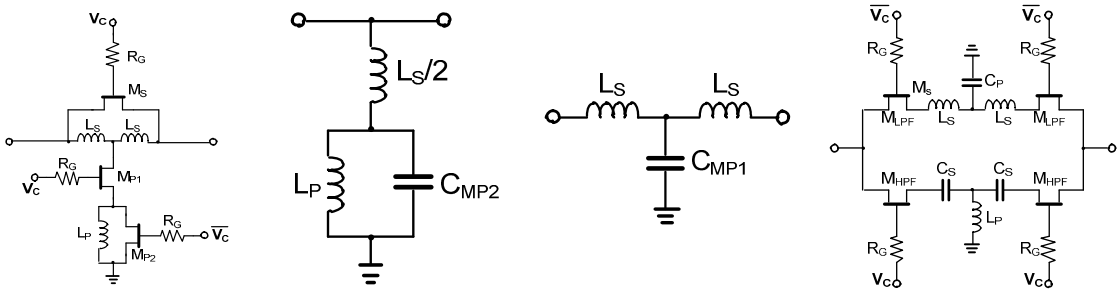
$$L_S = \frac{Z_0}{\omega} \tan\left(\frac{\Delta\phi}{2}\right) \tag{1}$$

$$L_P = \frac{1}{\omega^2 C_{MP2}} \tag{2}$$

$$C_{MP1} = \frac{\sin(\Delta\phi)}{\omega Z_0} \tag{3}$$

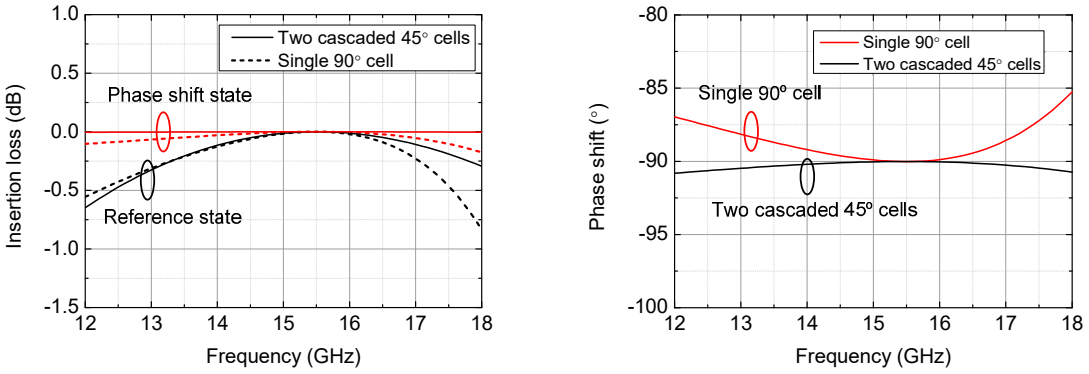
$$C_{MP2} = \frac{2L_S}{{Z_0}^2} \tag{4}$$

where $\Delta\phi$ is the designated phase shift, Z_0 is the characteristic impedance and ω is the operation frequency. It is noted that C_{MP1} and C_{MP2} become large as $\Delta\phi$ increases to 90°. The large off-capacitance requires a large-size transistor, which limits the operation bandwidth. Therefore, the 90° cell is implemented by connecting two 45° cells in cascade. In Figure 6a,b, the insertion loss and phase shift performance are compared, respectively, when a single 90° cell and two cascaded 45° cells are used. Obviously, the two cascaded 45° cells provide a wider bandwidth for 90° phase shift.



(**a**) (**b**) (**c**) (**d**)

Figure 5. (**a**) Bridged-T structure for 22.5°, 45° and 90° unit cells, (**b**) equivalent circuit in the reference state, (**c**) equivalent circuit in the phase shift state, (**d**) high-pass-filter/low-pass-filter structure for 180° unit cell.



(**a**) (**b**)

Figure 6. Performance comparison of two structures implementing 90° phase shift: (**a**) insertion loss, (**b**) phase shift.

A 180° cell is designed using the high-pass filter (HPF)/low-pass filter (LPF) structure shown in Figure 5d. The values of inductance and capacitance are calculated by the following equations [20].

$$L_S = \frac{Z_0 \Delta \tan\left|\frac{\Delta\phi}{2}\right|}{\omega} \tag{5}$$

$$L_P = \frac{Z_0}{\omega \Delta \sin|\Delta\phi|} \tag{6}$$

$$C_S = \frac{1}{\omega \Delta Z_0 \cdot \tan\left|\frac{\Delta\phi}{2}\right|} \tag{7}$$

$$C_P = \frac{\sin|\Delta\phi|}{\omega \Delta Z_0} \tag{8}$$

Figure 7 shows a complete schematic and micrograph of the 4-bit digital phase shifter. The placement order of each unit phase shift cell is optimized for a wide bandwidth and low insertion loss. The 4-bit digital phase shifter test cut occupies an area of 2.6 × 1.1 mm^2, excluding probing pads. The parameter value of each component is presented in Table 2.

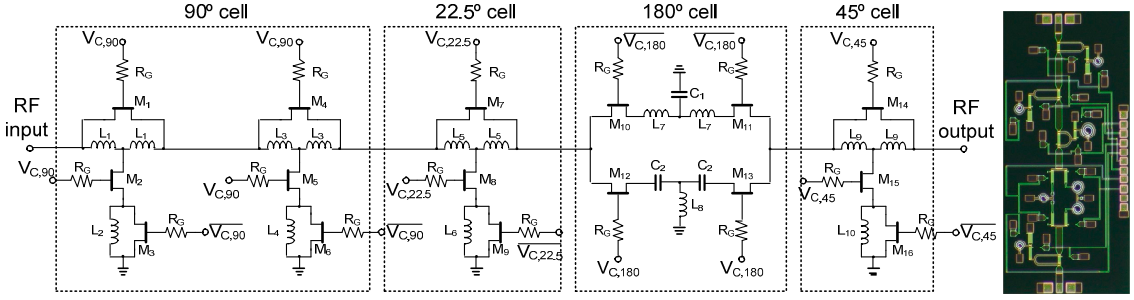


Figure 7. Schematic and chip micrograph of the 4-bit digital phase shifter.

Table 2. Design parameters of the 4-bit digital phase shifter.

Parameter	Design Value	Parameter	Design Value
M_1, M_4, M_8, M_9, M_{14}	5 × 75-μm	L_1, L_3, L_9	212.7 pH
M_2, M_5, M_7, M_{10}, M_{11}, M_{12}, M_{13}, M_{15}	5 × 125-μm	L_2, L_4, L_{10}	619.7 pH
M_3, M_6, M_{16}	9 × 100-μm	L_5	102.1 pH
R_G	2.1 kΩ	L_6	1.3 nH
C_1, C_2	205.4 fF	L_7, L_8	513.4 pH

The measurement results of the 4-bit digital phase shifter are shown in Figure 8. The insertion loss and matching performance in the reference state are depicted in Figure 8a. The insertion loss ranges from 2.5 to 4.5 dB over the entire Ku-band frequency. The input and output matching are below −10.7 and −11.2 dB, respectively. Figure 8b shows the measured phase shift of all 16 states, presenting a full 360° shift in the Ku-band. Figure 8c shows the input and output matching performance for all 16 phase shift states, which are below −5 dB from 13 to 20 GHz. The RMS phase and parasitic amplitude errors, shown in Figure 8d, are less than 6.3° and 2.1 dB, respectively.

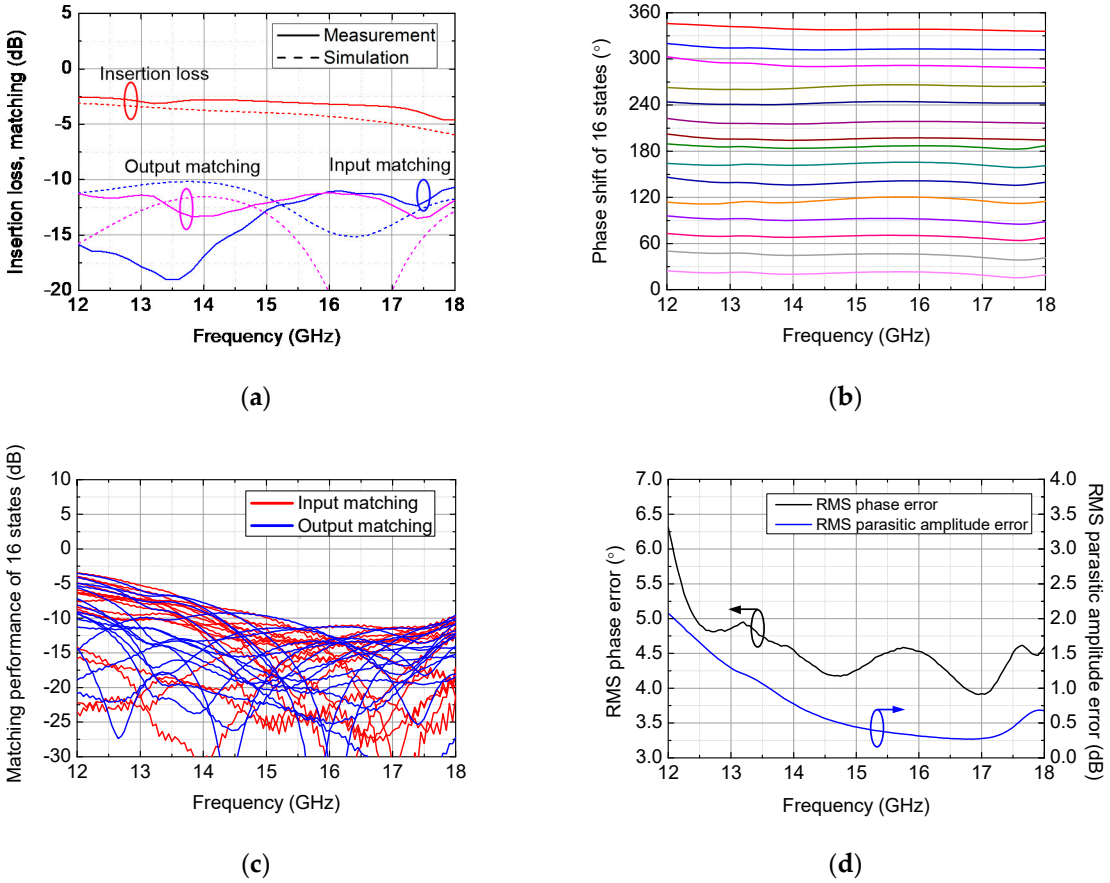


Figure 8. Measurement results of the 4-bit digital phase shifter: (**a**) insertion loss and matching performance in the reference state, (**b**) phase shift for all 16 states, (**c**) input and output matching for all 16 states, (**d**) RMS phase and parasitic amplitude errors.

3.3. Serial-to-Parallel Converter (SPC)

As the number of digital control bits increases, the interconnection between the multifunction chip and the digital control unit becomes demanding, especially in a large-scale phased-array system. To alleviate the interconnection complexity, an SPC is integrated into the multifunction chip, which enables serial data input for controlling the 5-bit attenuator and 4-bit phase shifter.

Figure 9 shows a block diagram and micrograph of the 9-bit SPC. It consists of a 9-bit shift register, nine latches, three input voltage transformers (IVT) for serial data input (D_{in}), clock (CLK), enable (EN), nine output voltage transformers (OVT) for control of the attenuator and phase shifter and one OVT for serial data output (D_{out}).

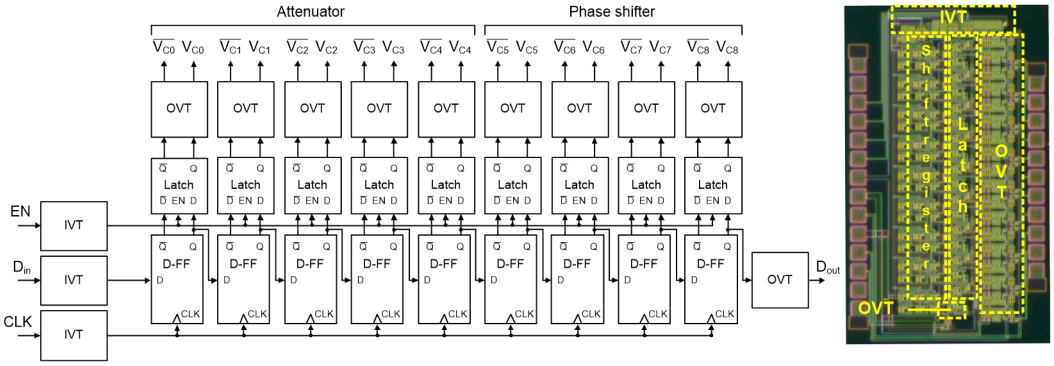
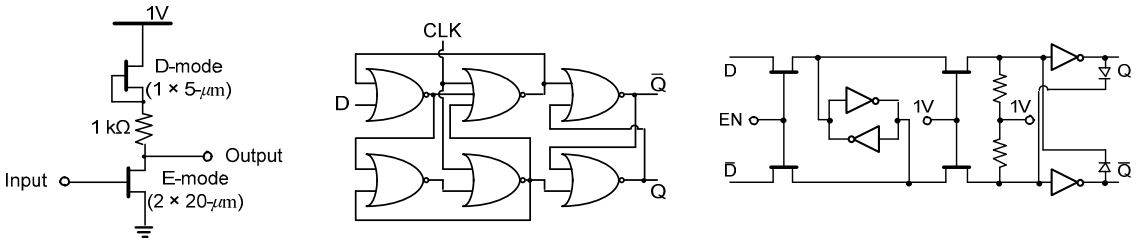


Figure 9. Block diagram and chip micrograph of the 9-bit SPC.

A simple direct-coupled FET logic (DCFL) is adopted for an inverter due to the small chip area and low DC consumption [21]. As shown in Figure 10a, the inverter consists of an E-mode switching HEMT and a D-mode load HEMT. By adding a 1-kΩ resistor in series with the load transistor, static power consumption can be reduced while sacrificing the switching speed. The static DC current is 0.65 mA. The shift register is based on a conventional D-flip flop, as shown in Figure 10b. Figure 10c shows the schematic diagram of the latch. A diode-coupled feedback is added to the output of the latch. This compensates for the reduced voltage swing caused by the finite on-resistance of the E-mode HEMT of the inverter logic.



(**a**) (**b**) (**c**)

Figure 10. Schematics of (**a**) the inverter, (**b**) shift register, (**c**) latch.

The input signals (D_{in}, CLK, EN) follow the Transistor-transistor logic (TTL), which swings from 0 to 5 V. To transform the TTL level to the DCFL inverter level (0 to 1 V), the IVT is designed as shown in Figure 11a. Similarly, two OVTs are designed for two different purposes. The first OVT, shown in Figure 11b, transforms the DCFL level to the control level of the digital attenuator and phase shifter (−5 to 0 V). The second OVT shown in Figure 11c transforms the DCFL level back to the TTL level. The SPC test cut shown in Figure 9 occupies an area of 1.8 × 0.8 mm^2, excluding probing pads, and consumes DC power of 350 to 415 mW depending on the input data.

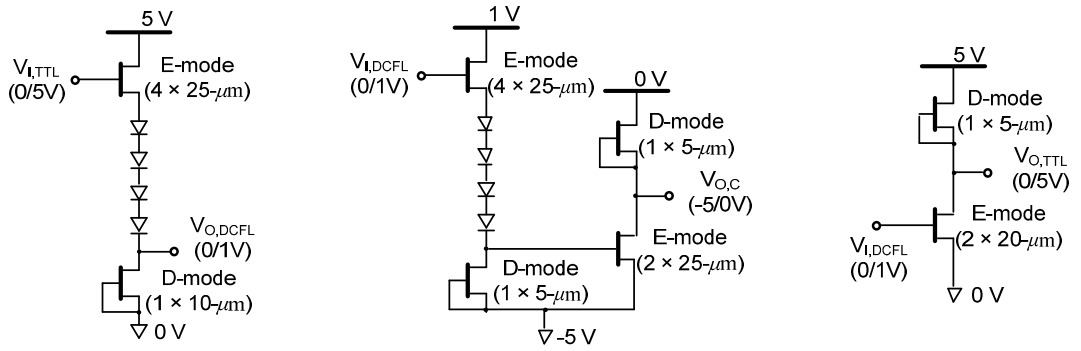


Figure 11. Schematics of (**a**) input voltage transformers (IVT), (**b**) output voltage transformers (OVT) for controlling the digital attenuator and phase shifter, (**c**) OVT for D_{out}.

3.4. Medium Power Amplifier (MPA)

A broadband MPA with high gain and output power is designed using E-mode HEMT to compensate for loss from the digital attenuator and digital phase shifter. Figure 12 illustrates a schematic of the MPA.

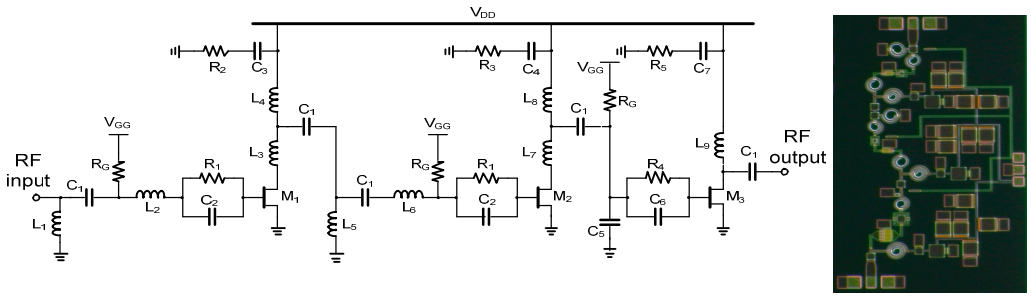
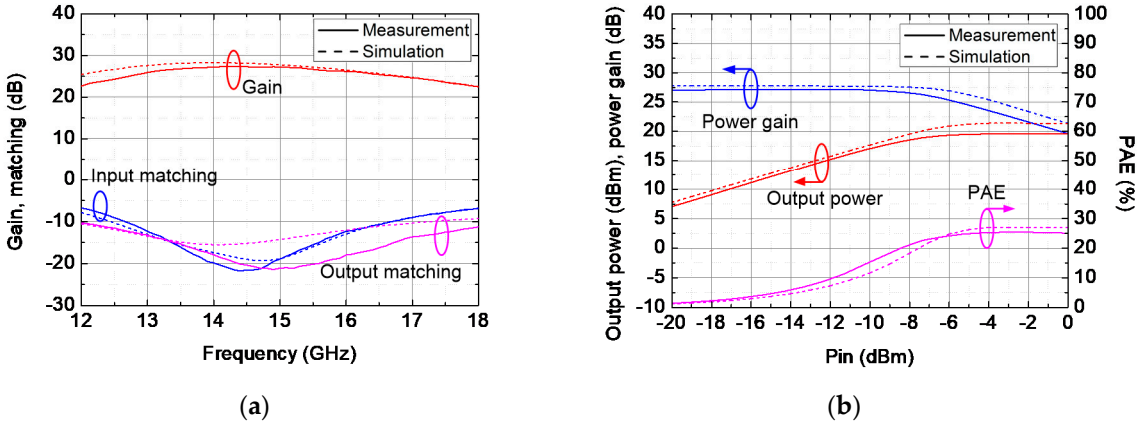


Figure 12. Schematic and chip micrograph of the medium power amplifier (MPA).

A three-stage common source topology is adopted to obtain more than 20 dB gain over the Ku-band. In the first two stages, a 2 × 50-μm HEMT (M_1, M_2) is used for high gain and wide bandwidth. The third stage employs an 8 × 50-μm HEMT (M_3) for high output power and linearity. The input is matched to 50 Ω by the L-section network of L_1 and L_2. Two inter-stage matching networks are implemented using L_3-L_4-L_5-L_6 and L_7-L_8-C_5, respectively. The matching frequencies of the networks are intentionally set differently from each other, such that wideband operation is obtained. The output network (L_9) is matched to the load-pull impedance for high output power. A parallel R-C network (R_1 and C_2) is inserted into the signal path to improve the stability at low frequencies. The MPA test cut, as shown in Figure 12, occupies 1.9 × 1.0 mm^2, excluding probing pads. The MPA consumes DC power of 380 mW, with a drain bias voltage of 5 V. The measurement results are shown in Figure 13. As shown in Figure 13a, the MPA exhibits a peak gain of 27.3 dB at 14.2 GHz and more than 22.4 dB gain over the Ku-band. The input and output matching are below −6.7 and −10.3 dB, respectively, over the Ku-band. The output power, power gain and power-added efficiency (PAE) at 15 GHz are shown in Figure 13b. The output P1dB (OP1dB) and saturated power (P_{sat}) are 18.9 and 19.6 dBm, respectively. The maximum PAE is 25.5%. A discrepancy between the measurement and simulation is presumably due to inaccuracy of the large-signal transistor model.



(**a**) (**b**)

Figure 13. Measurement results of the MPA. (**a**) Gain and matching performance, (**b**) output power, power gain and power-added efficiency (PAE) versus input power at 15 GHz.

3.5. Low-Noise Amplifier (LNA)

A schematic and micrograph of the Ku-band three-stage LNA is shown in Figure 14. The first two stages employ a 2 × 50-μm HEMT (M_1, M_2) while the last stage uses a 2 × 75-μm (M_3), considering the tradeoff among the gain, noise figure and DC power consumption. The inductive source degeneration (L_S) is applied to the first stage for compromising the noise figure, input matching and gain. In Figure 15, the maximum available gain (MAG) and minimum noise figure (NF_{min}) are simulated with different L_S values. With a compromised value of 0.35 nH, the MAG and NF_{min} exhibit values of 8.6 dB and 0.74 dB, respectively, at 15 GHz. A 10-Ω series resistor (R_S) is inserted into the output of each stage to improve the stability.

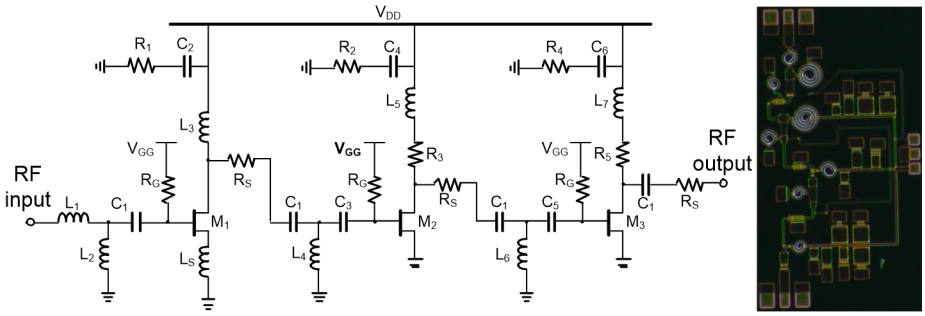


Figure 14. Schematic and chip micrograph of the low-noise amplifier (LNA).

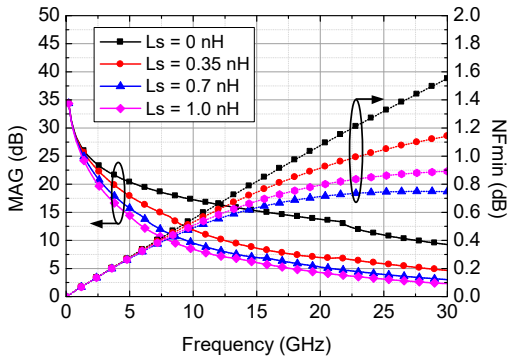


Figure 15. Simulated maximum available gain (MAG) and minimum noise figure (NF_{min}) of the 2 × 50-μm transistor with various values of L_S.

The LNA test cut occupies an area of 1.6×0.9 mm^2, excluding probing pads, as shown in Figure 14. The LNA consumes a DC power of 92 mW, with a drain bias voltage of 2 V. Figure 16 shows the measurement results of the LNA. The measured peak gain and noise figure, shown in Figure 16a, are 27.5 dB and 2.4 dB, respectively, at 15 GHz. In Figure 16b, the measured input matching is below −10 dB from 13.7 to 28.5 GHz. The output matching is broadband, below −10 dB, from 3.6 to above 30 GHz, due to the lossy output matching network.

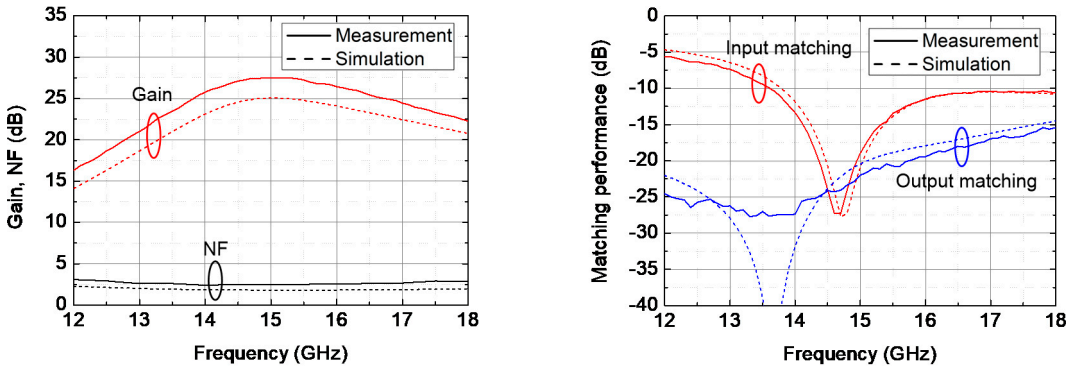


Figure 16. Measurement results of the LNA. (**a**) Gain and noise figure, (**b**) input and output matching.

4. Multifunction Transmitter and Receiver

The transmitter and receiver are designed by integrating the circuit blocks described in Section 3. The chip micrographs are shown in Figure 17. Each chip occupies 4.2×2.8 mm^2, including probing pads. On-wafer probing measurement is performed with a vector network analyzer, noise figure analyzer and power meter. The input digital signals of SPC (D_{in}, CLK, EN) are generated by NI USB-6361 X series multifunction DAQ. To facilitate the measurement for 512 states, the measurement equipment and DAQ are controlled by LABVIEW.

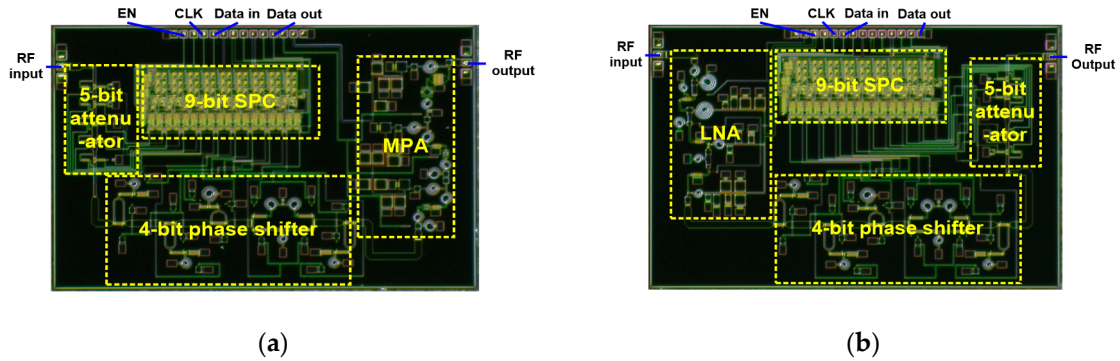
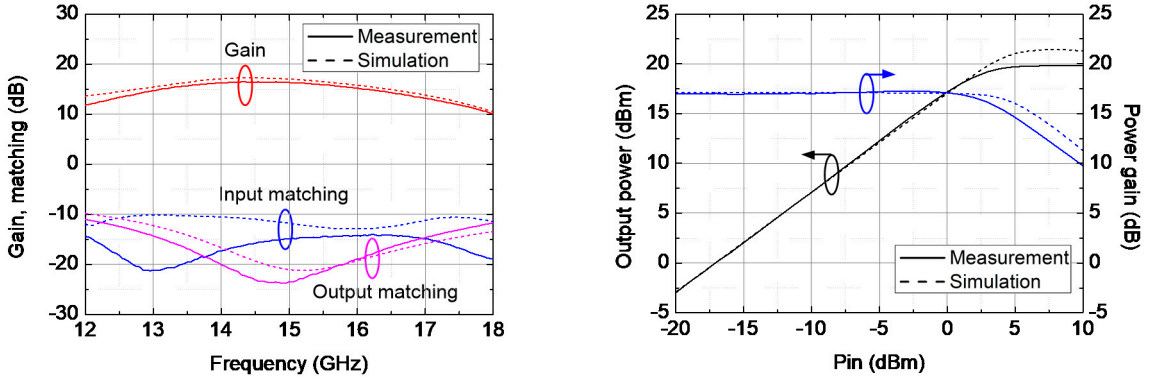


Figure 17. Chip micrographs of (**a**) the multifunction transmitter, (**b**) receiver.

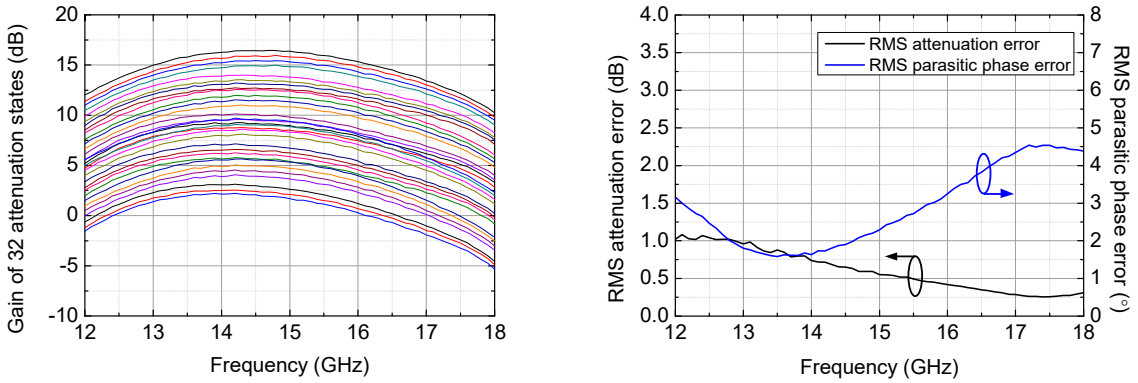
The measured gain, matching and output power of the multifunction transmitter chip are shown in Figure 18. The gain exhibits a peak value of 16.5 dB at 14.7 GHz and more than 10 dB over the Ku-band. The input and output matching are below −10 dB over the Ku-band. The OP1dB and P_{sat} at 15 GHz are 19.2 and 19.8 dBm, respectively.



(**a**) (**b**)

Figure 18. Measurement results of the multifunction transmitter in the reference state: (**a**) gain and matching performance, (**b**) output power and power gain versus input power at 15 GHz.

The measured gains for 32 attenuation states of the multifunction transmitter are depicted in Figure 19a. The gain varies from 1.5 to 16.5 dB at 14.7 GHz. The attenuation range is 13.9 to 15.9 dB over the Ku-band. The RMS attenuation and parasitic phase errors over 32 attenuation states are shown in Figure 19b. The averaged RMS attenuation and parasitic phase error values over the Ku-band are 0.6 dB and 2.9°, respectively.



(**a**) (**b**)

Figure 19. Attenuation performance of the multifunction transmitter: (**a**) gain in the 32 attenuation states, (**b**) RMS attenuation and parasitic phase errors.

The measured phase shifts of the multifunction transmitter for 16 phase states are shown in Figure 20a, confirming a full 360° shift. The RMS phase and parasitic amplitude errors over 16 phase states, shown in Figure 20b, are 6.4° and 0.8 dB, respectively, on average, over the Ku-band.

The measured gain, matching and noise figures of the multifunction receiver chip are shown in Figure 21. The multifunction receiver exhibits a peak gain of 17.3 dB and noise figure of 2.5 dB at 15 GHz. The noise figure over the Ku-band is below 4.3 dB. The measured input and output matching are below −7 and −13.2 dB, respectively, over the Ku-band.

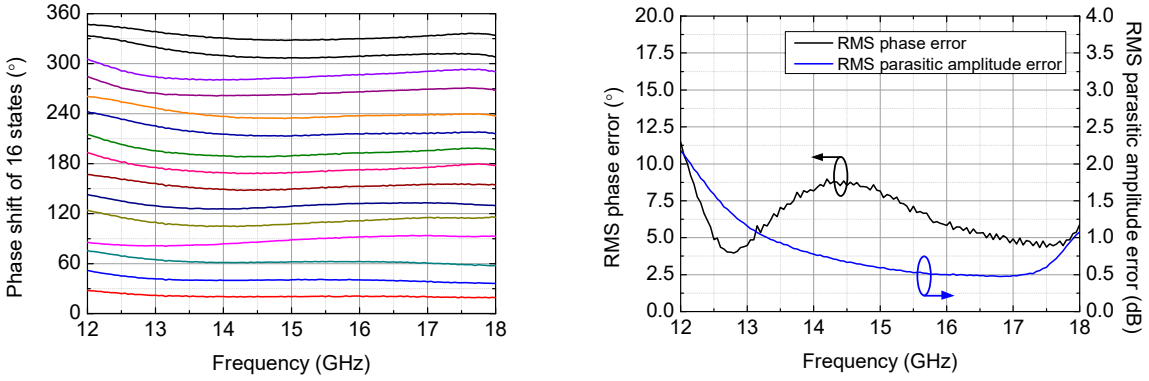


Figure 20. Phase shift performance of the multifunction transmitter: (**a**) phase shift in the 16 phase states, (**b**) RMS phase and parasitic amplitude errors.

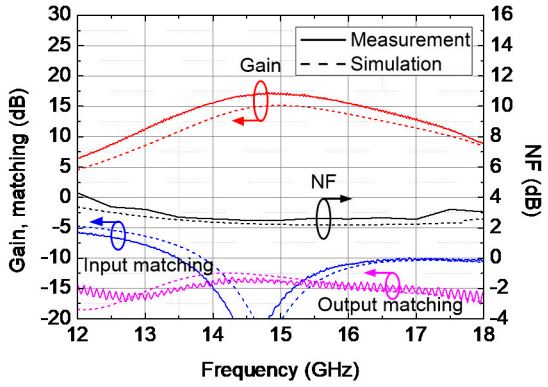


Figure 21. Measured gain, noise figure and matching performance of the multifunction receiver.

The measured gains for the 32 attenuation states of the multifunction receiver are depicted in Figure 22a. The gain varies from 2.5 to 17.3 dB at 15 GHz. The attenuation range is 13.8 to 16 dB over the Ku-band. The RMS attenuation and parasitic phase errors over the 32 attenuation states are shown in Figure 22b. The averaged RMS attenuation and parasitic phase error values over the Ku-band are 0.7 dB and 2.2°, respectively.

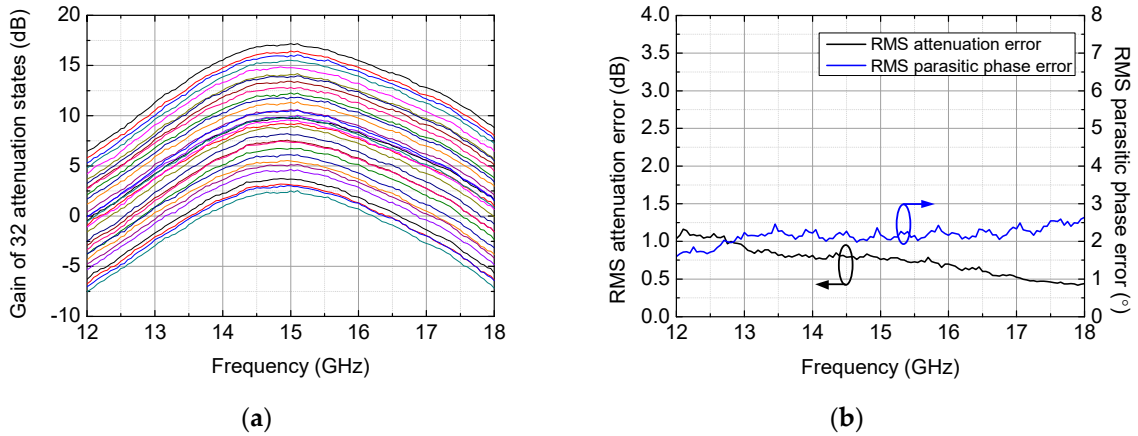


Figure 22. Attenuation performance of the multifunction receiver: (**a**) gain in the 32 attenuation states, (**b**) RMS attenuation and parasitic phase errors.

The measured phase shifts of the multifunction receiver for the 16 phase states are shown in Figure 23a, confirming a full 360° shift. The RMS phase and parasitic amplitude errors over the 16 phase states, shown in Figure 23b, are 5.1° and 0.8 dB, respectively, on average, over the Ku-band.

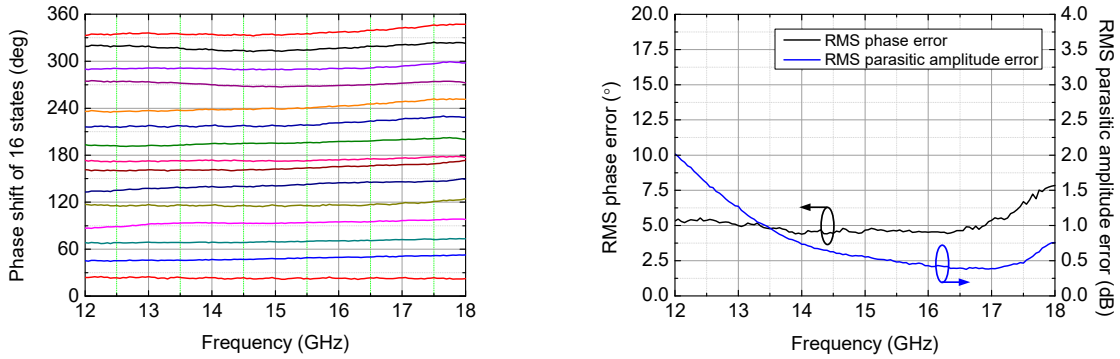


Figure 23. Phase shift performance of the multifunction receiver: (**a**) phase shift in the 16 phase states, (**b**) RMS phase and parasitic amplitude errors.

In Table 3, the performance of the multifunction transmitter and receiver in this work is summarized and compared with previously reported GaAs multifunction chips. The multifunction transmitter and receiver achieve a high level of integration, including the 5-bit digital attenuator, 4-bit digital phase shifter, 9-bit SPC and amplifier, thus presenting high gain and wideband performance. Moreover, the chipset features relatively high OP1dB and low noise figures over the full Ku-band due to the integration of MPA or LNA.

Table 3. Performance summary and comparison.

Ref.	Process	Freq. (GHz)	Architecture	$Gain_{MAX}$ [1] (dB)	OP1dB (dBm)	NF [2](dB)	PS/ATT [3](# of bits)	RMS Atten. Error [4] (dB)	RMS Phase Error [5] (°)	Chip Size (mm^2)
[1]	0.5-μm GaAs pHEMT	12–18	ATT + PS + SPC	−13	-	-	4/4	0.5	3.5	7.6
[8]	0.25-μm GaAs pHEMT	10.5–13	LNA + PS + SPC	12 *	3.3@12.25GHz	2	4/-	-	<6	3.0
[8]	0.25-μm GaAs pHEMT	13.5–15.5	PS + DA [6] + SPC	>10	12.5@14.5GHz	-	4/-	-	<3	3.0
[10]	0.18-μm GaAs pHEMT	8.6–10	SW + AMP_{Tx} [7] + AMP_{Rx} [8] + ATT + PS + SPC	11.9 (Tx) 12.3 (Rx)	-	-	6/6	-	-	14.8
[11]	0.18-μm GaAs pHEMT	6–18	SW + AMP_{Tx} + AMP_{Rx} + ATT + PS + SPC	23.5 *	>17	8	4/4	0.5	8	25.8
This work	0.25-μm GaAs pHEMT	12–18	ATT + PS + MPA + SPC	16.5	19.2@15GHz		4/5	0.6	6.4	11.7
This work	0.25-μm GaAs pHEMT	12–18	LNA + ATT + PS + SPC	17.3		4.3	4/5	0.7	5.1	11.7

[1] Maximum gain over the bandwidth. [2] Maximum noise figure over the bandwidth. [3] Phase shifter/attenuator. [4] Averaged RMS attenuation error. [5] Averaged RMS phase error. [6] Drive amplifier. [7] Transmitter amplifier. [8] Receiver amplifier. * The value is estimated from plots in the article.

5. Conclusions

In this paper, a high-gain multifunction transmitter and receiver chipset operating over the Ku-band is presented. MPA and LNA are integrated together with attenuator and phase shifter to achieve high output power and a low noise figure. In addition, SPC is integrated to control the 5-bit attenuator and 4-bit phase shifter, thereby facilitating the digital interconnection. The multifunction chipset was fabricated in a 0.25-μm GaAs pHEMT technology. The measurement results show that the multifunction chipset offers 15.5-dB attenuation with 0.5-dB step and 360° phase shift with 22.5° step. The multifunction transmitter exhibits a peak gain of 16.5 dB and OP1dB of 19.2 dBm. The multifunction

receiver exhibits a peak gain of 17.3 dB and noise figure of 2.5 dB. The multifunction chipset can be used for Ku-band phased array systems for military and satellite applications.

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