

Article

A 4-mW Temperature-Stable 28 GHz LNA with Resistive Bias Circuit for 5G Applications

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Abstract: This paper presents a low power two-stage single-end (SE) 28 GHz low-noise amplifier (LNA) in 90 nm silicon-on-insulator (SOI) CMOS technology for 5G applications. In this design, the influence of bias circuit is discussed. The 1200 Ω resistor which was adopted in bias circuit can feed DC voltage as well as keep whole circuit unconditionally stable. The gate bias points are set to 0.55 V to make the circuit low-power and temperature-stable. Measurement results illustrated that the LNA achieved a maximum small signal gain of 18.1 dB and an average 3.1 dB noise figure (NF) in operating frequency band. Measured S11 was below -10 dB between 25 GHz and 29 GHz and reverse isolation S12 was below -25 dB throughout the band. It consumed only 4 mW by proper selection of bias point with core area of 0.16 mm² without pads. The fabricated LNA has demonstrated a gain variation of 3 dB and a NF variation of 1.9 dB from -40 °C to 125 °C with power variation of 0.8 mW. It suggests that the proposed SOI CMOS LNA can be a promising candidate for 5G applications.

Keywords: low-noise amplifier; bias circuit; neutralized; SOI; 5G; temperature-stable

1. Introduction

Recent years have witnessed the development of the fifth-generation wireless system (5G), which can provide higher data rate, lower delay and larger-scale equipment connection compared with 4G [1–3]. To achieve high data-rate and high resolution for numerous applications, such as augmented reality (AR), Internet of things (IOT), smart home, automatic driving, etc. [4], millimeter-band is introduced owing to its unique advantages. Results in our previous work [5] showed that the use of frequency band between 24 GHz and 29 GHz is prevalent. The band is considered as the most popular 5G band, and circuits working in this band are worthy of studying. In Figure 1, the diagram of 5G phased-array transceiver is present [6]. To realize the massive multiple-input multiple-output (MIMO) and phased array techniques, more than one transceiver (TRX) is integrated in the system [7]. Moreover, a temperature-stable TRX is always desirable for 5G applications. Under this circumstance, a compact LNA with small area and low power consumption while maintaining good performance even at different temperatures is necessarily required.

As a critical building block in the radio frequency front-end module, LNA is always expected to achieve certain gain without introducing much noise since it dominates the radio sensitivity [8]. Numerous researchers have studied LNA for 5G applications [6,9–11]. The III–V technologies like GaAs, InP, GaN, etc., were once the first choice due to their excellent-performance and high-efficiency [9], but the low integration level and high cost are insufferable. As a contrast, the burgeoning CMOS

technology is promising to overcome the difficulties of above [6,10]. However, the costly process in [6] and poor performance in [10] are still intolerable.

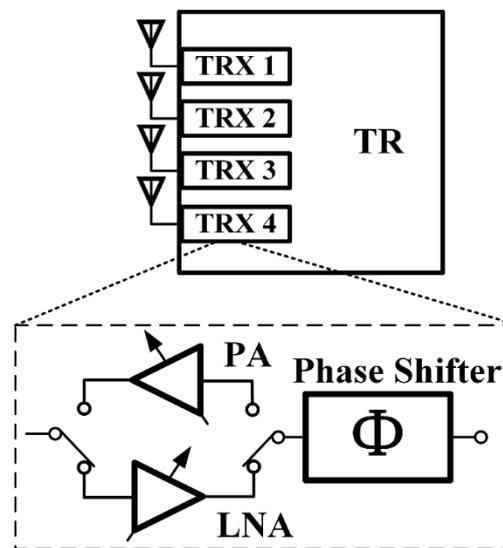


Figure 1. Block diagram of the phased-array transceiver.

Up to this day, the SOI CMOS process has drawn increasing attention due to its exclusive advantages [12–14]. Compared with bulk CMOS technology, the SOI's buried oxide layer above low resistivity substrate decreases RF coupling to the conductive Si substrate. Consequently, the parasitic resistance and capacitance of the transistors could be significantly reduced, thereby leading to a higher f_T and f_{MAX} . Furthermore, high-Q-factor passive components, like inductors and capacitors, can be realized on the SOI platform. Its lower temperature sensitivity of the threshold voltage makes it possible to get relatively temperature-stable performance [15]. Moreover, SOI process' high integration level is appropriate for RF front-end components integration. Therefore, SOI CMOS process is expected to be cost-effective for 5G applications.

In the case of LNAs, the design of the bias circuit is a key issue to make the transistors work in proper DC operating point [16], which determines gain, NF, stability, etc. The performance at different temperatures is related to the bias point, too. Other authors have investigated the impact of biasing on peak f_{max} values and noise parameters of MOSFETs [17], and paper [18,19] reported the temperature effect with different bias points. A gain-stable LNA is introduced in [15] while the NF and power consumption varied much at different temperatures. In this design, the simultaneous noise and input matching (SNIM) [20] is used to ensure high gain and low NF without sacrificing each other, which used to be a tradeoff. However, the SNIM state will be easily influenced by the bias circuit when designing LNAs, leading to mismatch and deteriorated performance. No paper has reported the influence of bias circuit on SNIM state in an LNA. Under this circumstance, a well-designed bias circuit is worthy of discussing.

In this paper, we studied the influence of bias circuit on the performance of LNA utilizing SNIM method. The bias points were selected to make the proposed LNA low-power and temperature-stable. After simulation, results showed that circuit properly fed by a modest resistor exhibits high gain, low-noise and unconditionally stable in full spectrum band. On the basis of designated bias circuit, in second stage a neutralized inductor was introduced to resonate with parasitic capacitors between the common source (CS) transistor and the common gate transistor (CG). Meantime, an inductor was added at the gate of the CG transistor as resonant tank to boost gain at the target frequency.

2. Analysis and Design

2.1. Bias Circuit Design

2.1.1. Bias Circuit with SNIM

In traditional condition, the main parameters: gain and NF, were a tradeoff. Thanks to SNIM method, researchers can get balanced results by uncomplicatedly designing. It has been widely used since it was proposed [20]. However, the non-ideal bias circuit will affect the SNIM state. In this way, both input matching and noise matching lose efficacy.

The bias circuit consists of applied voltage source, bypass capacitors and bias-feed component in general. Among them, the bypass capacitors usually include 1–3 different capacitances to make sure the clutter signals from supply source can be bypassed. The bias feed component plays the role of feeding DC signal while blocking RF signal in general. The bias circuit is regarded as an open circuit in the small-signal, and the bias-feed component is often an inductor or a resistor.

Figure 2 shows two placement modes of bias circuit with SNIM. V_s stands for the signal source who feeds RF signal and R_s is its intrinsic impedance. Capacitor C_{in} is used to block the DC signal and inductors L_{in} and L_s are introduced to get SNIM. Under ideal conditions, the blocking capacitor C_{in} can be neglected. The schematic diagram of input small signal of two modes can be seen in Figure 3.

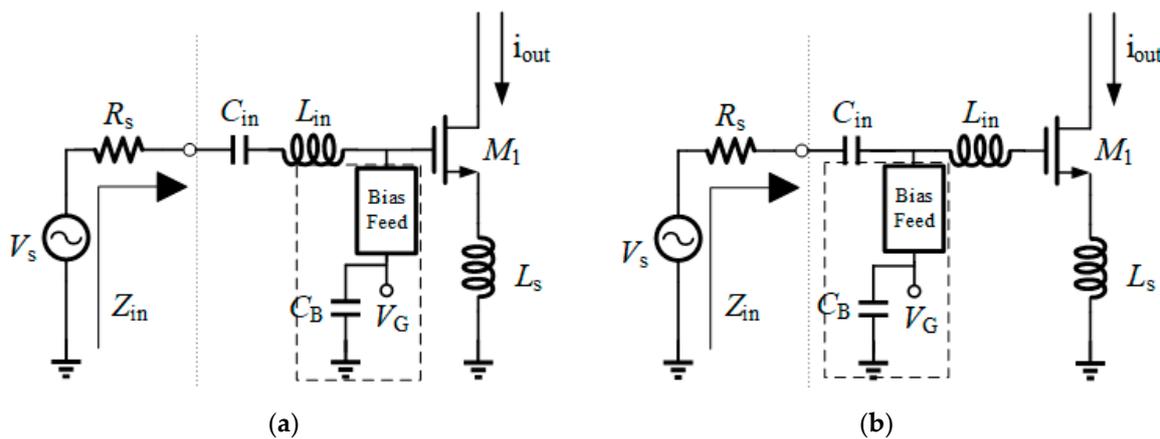


Figure 2. (a) Input schematic diagram with bias circuit postposition after L_{in} ; (b) input schematic diagram with bias circuit preposition before L_{in} .

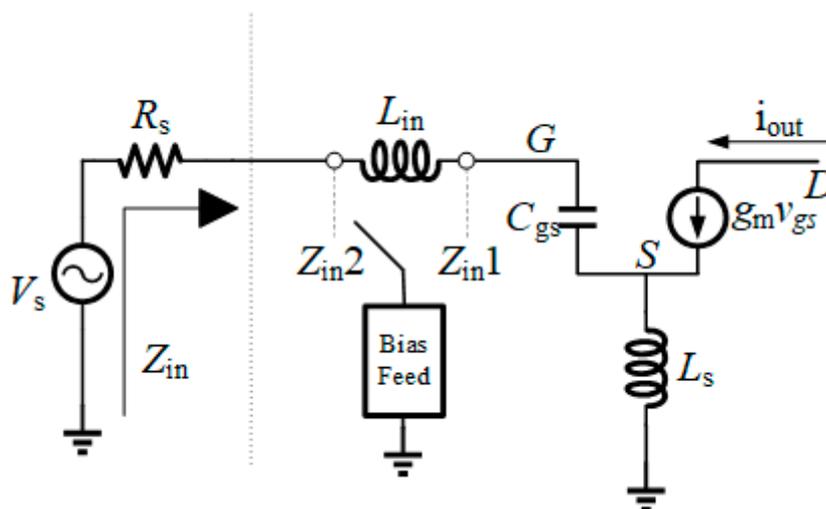


Figure 3. Schematic diagram of input small signal.

According to the SNIM method, the small signal input impedance can be expressed as

$$Z_{in} = sL_{in} + sL_s + \frac{1}{sC_{gs}} + \omega_T L_s \quad (1)$$

where $\omega_T = g_m/C_{gs}$. In RF applications, LNA receives signals from antenna whose intrinsic impedance R_s is commonly 50 Ω . For input matching, Z_{in} should get conjugate match with source impedance. Moreover, for noise matching, Z_{in} should be equal to the optimum source impedance, which is set to R_s in SNIM. That is to say, as long as SNIM is achieved, Z_{in} from Equation (1) is equal to R_s and the imaginary part is equal to 0. When taking non-ideal bias circuit into account, the input impedance can be expressed as

$$Z_{in1} = sL_{in} + Z_B \parallel (sL_s + \frac{1}{sC_{gs}} + \omega_T L_s) \quad (2)$$

$$Z_{in2} = Z_B \parallel (sL_{in} + sL_s + \frac{1}{sC_{gs}} + \omega_T L_s) \quad (3)$$

where Z_{in1} stands for condition of bias circuit postposition after L_{in} in Figure 2a and Z_{in2} stands for condition of bias circuit proposition before L_{in} in Figure 2b.

From the viewpoint of size reduction, the inductor bias-feed circuit needs an area consumptive off- or on-chip inductor and the use of an on-chip resistor bias feed instead of an inductor bias feed is preferable [21]. By this means, in Equations (2) and (3), $Z_B = R_B$. From Equation (1), the Z_{in} is equal to 50 Ω , so Equations (2) and (3) can be simplified as

$$Z_{in1} = R_s - \frac{(sL_{in})^2}{R_B - sL_{in}} \quad (4)$$

$$Z_{in2} = R_B \parallel R_s \quad (5)$$

From Equation (5), we can easily conclude Z_{in2} is approximately equal to R_s as long as Z_B is much larger than R_s . As for Z_{in1} , an extra inductive impedance part is added, leading to mismatch of input-matching and noise-matching.

To find a proper resistor for bias circuit, simulation of two placement modes of bias circuit with different resistors from 300 Ω to 3000 Ω is carried out and the results shown in Figure 4. To simplify the comparison, the second stage of the LNA is discarded. Three main parameters: K factor, noise figure and S11, presenting the stability, noise matching and input matching, respectively, most sensitive to bias circuit, are selected as performance index.

Researchers found proper resistance bias resistor could enhance the stability of amplifiers [22]. Unconditional stability in whole band is a must for LNA to avoid oscillation happening, which is unexpected for designers. Therefore, keeping the circuit stable is top priority, which means the K factor should be larger than 1 in the whole band. Figure 4a depicted K factor of bias circuit postposition after L_{in} and Figure 4b depicted K factor of bias circuit proposition before L_{in} . The two results share the same trend. From Figure 4a, b, the stability is decreasing with the bias resistance increasing. However, when bias resistance is larger than 1500 Ω , the K curve will show a part below 1. We commonly call this part "unstable area". In this design, the bias resistor with resistance no more than 1500 Ω is allowed.

Figure 4c,d depicted NF with different resistance bias circuits in two conditions mentioned above. On the whole, the NF performance is better as the bias resistance is larger. With same bias resistor, results in Figure 4c show higher noise than Figure 4d. It is consistent with former theoretical derivation in Equations (4) and (5), indicating that resistor bias circuit postposition after L_{in} has a greater effect on SINM than resistor bias circuit proposition before L_{in} . Figure 4d also indicated that when bias resistance is larger than 1200 Ω , the decreasing trend of NF is not obvious. It can be assumed that resistance of bias resistor is accepted when larger than 1200 Ω . Input reflecting parameter S11 of two

conditions are shown in Figure 4e,f. With bias resistance increasing, S11 performance became better. Compared with figure S11 in Figure 4e, the minimum point frequency of S11 shown in Figure 4f is more constant. In practice, S11 is adequate when it is below 10 dB. The frequency band of S11 below 10 dB in Figure 4f is wider than the one in Figure 4e. Once again, the resistor bias circuit proposition before L_{in} has proved to be better than resistor bias circuit postposition after L_{in} .

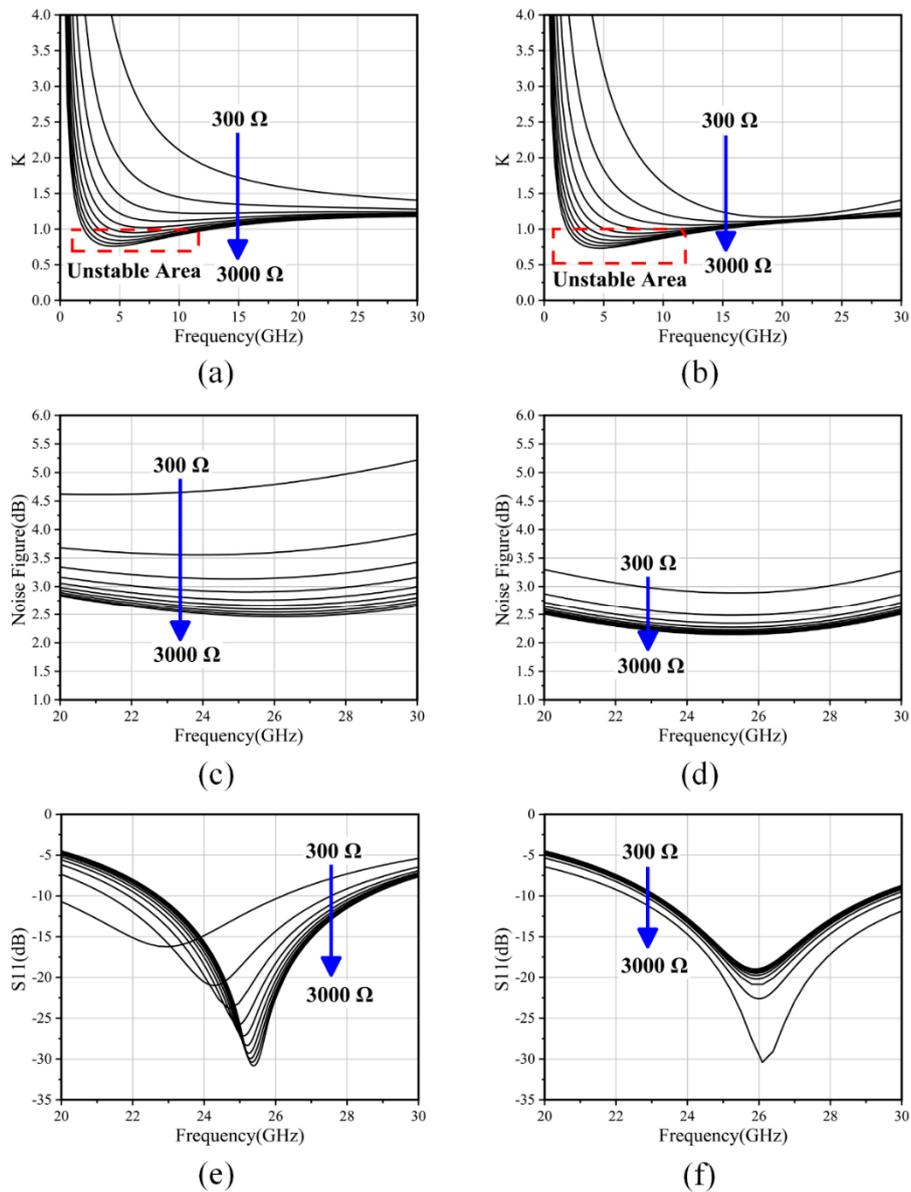


Figure 4. (a) Simulated K factor with resistor bias circuit postposition after L_{in} ; (b) simulated K factor with resistor bias circuit proposition before L_{in} ; (c) simulated noise figure with resistor bias circuit postposition after L_{in} ; (d) simulated noise figure with resistor bias circuit proposition before L_{in} ; (e) simulated S11 with resistor bias circuit postposition after L_{in} ; (f) simulated S11 with resistor bias circuit proposition before L_{in} .

After taking K factor, NF and S11 into consideration, a 1200 Ω resistor is chosen in bias circuit to make the circuit unconditionally stable in whole band and good performance of noise figure and input reflection parameter S11.

2.1.2. Bias Points Design

To make the circuit low-power and temperature-stable, a proper bias point is of great significance. For the CMOS technology MOSFETs, there is a particular bias point characterizing the temperature behavior called “Zero Temperature Coefficient” (ZTC) [18]. The ZTC bias point is defined as the bias at which the transconductance characteristic (g_m - V_{GS}) of the MOSFET remains constant when temperature varies, as shown in Figure 5.

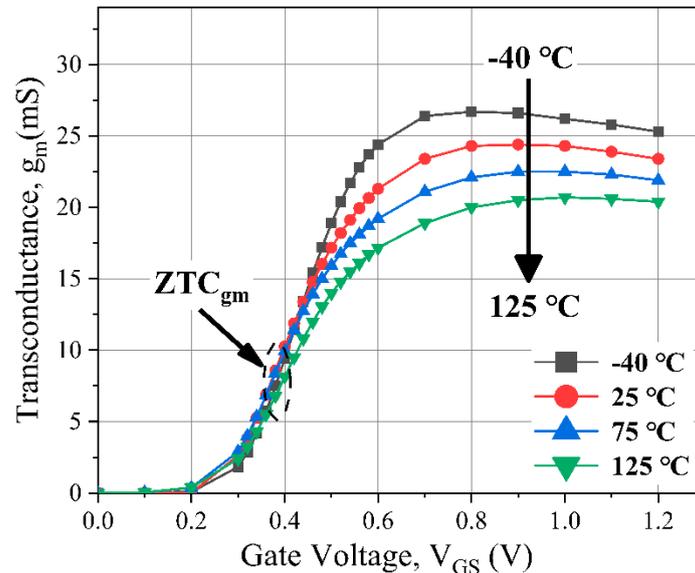


Figure 5. Simulated g_m vs. V_{GS} at different temperatures.

From Figure 5, the ZTC can be observed to be 0.4 V, which means transconductance of the MOSFET can be constant when temperature varies from $-40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ at the bias voltage of 0.4 V. However, the g_m in ZTC, which plays an important role in gain, is not big enough to keep adequate gain performance. Based on the simulation results, variation at different temperatures of NF and power became more gently with bias voltage increasing. Setting bias voltage to 0.4 V can achieve temperature-stable gain performance, while degrading NF and power consumption consistency at different temperatures. To make the LNA a balanced one, NF, gain and power as well as their temperature variations should be taken into consideration. After simulation and comparison, bias points of amplification transistors are elaborately set to 0.55 V for enough gain, acceptable NF and power consumption reduction, sacrificing temperature stability to a certain extent.

2.2. Two-Stage Single-End LNA Design

On the basis of optimized resistor bias circuit, a two-stage single-end LNA is designed in our work. The single-end topology is adopted to avert lossy balun and additional power consumption. To meet the requirements of noise figure and gain, a common-source (CS) amplifier is set to be first stage to keep the circuit low-noise, followed by a cascode amplifier to enhance gain. The schematic of proposed two-stage single-end LNA is shown in Figure 6.

As depicted in Figure 6, sizes of transistors M1, M2 and M3 are selected elaborately through simulating. Moreover, proper biasing is chosen to make the circuit keep low-noise and adequate gain. L_m , as neutralized inductor, is added between the CS and the common-gate (CG) to resonate with parasitic capacitor to minimize the NF and increase the gain [23]. Meantime, an inductor L_g is added at the gate of the CG transistor as resonant tank to boost gain at the target frequency [24]. L_m is well-designed transmission line fabricated with upmost metal to maintain high Q, as well as L_g . A matching network composed of C_p , L_p and C_1 is used to get interstage match and transfer signal.

C_{B1} – C_{B4} are bypass capacitors for leaching the clutter signal from supply source. The elements values of proposed LNA is shown in Table 1.

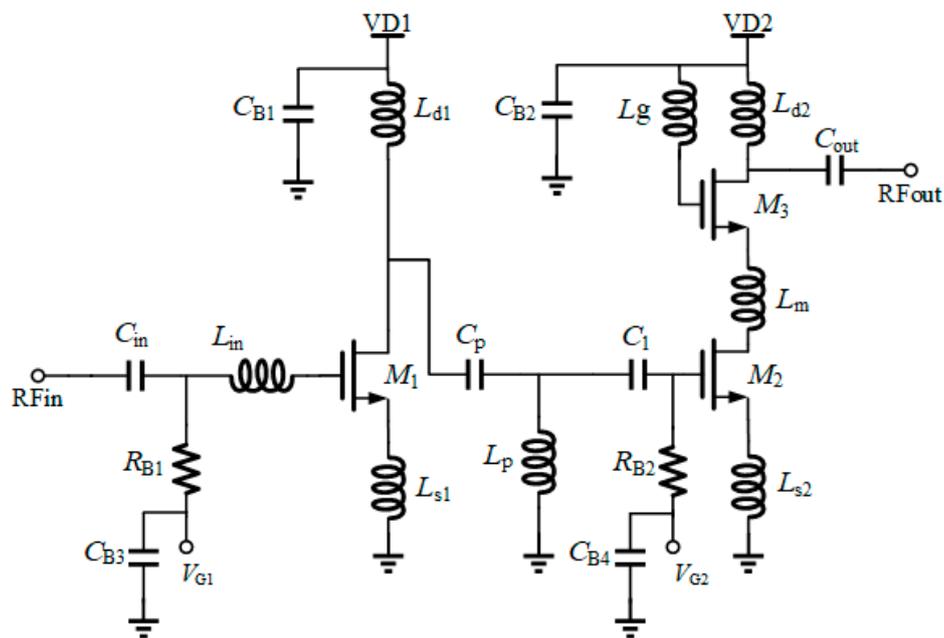


Figure 6. Schematic of two-stage single-end low-noise amplifier (LNA).

Table 1. Elements values of proposed LNA.

M_1 – M_3 30 $\mu\text{m}/90$ nm	C_{in}/C_{out} 1.25 pF	C_{B1} – C_{B4} 2 pF	R_{B1}/R_{B2} 1.2 k Ω	C_p 110 fF	C_1 1 pF	L_{in} 680 pH
L_{s1} 300 pH	L_{s2} 270 pH	L_{d1} 550 pH	L_{d2} 700 pH	L_m 140 pH	L_g 160 pH	

To reduce the power consumption, VD1 was set to be 0.45 V while VD2 was set to be 1.2 V. The bias points of M1 and M2 were set to 0.55 V, as discussed above. Parasitic parameters of transistors was extracted with Calibre. Passive part of the layout, such as inductors, capacitors and transmission lines were simulated in ADS momentum EM simulator.

3. Results

The proposed LNA was fabricated in a 90-nm SOI CMOS process. The chip photo is shown in Figure 7. To minimize the chip area and avoid degrading performance, elements were put closely to each other based on the EM simulation results. Every DC pad had connected to ground chip with an on-chip 2 pF decoupling capacitor. Finally, a compact LNA chip size of 0.63 mm \times 0.5 mm was achieved. Excluding pads and edge, the chip was only 0.47 mm \times 0.33 mm. The power consumption was only 4 mW with assigned supply voltage. Compared with others [6,9,11,13,14], it consumed the least power and occupies a rather small area.

Measurements at ambient temperature of this 28 GHz LNA were carried out on an RF probe station to avoid the parasitic effects introduced by the packing, circuit board or connection wires. The Agilent N5247A network analyzer offered platform for small-signal measurements. NF was measured with Agilent N8975A NFA series noise figure analyzer. The measured and simulated small signal results are shown in Figure 8a. The measured S21 was identical to simulated S21 in the frequency band before 26 GHz. After gain reached its peak of 18.1 dB at 26 GHz, the measured S21 began to be lower than simulated one. The -3 dB bandwidth measured was about 2 GHz from 24.8 GHz to 26.8 GHz, much less than the simulated bandwidth of 3 dB from 24.5 GHz to 27.5 GHz. The reason

may be the worsened S22 measured than simulated. The S11 was lower than -10 dB from 25 GHz to 29 GHz and S22 was under -10 dB from 25.2 GHz to 26.5 GHz. Moreover, S12 seen in Figure 8a showed good reverse isolation below -25 dB throughout the band. Figure 8b shows the measured and simulated NF. An average 3.1 dB noise figure (NF) in operating frequency band was obtained in this design, and the minimum NF was 2.8 dB at 24 GHz and 27.5 GHz.

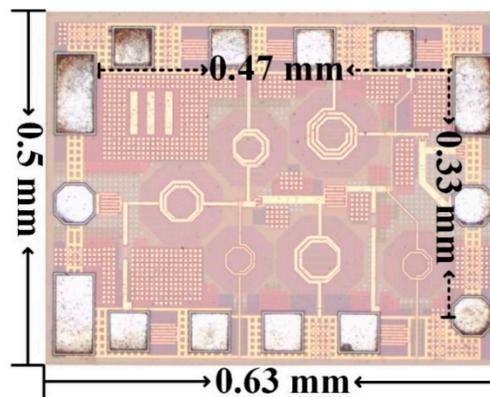


Figure 7. Chip photo of the proposed LNA.

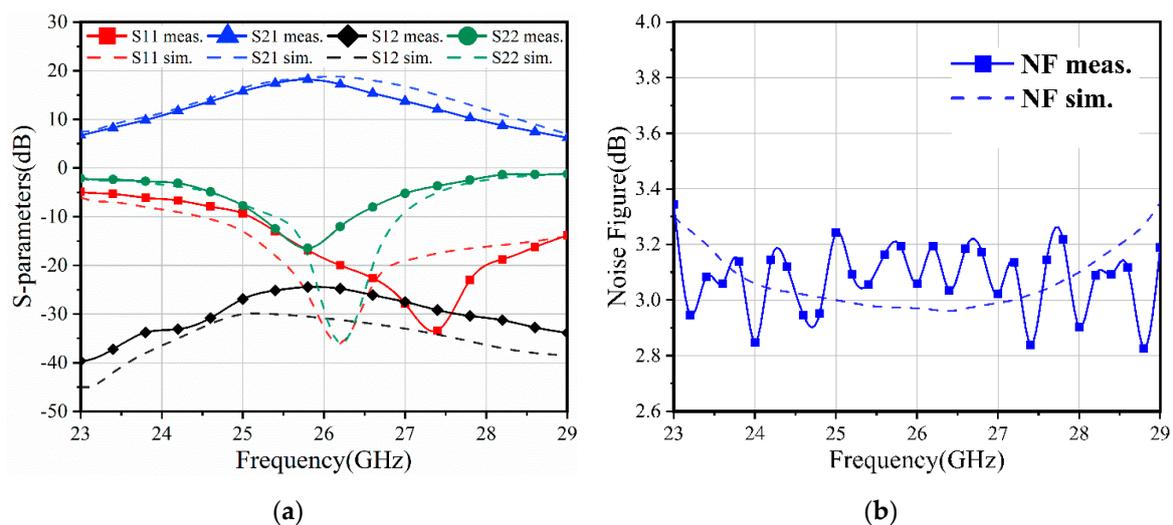


Figure 8. (a) S-parameters of measurements and simulations; (b) noise figure of measurements and simulations.

Figure 9a,b illustrated $IP_{1\text{ dB}}$ and IIP3 separately. The power gain versus input power was plotted in Figure 9a, from which an $IP_{1\text{ dB}}$ of -16 dBm at 26 GHz can be extracted. The IIP3 is -6 dBm from Figure 9b. Measurement results showed poor linearity of the design. Linearity, gain and power consumption are always tradeoff. In this design, the gain and power consumption are relatively good, especially the latter. By increasing power consumption, linearity can improve a lot.

The performance of the proposed LNA is summarized in Table 2 together with the performance characterizations of other reported 28 GHz LNAs. Compared with the others, this work demonstrated the lowest power consumption and rather small area due to proper bias resistor selection and introduction of neutralized and boost inductors, making the LNA compact one.

High and low temperature semiautomatic probe station was used to measure the RF performance of LNA at different temperatures, as shown in Figure 10. To assess the temperature characteristic of the LNA, range from -40 °C to 125 °C was chosen and four representative temperatures were selected to be -40 °C, 25 °C, 75 °C and 125 °C. As can be seen, the LNA had a decreasing power gain from

18.8 dB to 15.8 dB with temperature arising, and average NF had an opposite trend from 2.3 dB to 4.2 dB. Meanwhile, power consumption varied from 3.7 mW to 4.5 mW.

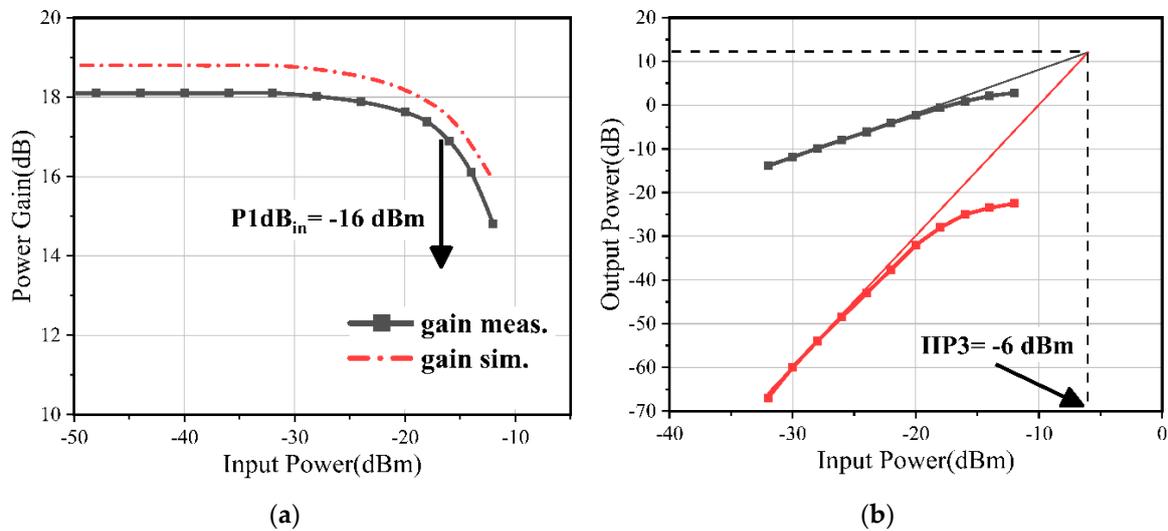


Figure 9. (a) P1dB of proposed LNA; (b) IIP3 of proposed LNA.

Table 2. Performance comparison table.

	This Work	[13]	[14]	[25]	[26]	[12]
Technology	90 nm SOI	22 nm SOI	45 nm SOI	45 nm SOI	22 nm SOI	45 nm SOI
Topology ¹	2 SE	1 SE	1 SE	1 SE	2 SE	1 SE
Bias circuit	resistive	off-chip	resistive	inductive	off-chip	resistive
Gain (dB)	18.1	12.6	10.5	8.5	20.1	12.8
NF ² (dB)	3.1	1.35	1.6	3	1.95	1.4
IP ₁ dB (dBm)	-16	-7.9	-10.3	3.5	NA	NA
IIP3 (dBm)	-6	1.4	NA	NA	-14	5
P _{DC} (mW)	4	13	6	12	17.3	7
Area ³ (mm ²)	0.16	0.21	0.18	NA	0.05	0.3

¹: "2 SE" refers to 2-stage single-end; "3 Diff." refers to 3-stage differential; ²: average NF; ³: core area without pads.

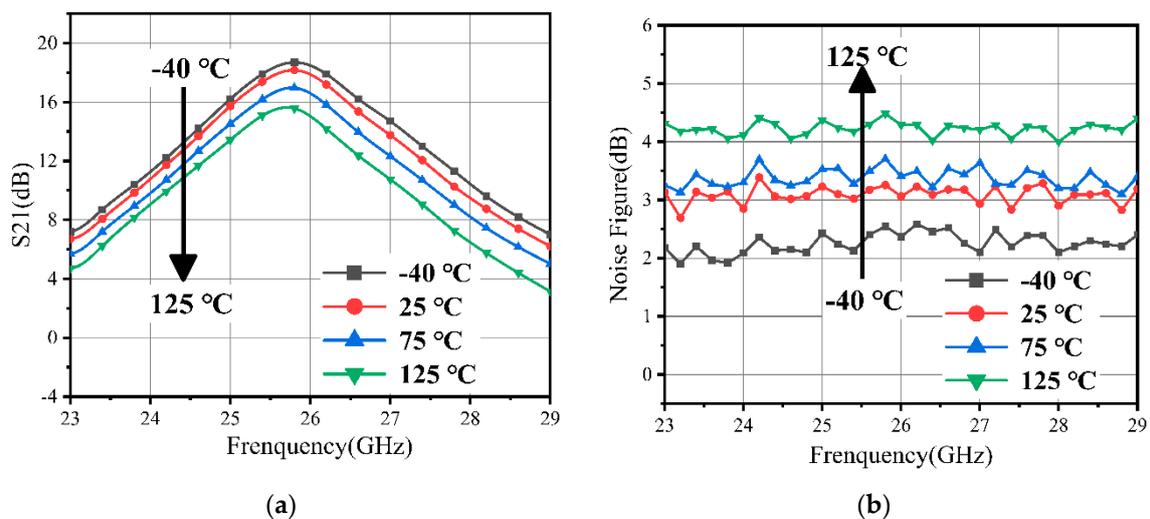


Figure 10. (a) Measured S21 at different temperatures; (b) measured NF at different temperatures.

Performance comparison of proposed LNA and others at different temperatures are summarized in Table 3. No one has studied performance of LNA for 5G application at different temperatures,

while article [15,27] can be as reference because the performances variations share same tendency with the wide range of temperature. As can be seen, the 1.9 dB variation of NF and 0.8 dB variation of power consumption were the smallest among them. Though article [15] showed better gain-stable performance, the NF and power consumption varied much at different temperatures. After comprehensive consideration of gain, NF and power consumption variation, the proposed LNA shows good temperature stability.

Table 3. Performance comparison table at different temperatures.

	This Work	[15]	[27]
Technology	90 nm SOI CMOS	130 nm SOI CMOS	180 nm CMOS
Frequency (GHz)	26	2.5	17
Gain (dB)	15.8–18.8	9.1–10	18.7–23
Gain variation (dB)	3	0.9	4.3
NF (dB)	2.3–4.2	3.4–5.7	2.2–4.3
NF variation (dB)	1.9	2.3	2.1
Power consumption (mW)	3.7–4.5	2.2–3.7	66 ¹
Power variation (mW)	0.8	1.5	NA
Temperature range (°C)	−40–125	25–200	−55–120

¹: power consumption at ambient temperature.

4. Conclusions

In this paper, the influence of the bias circuit with SNIM is studied, which is of great significance for LNA design. Proper resistance of bias resistor can make the circuit unconditionally stable in the whole band, enhance gain and decrease NF without deteriorating the SNIM state. Bias points of the circuit were chosen to keep performance temperature-stable and reduce power consumption. Neutralized technology and boost inductors were introduced to improve performance. Based on these, a two-stage single-end LNA is fabricated in 90-nm SOI CMOS technology occupying only 0.16 mm² core area. Experimental results showed a maximum small signal gain of 18.1 dB with 3.1 dB average NF, while consuming only four microwatts. The little variation of performance at different temperatures showed good temperature stability. These results demonstrated that the proposed LNA can be a promising candidate for 5G applications.

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