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A Sub-THz Wireless Power Transfer for Non-Contact Wafer-Level Testing

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Abstract: In this paper, a sub-THz wireless power transfer (WPT) interface for non-contact wafer-level testing is proposed. The on-chip sub-THz couplers, which have been designed and analyzed with 3-D EM simulations, could be integrated into the WPT to transfer power through an air media. By using the sub-THz coils, the WPT occupies an extremely small chip size, which is suitable for future wafer-testing applications. In the best power transfer efficiency (PTE) condition of the WPT, the maximum power delivery is limited to 2.5 mW per channel. However, multi-channel sub-THz WPT could be a good solution to provide enough power for testing purposes while remaining high PTE. Simulated on a standard 28-nm CMOS technology, the proposed eight-channel WPT could provide 20 mW power with the PTE of 16%. The layouts of the eight-channel WPT transmitter and receiver occupy only 0.12 mm^2, 0.098 mm^2, respectively.

Keywords: wireless power transfer (WPT); non-contact testing; sub-THz WPT; wafer-level testing

1. Introduction

Wafer-level testing is an essential process for semiconductor device fabrication. The traditional wafer testing technique utilizes a probe card that directly connects to pads or bumps of a device under test (DUT) [1], as shown in Figure 1a. The probe card is required to be accurately placed on top of the DUTs because any misalignment between the probe card and the DUTs could lead to unreliable testing results. To overcome the misalignment risk, a complex probe card is required and testing cost could be increased [2]. Moreover, direct contact causes severe damage to both the probe card and the DUT. In simultaneous on-wafer test technique, as demonstrated in [2], all DUTs on a given wafer are tested at the same time for the maximum testing speed. Each pad of the DUTs generally suffers from an approximate pressure of three grams during the wafer test [2]. If 2000 DUTs are fabricated in a wafer and each DUTs has 60 pads, the total pressure on the pad is 350 kg, which could break any wafer used in recent semiconductor technology [2]. Therefore, the traditional wafer testing technique encounters challenges from high-cost testing, low-reliability, and limited testing speed.

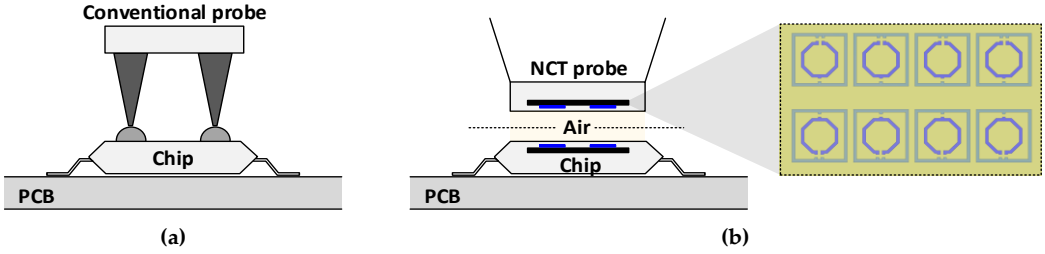


Figure 1. (**a**) The traditional wafer-level testing interface; (**b**) Non-contact wafer-level testing interface with inductive coupling link.

The challenges of the contact testing technique lead to the studies of non-contact testing (NCT) interface [3–8] where the wired link has been replaced by the inductive coupling link. Compared to the complex probe card of the wired testing interface, the NCT probe card has a simpler architecture, therefore, the testing cost could be significantly reduced [3–5]. The NCT interface provides a more reliable testing result because the performance of the inductive coupling link remains more stable than the performance of the direct contact link when the misalignment risk happens [6,7]. Additionally, when the pressure on the wafer has been removed, the testing speed could be improved because more DUTs could be tested at the same time [3,6,8]. However, increasing the number of DUTs on a single wafer leads to a new challenge, the NCT chip size needs to be very small. An NCT system usually requires both wireless data transfer (WDT) and wireless power transfer (WPT) chips [9–12], which occupy a very large chip size due to the bulky inductive couplers. Therefore, NCT in the advanced wafer-level testing technique requires a new task: reduce WDT and WPT chip size.

Recent research on WPT [2,13–18] has been reported in terms of scaling down chip size and improving power transfer efficiency (PTE). Aiming to the biomedical applications, the conventional WPTs in [13–17] only focus on optimizing the receiver (RX) chip size. The transmitter (TX) chip size is usually very large to provide enough power to the RX because the transfer distance is required to be larger than a certain value (i.e., TX area: 900 mm^2, distance: 10 mm [14]). To be designed for the applications with much shorter distance, the conventional WPTs in [2,18,19] provide both optimized TX and RX chip size (i.e., TX area: 0.49 mm^2, RX area: 0.49 mm^2, distance: 0.02 mm [18]). When the TX chip size and the transfer distance could be considered as a trade-off, the RX chip size of the conventional WPTs is expected to be as small as possible. However, the scaling down RX chip size in the conventional method is limited by the bulky couplers, which are designed for low-frequency operation (i.e., 144 MHz [2]).

In this paper, we propose an extremely small form factor WPT by utilizing the sub-THz band for the inductive-coupling link. Figure 1b shows the principle of the proposed WPT where multiple sub-THz couplers could easily fit into a single WPT link because the sub-THz band provides much scaled inductive coils (i.e., 300 MHz as 0.7 × 0.7 mm [18], 200 GHz as 0.06 × 0.06 mm). Furthermore, from the advanced design techniques that have been reported for the conventional WPTs, the proposed WPT transmitter and receiver have been upgraded for the higher PTE in the desired sub-THz frequency operation. The proposed multi-channel WPT could be a good solution for the power coupling scalability (i.e., when more THz coils for WPT is added, more transfer power is achieved).

2. The Proposed Sub-THz WPT Design

2.1. The Proposed Sub-THz Transmitter Design

Figure 2 shows the architecture and schematic of the proposed sub-THz WPT TX. In the TX, an LC tank voltage-controlled oscillator (VCO) generates the sub-THz carrier. To provide higher power transmission, the sub-THz VCO output signal goes into a power amplifier (PA), which drives the gate voltage of M_3 and M_4 to change the current flow on an inductor (L_1). The higher current fluctuation causes a stronger magnetic field on the L_1, which enhances the efficiency of WPT. Furthermore, the network impedance of the PA is matched to our WPT load impedance for maximum power transfer. The LC-tank VCO consists of active transistors (M_1 and M_2) and an LC tank. The cross-coupled NMOS transistors are utilized to provide the negative resistances and overcome the loss due to the parasitic resistance of the LC tank. Passive circuit elements such as inductor (L) and capacitor (C) are usually very large in on-chip CMOS implementation, especially if the inductor is bulky. For our WPT, the sub-THz inductors are used to implement smaller form factor VCO and PA. Moreover, to achieve a high power gain at the sub-THz frequency operation, the PA is designed as two symmetric class E amplifiers. These amplifiers are made of two NMOS transistors and the L_1. The output impedance of

the PA is a combination of the inductance on the L_1, the parasitic capacitance ($C_{p)}$, and resistance (R_p) of the NMOS transistors and the inductor. The transfer function of the PA (A(s)) is given by

$$A(s) = \frac{sR_pL_1g_m}{s^2R_pL_1C_p + sL_1 + R_p} \quad (1)$$

or

$$A(s) = A_0 \frac{s}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \quad (2)$$

where g_m is the trans-conductance of M_3 and M_4, $A_0 = L_1g_m$ is the mid-band gain of the PA. As shown in Equations (1) and (2), the A(s) is a form of a band-pass filter transfer function with two poles frequency, ω_{p1} and ω_{p2} satisfy

$$\omega_{p1} + \omega_{p2} = \frac{1}{R_pC_p} \quad (3)$$

$$\omega_{p1} \times \omega_{p2} = \frac{1}{L_1C_p} \quad (4)$$

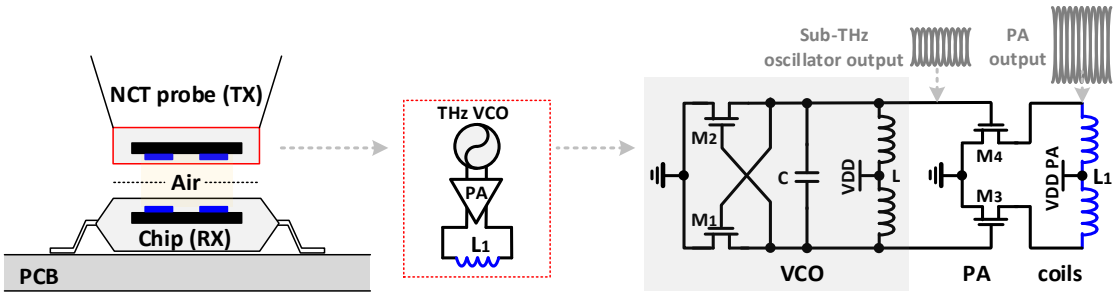
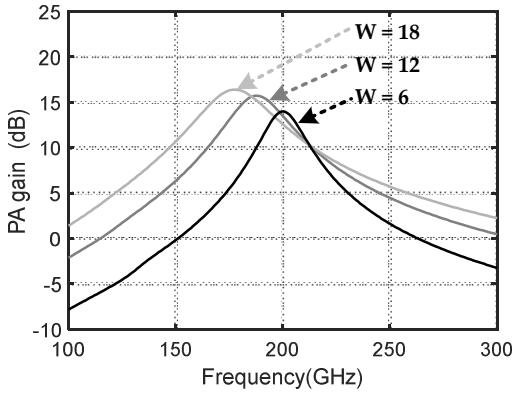


Figure 2. The architecture and schematic of the proposed sub-THz wireless power transfer (WPT) transmitter.

When the channel width of M3 and M4 is increased, the g_m and the C_p are both increased. The mid-band gain A_0 increases when g_m is increased. However, Equations (1) and (2) show that increasing C_p causes the reduction in poles-frequency of the A(s), reduces the gain in higher frequency operation. Therefore, the sizes of the PA NMOS transistors need to be carefully optimized to obtain the highest gain in the desired frequency. Figure 3 shows the performance of the PA dependent on the channel width (W_{PA}) of M_3 and M_4. When W_{PA} = 6 µm, the PA achieves approximately 14 dB gain when consumes 9.6 mW power. When W_{PA} increases, the power consumption of PA is dramatically increased while the gain starts decreased at 200 GHz frequency operation.



Performance of the PA dependent on M_3 and M_4

M_3, M_4 channel width W (µm)	Gain at 200 GHz (dB)	PA power
6	14	9.6
12	13.3	12
18	12.4	32.6

Figure 3. The performance of power amplifier (PA) according to the channel width of M_3 and M_4.

To increase the delivered power (P_L) for the WPT, the output voltage swing on the PA need to be increased. When the PA has been optimized at the desired frequency operation, we can increase the PA output voltage swing by providing more power to the VCO. Higher power consumption on VCO provides a higher gate voltage driver on M_3 and M_4. Figure 4a shows the power consumption and output voltage swing of the VCO dependent on the channel width of M_1 and M_2. However, the PA performs the best efficiency with a limited range of the VCO output voltage swing. When the limitation voltage range has been reached, increasing the channel width of M_1 and M_2 only increases the power consumption but not improves the P_L. The maximum PTE of the proposed WPT is achieved when the channel width of M_1, M_2 is 15 μm, as shown in Figure 4b.

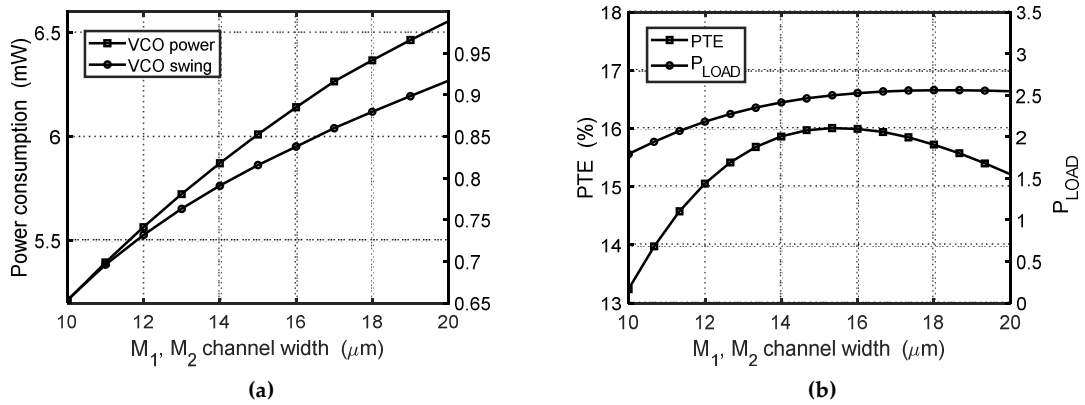


Figure 4. (**a**) Power consumption and output voltage swing of the voltage-controlled oscillator (VCO) according to the channel width of M_1 and M_2; (**b**) power transfer efficiency (PTE) and P_L of the proposed WPT according to the channel width of M_1, M_2.

2.2. The Proposed Sub-THz Receiver Design

The architecture and schematic of the sub-THz WPT RX are shown in Figure 5. The changing magnetic field produced on the L_1 generates a current flow in the primary coil of the receiver (L_2). The sub-THz rectifier converts the ac current signal to the dc voltage signal (V_{OUT}). The key task of designing a sub-THz WPT RX is to design a sub-THz rectifier with high power conversion efficiency (PCE).

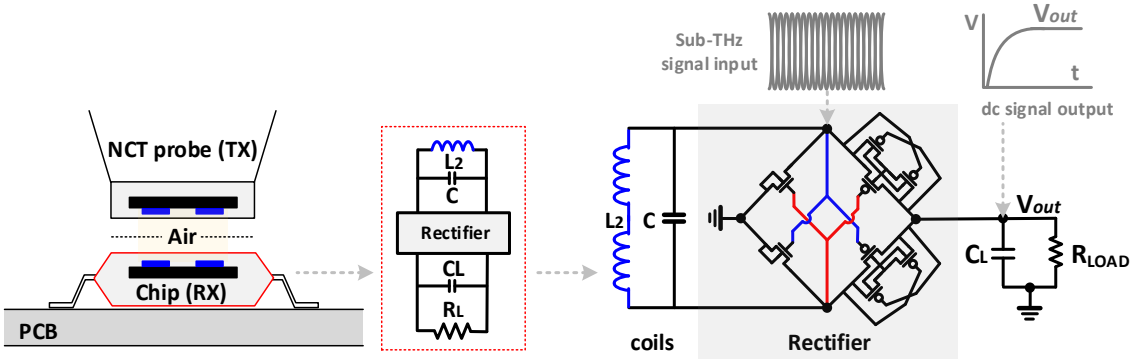


Figure 5. The architecture and schematic of the proposed sub-THz WPT receiver.

The PCE is calculated as what the percentage of ac power can be converted to dc output power. The most fundamental rectifier is a full bridge rectifier, which uses four Schottky diodes arranged in series pairs [20]. Each pair is active in each half cycle of the supply to convert the ac signal into the dc signal. However, due to the forward voltage drop on each Schottky diodes, this architecture performs very low PCE, especially when the ac input swing is low. There are state-of-the artworks

to overcome PCE limitations [6,21,22]. The [21] presented an NMOS cross-connected gate rectifier for the V_{TH} cancellation, leading to eliminate the voltage drop on the NMOS transistor. In [6], a SiP PMOS bridge rectifier was proposed, which uses two auxiliary PMOSs to connect the N-well to V_{OUT} or V_{IN}. This helps to control the body of the transistors by eliminating the substrate leakage and risk of latch-up. The [22] utilized an active NMOS rectifier with two integrated comparators and a cross-connected PMOS pair. When the cross-connection cancels the V_{TH} drop on the PMOS pairs, the comparators could provide a wide bias voltage swing for the NMOSs, leading to the better PCE when the ac input signal swing is small. However, at the sub-THz frequency operation, the PCE of prior works degrades significantly because of the increased parasitic capacitance of bulky NMOS and PMOS transistors of the rectifier.

As shown in Figure 6a, our proposed sub-THz rectifier utilizes the cross-connection to both NMOS (M_5, M_6) and PMOS (M_7, M_8) pairs to achieve the V_{TH} self-cancellation, which improve the PCE of the rectifier at sub-THz frequency range. Additionally, the body dynamic control topology is also employed on the PMOS pair. The inevitable trade-off between parasitic capacitance and transconductance of each transistor results in the compromise between frequency limitation and power conversion efficiency of the rectifier. The channel width of all the transistors in the rectifier should be less than 10 µm to reduce the parasitic capacitance, which dramatically decreases the sub-THz current signal on L_2. For the best PCE achievement, the channel width of the NMOS pair should be 6–10 times smaller than the channel width of the PMOS pair. Figure 6b shows the performance comparison among the proposed rectifier with the state-of-art rectifiers. Although the PCE of [22] (i.e., 84%) is higher than others [21,23] the PCE starts degrading in higher frequency and achieves 82 and 67.5% respectively at 13 MHz and 330 MHz. However, our proposed rectifier maintains the PCE up to 78% from low frequency to higher sub-THz frequency.

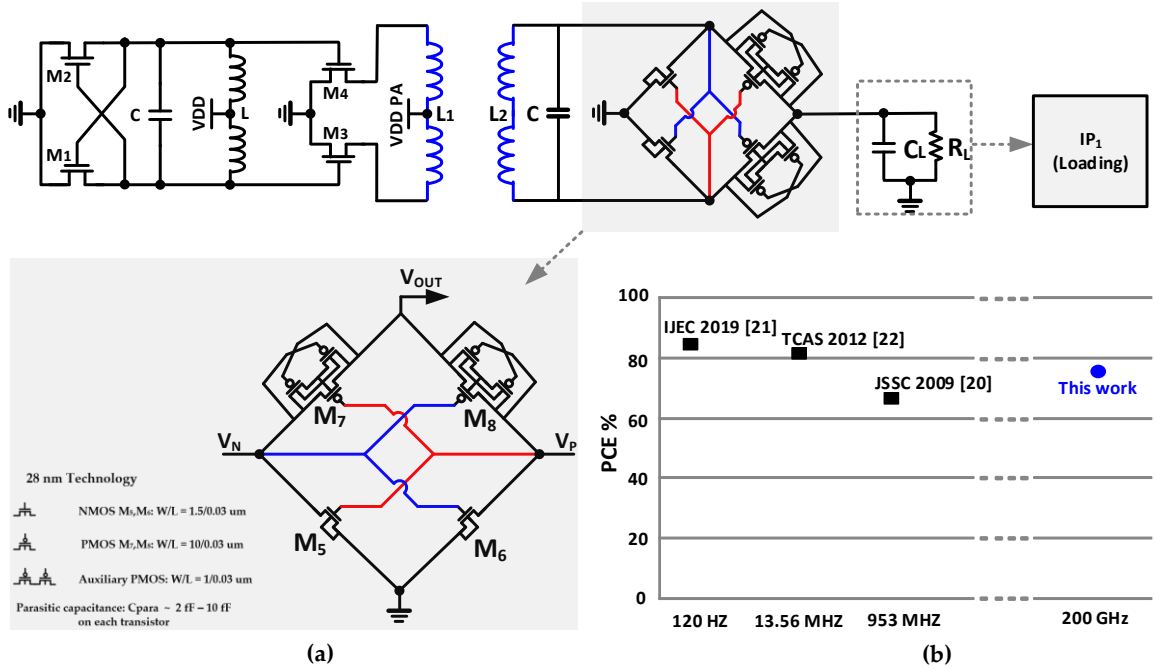


Figure 6. (**a**) The upgraded rectifier for the sub-THz frequency operation; (**b**) Performance comparison among the conventional rectifiers and the sub-THz rectifier.

2.3. The Proposed Sub-THz Coupling Coils Design

The on-chip sub-THz coupling inductors L_1 and L_2 are the most important components that influence the performance of the proposed sub-THz WPT. The coupling factor between L_1 and L_2 is the most critical factor that decides the power transfer efficiency (PTE) of the WPT [24–26]. The

quality factor of the on-chip inductors is limited by considerable parasitic resistance and capacitance. The parasitic resistance of L_1 on the TX chip must be as small as few Ohms to allow the maximum output power of the PA. The parasitic resistance of inductor L_2 on the RX chip should be relatively small, compared with the load and on-state resistance of the rectifier [27].

A typical inductor design process usually requires a 3-D electromagnetic (EM) field simulator such as HFSS. In this section, multiple case studies for the sub-THz coupling inductors (couplers) are presented. By using the HFSS EM simulator, the couplers have been designed and verified by the most accurate 3D EM model extraction for the sub-THz WPT PTE. Figure 7a shows an on-chip coupler for a conventional WPT [18], which operates at 300 MHz. The low-frequency inductor occupies a 0.49-mm^2 footprint, which is a huge area and not suitable for wafer-level testing in deep sub-micron technologies. Figure 7b shows the proposed on-chip sub-THz coupling inductors that are implemented on two silicon dies. To be designed for the 200 GHz frequency operation, the proposed coupler occupies only 0.0036 mm^2, which is 136 times smaller than the state-of-the-art NDT [13]. Therefore, the proposed WPT can significantly reduce the overall size of the non-contact wafer-level probes. Figure 8a shows the simulated quality factors Q_1 and Q_2 of the coupler, which are 16.7 and 15.2, respectively at 200 GHz frequency. Figure 8b shows the coupling factor (k) of the proposed WPT coupler with a 0.02-mm air gap distance. When the coupler operates at a higher frequency, k is higher. At the desired frequency operation (200 GHz), the coupling factor k = 0.6.

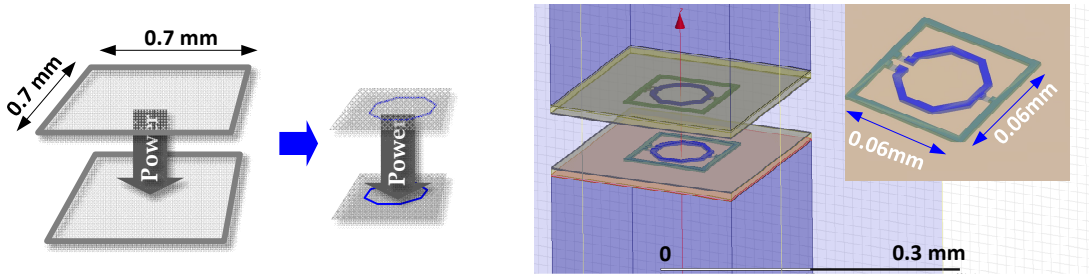


Figure 7. (**a**) A comparison between a conventional on-chip coupler and the proposed on-chip sub-THz coupler; (**b**) The proposed on-chip sub-THz coupler design.

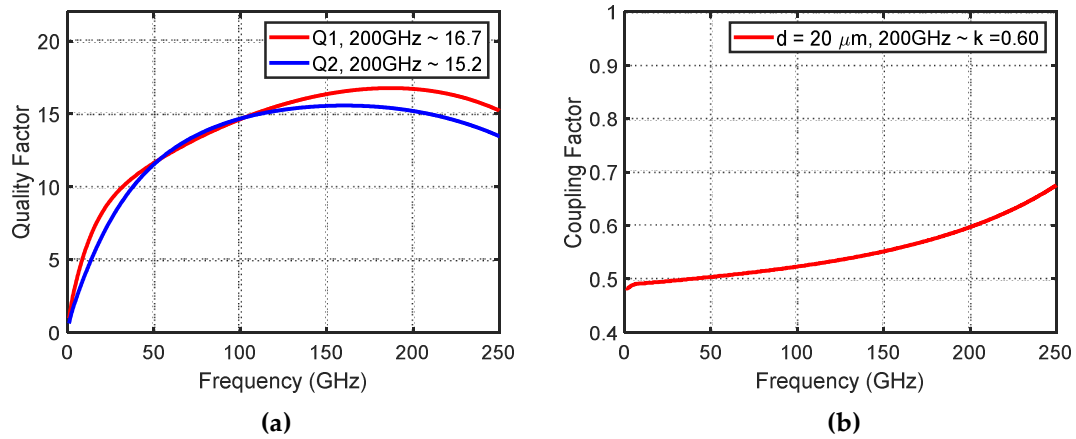


Figure 8. (**a**) Quality factors Q1 and Q2 of the proposed sub-THz coupler; (**b**) coupling factor of the proposed sub-THz coupler.

In the non-contact wafer-level testing, it is not always available to place the testing probe exactly alight with the DUT. Therefore, there are always an *offset distance* (Δ) and a *distance* (d) between the inductors of the sub-THz coupler. Those offsets yield a big impact on the coupling factor. To evaluate

the critical impacts on the coupling factor accurately, the key case studies are executed as shown in Figure 9. The k decreases from 0.6 to 0.36 when d increases from 20 to 50 µm and decreases from 0.6 to 0.25 when Δ increases from 0 to 20 µm. Therefore, in the proposed non-contact wafer-level testing system, any misalignment between the sub-THz NCT probe and DUTs causes a reduction for the k, leading to decreasing the PTE.

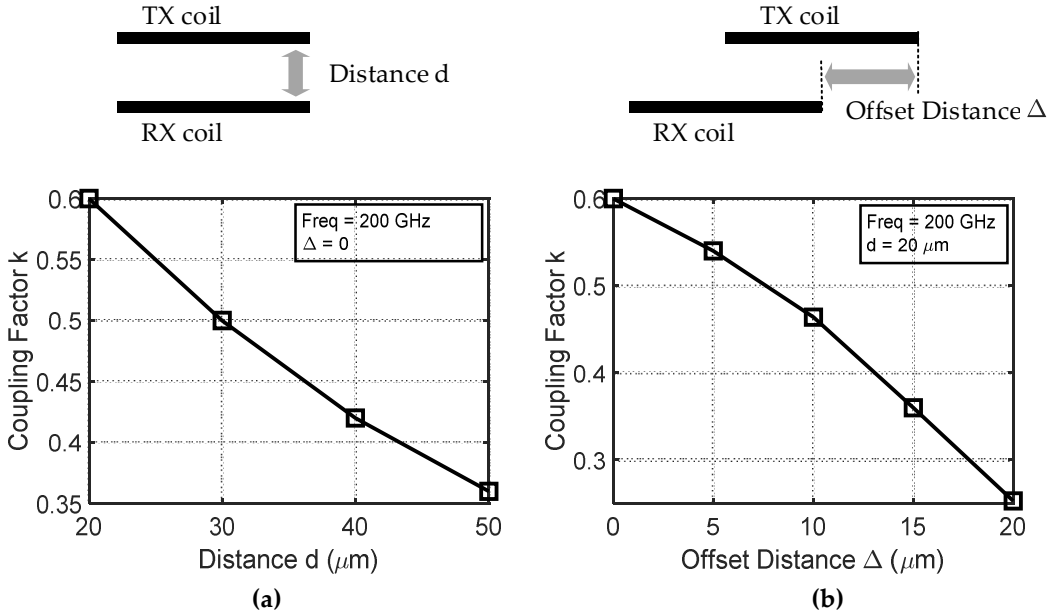


Figure 9. Simulation results of the proposed coupler at 200 GHz according to (**a**) various distance (d); (**b**) various offset distance (Δ).

An important specification of a WPT is the maximum power that it could provide to the load [28–30]. In the proposed sub-THz WPT, the maximum power transfer is limited by the specification of the sub-THz PA and rectifier (i.e., 200 GHz as 2.5 mW maximum). However, if multiple parallel channels are integrated into a single WPT, the desirable transfer power could be achieved while the total footprint remains much smaller than the conventional WPT (i.e., 8 channels as 20 mW, 0.04 mm^2). When higher PTE is required, the number of WPT channels could be simply increased along with the number of sub-THz couplers. Figure 10 shows a sub-THz multi-channel WPT system using a high-performance 8-channels coupler. On each chip die, 8 sub-THz inductors are arranged into a 2 × 4 rectangle. The total area of the 8-channels coupler is only 0.04 mm^2.

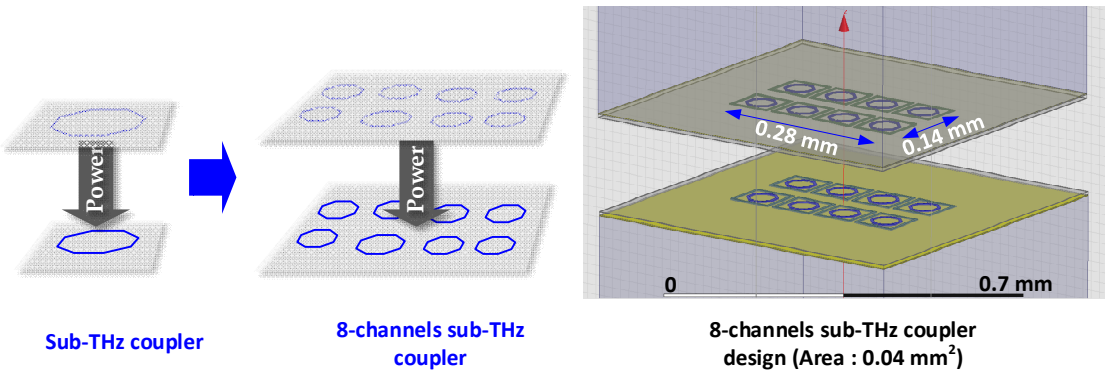


Figure 10. An 8-channels sub-THz coupler design.

2.4. The Proposed Sub-THz WPT Layout

The proposed sub-THz WPTs has been implemented in 28-nm CMOS technology. Figure 11a,b show the layout of the single-channel WPT transmitter and receiver, respectively. In the single-channel WPT, the coupling coils occupy a 0.0036 mm^2 area while the total chip area is 0.0072 mm^2 for TX and 0.0048 mm^2 for RX. Figure 11c,d show the layout of the 8-channels WPT where the total area of the coupler is 0.04 mm^2 for both TX and RX. In the 8-channels WPT, the sizes of the TX and the RX are still only 0.12 mm^2 and 0.098 mm^2 respectively.

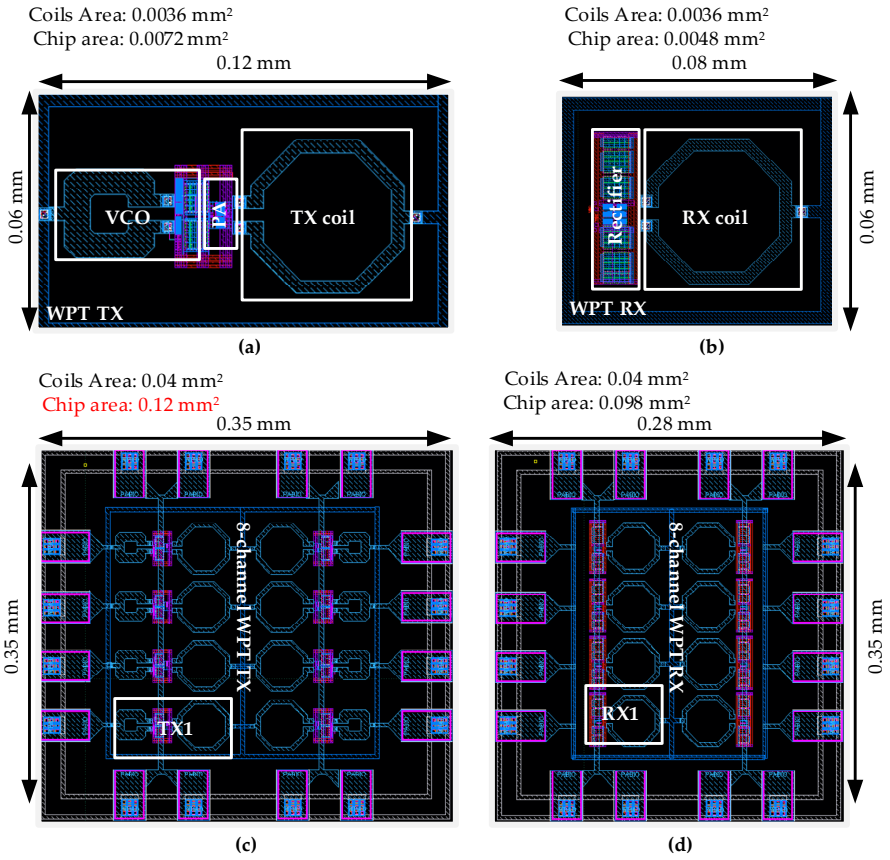


Figure 11. (**a**) Layout of the single-channel WPT TX; (**b**) Layout of the single-channel WPT RX; (**c**) Layout of the 8-channels WPT TX; (**d**) Layout of the 8-channels WPT RX.

3. Results

3.1. Simulation Results of a Single Channel Sub-THz WPT Interface

The post-layout-extracted simulation for a single channel WPT TX and RX is performed to evaluate the maximum and worst-case performance of the proposed WPTs. For an accurate WPT coupler modeling including wire bonds and parasitic capacitance, the 3-D EM solver tool (HFSS) is used to generate s-parameters. The worst-case simulated signal-flow (SS/0.9/100°) of the proposed single-channel sub-THz WPT at 200 GHz frequency operation is shown in Figure 12. The VCO consumes 6 mW power to generate a 200 GHz signal with 0.8 V voltage output swing as shown in Figure 12a. The PA is applied to magnify the signal amplitude to 3.9 V as shown in Figure 12b. The power consumption of the PA is 9.6 mW. The total power consumption of the single-channel WPT TX (P_{TX}) is 15.6 mW. Figure 12c shows the input voltage signal of the rectifier which has a 1.5 V ac output swing. When a 400 Ω load resistance is applied for the RX, the dc voltage output on the load is 1 V, as shown in Figure 12d. As a result, the power delivered to the load could be calculated as

$P_L = V_{OUT}^2/R_L$ = 2.5 mW. The PTE of the proposed single-channel WPT is P_L/P_{TX} = 16% at 200 GHz frequency operation.

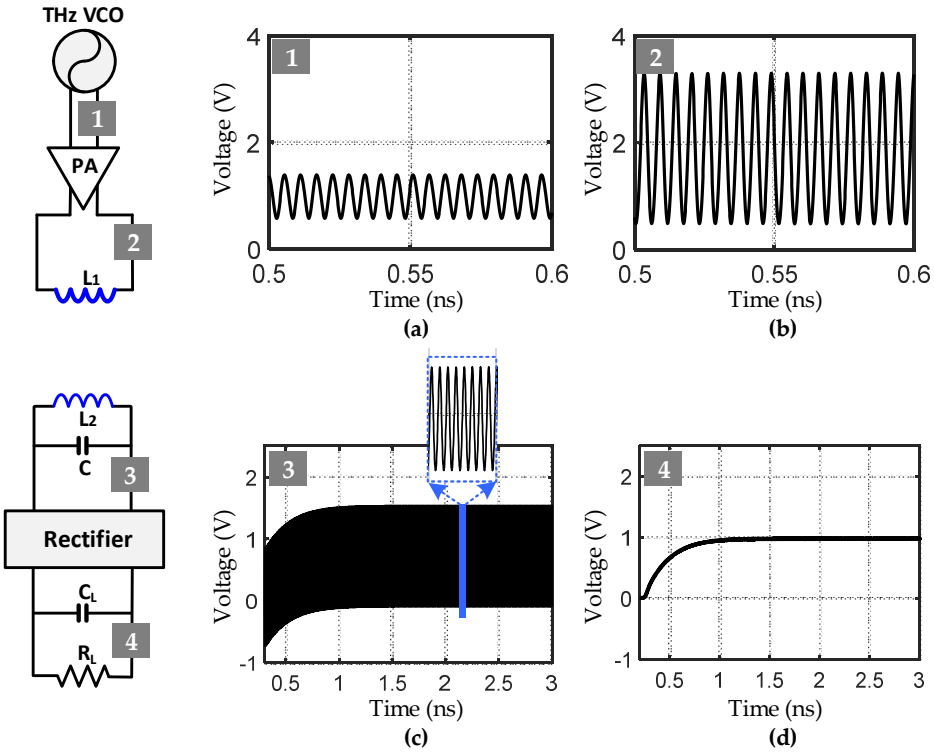


Figure 12. The simulated signal-follow of the proposed single-channel sub-THz WPT at *200* GHz frequency operation (SS/0.9/100°). (**a**) VCO output; (**b**) PA output; (**c**) rectifier input; (**d**) rectifier output (V_{OUT}).

The output voltage (V_{OUT}) and the power transfer of the proposed WPTs depend on the loading resistance value (R_L). Figure 13a shows the output voltage (V_{OUT}) when the R_L increases from 200 to 500 Ω. The V_{OUT} keeps increasing when the R_L increases. However, the maximum received power is 2.5 mW when the loading resistance R_L = 400 Ω, as shown in Figure 13b. This is because the performance of the proposed rectifier depends on the output loading condition. Therefore, with a specific power delivery requirement, the sub-THz rectifier should be carefully optimized for the best PTE achievement.

3.2. Simulation Results of a Multi-Channel Sub-THz WPT Interface

Based on the design of the single-channel WPT with the maximum PTE, the optimal multi-channel WPT has been designed, shown in Figure 14. The 8-channels sub-THz coupler is modeled by an N-ports with the s-parameter generated from the HFSS model to consider crosstalk between multiple channels. As the number of the WPT channels is added, the maximum overall power transfer efficiency could be significantly improved because the sub-THz WPT can provide enough space. To evaluate the power offset of the proposed WPTs depending on the process, voltage, and temperature (PVT) variation accurately, the Monte Carlo simulation has been performed for both single-channel and multi-channel cases. Figure 15 shows that the power transfer distortion is 0.77 mW and 6.9 mW at the 3-sigma of single-channel and multi-channel WPT, respectively. To achieve better power transfer for the proposed WPT, the accurate alignment between WPT coupling inductors is needed. In terms of multi-channel WPT case with the worst-case scenario, the max power mismatch is 6.9 mW. Therefore, when the proposed WPT provides the max power transfer for various intertextual properties (IPs)

such as bandgap, PLL/DLL, ADC, and PA/LNA blocks, the optimal number of WPT channels should be considered.

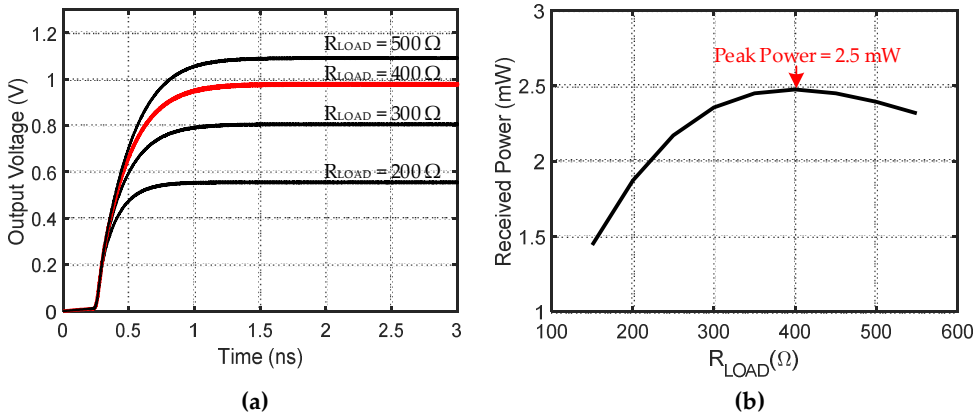


Figure 13. (**a**) The simulated output voltage V_{OUT} versus variation in R_L at 200 GHz (SS/0.9/100°). (**b**) The simulated output power P_L versus variation in R_L at 200 GHz.

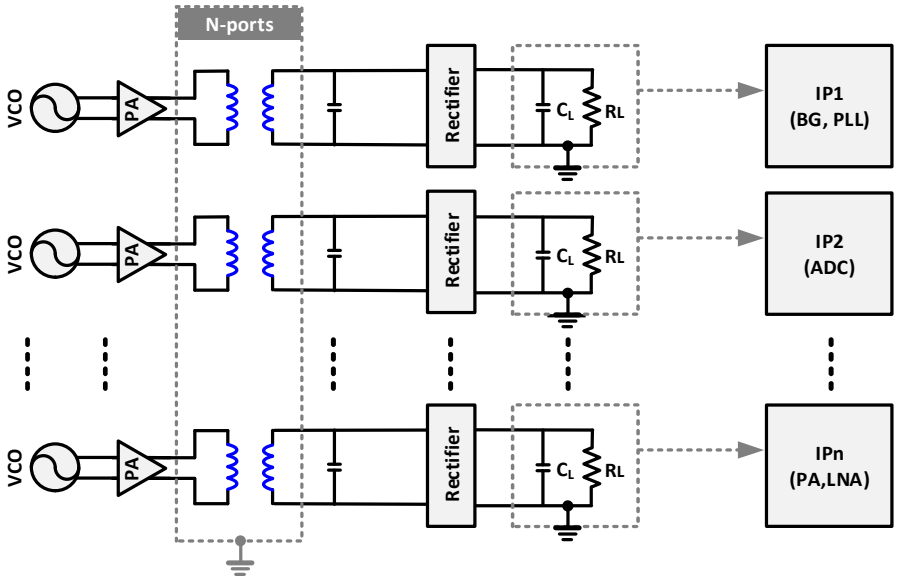


Figure 14. The architecture of the 8 parallel channels sub-THz WPT.

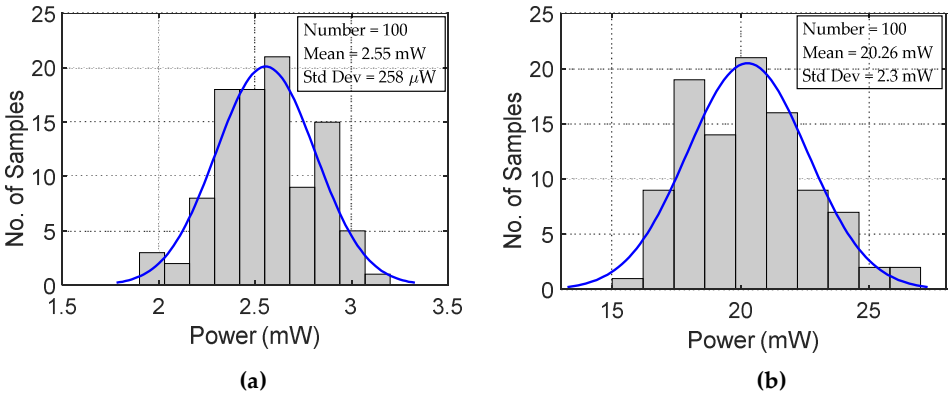


Figure 15. The Monte Carlo simulation results. (**a**) Power transferred of single-channel WPT; (**b**) Power transferred of 8-parallel channels WPT.

Table 1 shows the performance comparison of the prior works and the proposed work. To the best if the authors' knowledge, the proposed sub-THz WPT design has not been reported.

Table 1. Performance of the proposed sub-THz wireless power transfer.

	Unit	This Work	JSSC 2012 [18]	TBCS 2016 [13]	TMTT 2017 [14]	JSSC 2017 [15]	TIM 2017 [2]	TCAS 2018 [19]	TSWMCS 2019 [16]	TMTT 2020 [17]
Received Power, P_{RX}	mW	20	10	0.224	18	0.16	5.29	N/A	79.43	N/A
RX Area, A_{RX}	mm^2	0.098	0.49	1	25	9	0.87	0.45	36	33.6
TX Area, A_{TX}	mm^2	0.12	0.49	576	900	625	0.93	N/A	784	2500
Distance, d	mm	0.02	0.02	12	10	10	0.1	2.5	10	20
Efficiency, η	%	16	10	1.02	19.1	1.23	37.5	N/A	21	5.1
Carrier Frequency, f_c	GHz	200	0.3	0.2	0.0136	0.144	0.144	0.865	0.025	1.9
Supply Voltage, V_{DD}	V	1.0/1.8 *	1.2	N/A	2	1.5	1.9	N/A	N/A	N/A
CMOS Technology	nm	28	350	N/A	180	180	180	180	65	N/A

* 28 nm: two devices used (standard CMOS: 1V, I/O device: 1.8V for PA)

The conventional WPTs shown in Table 1 are designed for two practical applications. The biomedical related WPTs [13–17] could transfer the power through a greater distance with a very large TX chip size. The wafer-level testing related WPTs [2,18,19] performs the power delivery in a much shorter distance, but the TX chip area is much smaller. When the trade-off between the TX chip size and the delivered distance is eliminated, small RX chip size and maximum power delivery are the most critical factors required for both biomedical WPTs and wafer-level testing WPTs. The proposed WPT RX chip occupies only 0.098 mm^2 area (5 times smaller than the smallest one [19]). The maximum power delivery of the proposed WPT is 20 mW (only [16] could provide 4 times more power, but the RX chip size is 367 times larger). To be designed for the wafer-level testing applications, the proposed WPT could significantly reduce the chip size and improve power delivery. Therefore, more DUTs on a single wafer could be tested at the same time, the testing speed could be improved.

4. Conclusions

In this paper, we presented a sub-THz wireless power transfer interface for non-contact wafer-level testing. Multiple case studies of the sub-THz WPTs have been designed in a 28-nm CMOS RF process. To enhance the PTE, the PA has been designed and analyzed to obtain the highest gain at 200 GHz frequency operation. The VCO has been well designed for reasonable output voltage range, allowing the best performance operation of the PA. From the advance rectifier design techniques that have been reported, the upgraded rectifier could achieve 78% PCE at the desired sub-THz frequency operation. The simulated proposed single-channel WPT could transfer 2.5 mW power to the load with the PTE of 16%. To enhance the power delivery, the 8-channels sub-THz WPT has been simulated, which could provide up to 20 mW power to the DUT while the total chip size is only 0.12 mm^2 and 0.098 mm^2 for TX and RX, respectively.

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