

Review

Junctionless Transistors: State-of-the-Art

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Abstract: Recent advances in semiconductor technology provide us with the resources to explore alternative methods for fabricating transistors with the goal of further reducing their sizes to increase transistor density and enhance performance. Conventional transistors use semiconductor junctions; they are formed by doping atoms on the silicon substrate that makes p-type and n-type regions. Decreasing the size of such transistors means that the junctions will get closer, which becomes very challenging when the size is reduced to the lower end of the nanometer scale due to the requirement of extremely high gradients in doping concentration. One of the most promising solutions to overcome this issue is realizing junctionless transistors. The first junctionless device was fabricated in 2010 and, since then, many other transistors of this kind (such as FinFET, Gate-All-Around, Thin Film) have been proposed and investigated. All of these semiconductor devices are characterized by junctionless structures, but they differ from each other when considering the influence of technological parameters on their performance. The aim of this review paper is to provide a simple but complete analysis of junctionless transistors, which have been proposed in the last decade. In this work, junctionless transistors are classified based on their geometrical structures, analytical model, and electrical characteristics. Finally, we used figure of merits, such as I_{on}/I_{off} , $DIBL$, and SS , to highlight the advantages and disadvantages of each junctionless transistor category.

Keywords: junctionless; transistor; nanowire; double gate; planar; gate-all-around; FinFET; thin film; tunnel

1. Introduction

The concept of junctionless transistor (JLT) was introduced by J. E. Lilienfeld in the 1920s [1]. The main feature of this device is the absence of any pn junction; hence, the requirement of doping concentration gradients is avoided. It simplifies the fabrication process of the transistors with sizes below 10 nm. There are two main requirements to realize JLTs. First, the transistor channel must be highly doped ($\sim 1 \times 10^{19} \text{ cm}^{-3}$). Second, the channel thickness has to be in the nanometer scale ($\sim 10 \text{ nm}$). Due to the limitations in the microfabrication technology, it took more than 80 years to realize the first junctionless transistor. The first successfully fabricated JLT was a junctionless nanowire (NW), which was realized at the Tyndall Institute by Colinge et al. [2]. This device turned out to be the first one of a new generation of transistors. In the last decades, many other junctionless devices were proposed, which includes FinFET [3–23], Gate-All-Around (GAA) [24–37], Single Gate (SGJLT) [38–50], Double Gate (DGJLT) [51–75], Thin Film (TFT) [76–86], and Tunnel FET (TFET) [87–97]. Because most of the review papers on JLTs were published in 2010–2014 [98–102], a complete overview on the basis of the latest developments is missing. Therefore, in this paper, we provide a critical analysis of JLTs in terms of structure and performance comparison.

2. Classification

Junctionless transistors can be divided in two main categories: depletion-based and tunnel-based JLTs. In depletion-based devices, the amount of electrical current flowing through the device depends on the dimension of the depletion region, which is controlled by the applied gate voltage. In tunnel-based devices, the electrical current is governed by band-to-band tunneling (BTBT). JLT categories can be then classified based on the geometrical shape, material composition of the channel, as well as the gate structure. When a single gate on the top of the channel controls the current through the device, it is known as Single Gate junctionless transistor. If an additional gate is present below the channel, then it is called Double Gate junctionless transistor. If the transistor channel thickness is very thin (≤ 10 nm) and the channel material is not monocrystalline silicon, then it is known as Thin Film junctionless transistor. Gate-All-Around JLTs are characterized by a gate electrode that entirely surrounds the channel of the transistor; the channel can be either cylindrical or rectangular. When the transistor channel is a tube-shaped nanostructure, it is called junctionless Nanowire. If the electronic device is a fin-shaped transistor, it is called junctionless FinFET. This simple classification is coherent with the analyzed literature, whose distribution is shown in Figure 1. Although most of the reported junctionless transistors are inorganic electronic devices, organic solutions were also proposed [103–108]. In this work, we focus on inorganic junctionless transistors, where the following parameters are considered as the main figures of merit: the Drain-Induced Barrier Lowering (DIBL), which represents the drain voltage influence on the threshold voltage, defined as $DIBL = |\Delta V_{th}|/|\Delta V_{ds}|$ [109]; the Subthreshold Swing (SS), which can be defined as the change in the gate voltage required to decrease the drain current by one decade ($SS = dV_{gs}/d\log(I_d)$) [110]; the I_{on}/I_{off} ratio, which is the ratio between the maximum available drain current, I_{on} ($V_{gs} = V_{dd}$, $V_{ds} = V_{dd}$), and the current in the off state, I_{off} ($V_{gs} = 0V$, $V_{ds} = V_{dd}$).

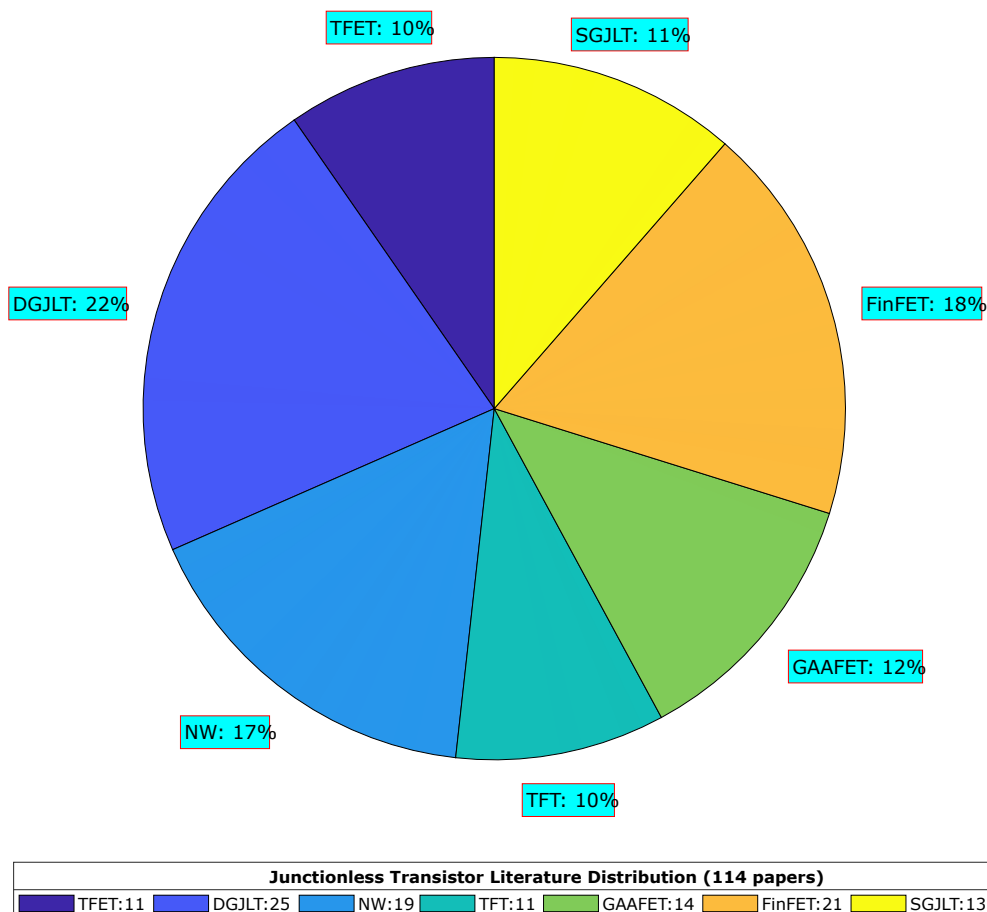


Figure 1. Junctionless transistor literature distribution analyzed in this work.

3. Analysis

3.1. The First Junctionless Transistor

In 2010, J. P. Colinge et al., fabricated the first junctionless transistor (Figure 2) in the form of a nanowire characterized by a silicon thickness of 10 nm and a channel length of 1 μm [2]. The process requires uniform and heavy doping ($\geq 1 \times 10^{19} \text{ cm}^{-3}$) of the nanowire in order to ensure the correct operation of the device [111]. The nanowire transistor was realized over a SOI (Silicon on Insulator) wafer and patterned by electron-beam lithography.

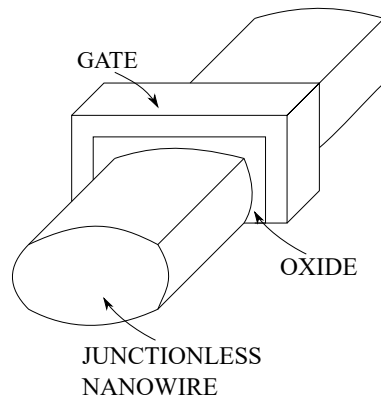


Figure 2. Structure of the junctionless nanowire.

Junctionless NWs do not work in inversion mode (IM) like conventional MOSFETs. The threshold voltage is defined as the gate voltage that fully depletes (*OFF* state) the device layer (Figure 3c) [112,113]. Thus, the *OFF* state definition is more similar to that of accumulation mode (AM) devices (Figure 3b); also from an analytical point of view, they can be modelled from AM device descriptions, since the current flowing in the device can be decomposed into two components: a bulk and an accumulation current [114,115]. When the gate voltage is greater (in absolute value) than the threshold voltage, partial depletion takes place creating a path in the substrate for the bulk current. When the gate voltage reaches the flat band voltage, the whole channel becomes conductive (*ON* state), and an accumulation current starts to form at the semiconductor/insulator interface [112].

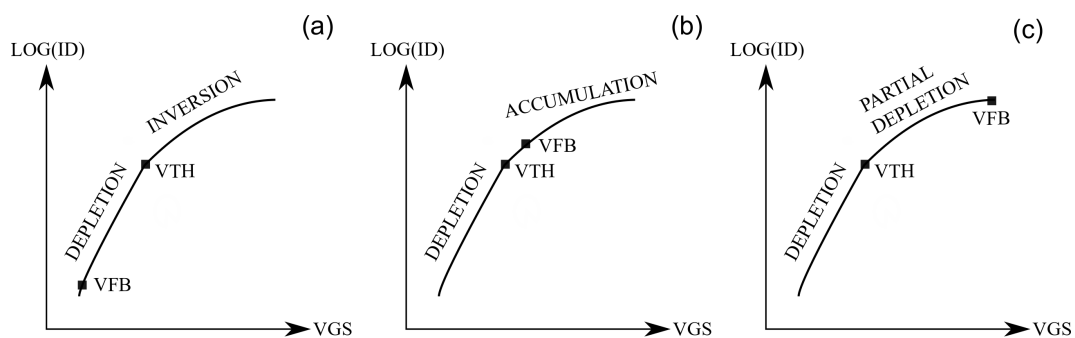


Figure 3. Current behavior in (a) inversion mode (IM), (b) accumulation mode (AM), and (c) junctionless transistors.

The threshold and flat band voltages are of critical importance, since they determine the operating range of the device [2]. The threshold voltage can be extracted as the gate voltage at which the curve g_m / I_D (where g_m is the transconductance) drops to half of its maximum value [116]. It increases (in absolute value) with increasing doping, while decreasing with increasing gate oxide thickness, nanowire width, and length [117]. An analysis of the doping concentration influence on the threshold voltage is also reported in [118]: by increasing the doping concentration from $1 \times 10^{14} \text{ cm}^{-3}$ to

$1 \times 10^{18} \text{ cm}^{-3}$, the threshold voltage decreases from 0.455 V to 0.37 V; this could be attributed to the fact that, for high doping concentration, more carriers are available for the same gate voltage. An interesting characteristic of the flat band voltage is the dependency on the temperature. A detailed analysis of this parameter is presented in [119,120], in which it is shown that the flat band voltage decreases as the temperature increases. For low temperature (4.2 K) and high doping concentration ($1 \times 10^{19} \text{ cm}^{-3}$), the thermal energy is not strong enough to ionize all of the dopants. This results in an incomplete ionization that causes the series resistance to increase (Figure 4) and the drain current to decrease.

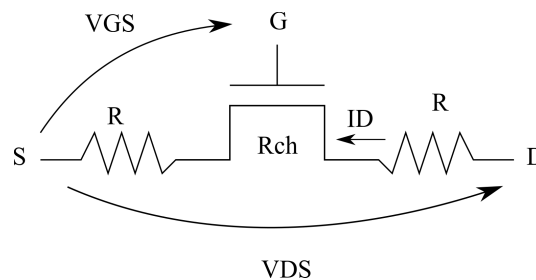


Figure 4. Junctionless nanowire resistance model representation.

As reported in [121], junctionless nanowire transistors present a reduction of short channel effects as compared to inversion mode devices, but they are highly sensitive to the series resistance. The simulation of junctionless NWs with channel length of 100 nm and doping concentration of $1 \times 10^{19} \text{ cm}^{-3}$ provided an intrinsic source/drain resistance of 5.5 k Ω . By decreasing the doping to $5 \times 10^{18} \text{ cm}^{-3}$, the resistance reached a value of 11 k Ω . The performance of junctionless nanowire transistors can also be affected by current leakages that are associated to gate tunneling. The latter phenomenon is directly proportional to the length and width of the transistor (so to the gate surface area), and to the temperature [122,123].

Because the current in junctionless transistors flows far from the gate oxide/channel interface, the mobility degradation is minimized. This is one of the main advantages of depletion-based junctionless transistors with respect to the conventional ones [124]. Enhanced mobility in junctionless NWs was also attributed to the reduction of the scattered impurities that are caused by an overall smaller charge of ionized impurities [125]. Junctionless NWs were also investigated in terms of crystal orientations and material channel (germanium and silicon) and compared to inversion mode devices; the junctionless NW found to be less sensitive to short channel effects, presenting smaller *SS*, reduced *DIBL*, and higher I_{on}/I_{off} than inversion mode transistors. As compared to silicon JLTs, germanium junctionless NWs were observed to be slightly more sensitive to short channel effects, but more competitive from an electrostatic control point of view [126–128].

3.2. Gate-All-Around

Figure 5 shows a schematic of a cylindrical junctionless Gate-All-Around transistor. The device, as the name suggests, is characterized by a channel entirely surrounded by the gate. The channel geometry determines the complexity of the equations that are needed to model the device behavior. In this case, the solutions to the Poisson equations are more complex, since cylindrical coordinates have to be introduced [26,31]. Additionally, GAAFETs with rectangular channels are reported, but they suffer from performance degradation due to corners effects [25]. An important parameter in the design of GAAFETs is the channel length. For a channel length reduction from 40 nm to 16 nm, the *DIBL* increases from 12 mV/V to 123 mV/V, while the *SS* increases from 62 mV/dec to 82 mV/dec [29]. The channel radius determines the device speed; lower radius corresponds to faster operation [26].

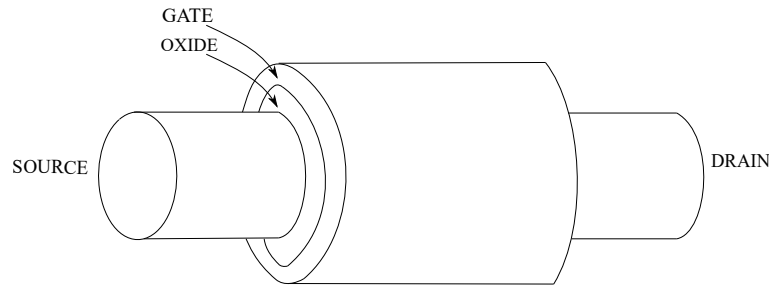


Figure 5. Three-dimensional (3D) structure of a cylindrical junctionless GAAFET.

With respect to inversion mode devices, junctionless GAAFETs generally present higher I_{on}/I_{off} ratio and less short channel effects [25,30]. Regarding the low-frequency noise (LFN) behavior, junctionless GAAFET is almost not sensitive to gate bias and doping concentration variations [28]. Instead, the intrinsic gain and cutoff frequency were observed to be degraded by the hot carrier effect; a relative degradation of 15.44% for both of the analog parameters was reported [32]. The designer could improve the analog performance (small signal parameters and drain current drivability) by adding source and drain extensions, as shown in Figure 6 [24]. The structure that is depicted in Figure 5 can be further modified in order to increase the device performance. For example, a gate insulator made of hafnium oxide (HfO_2) instead of silicon oxide (SiO_2) can enhance the *DIBL* and the *SS* [27].

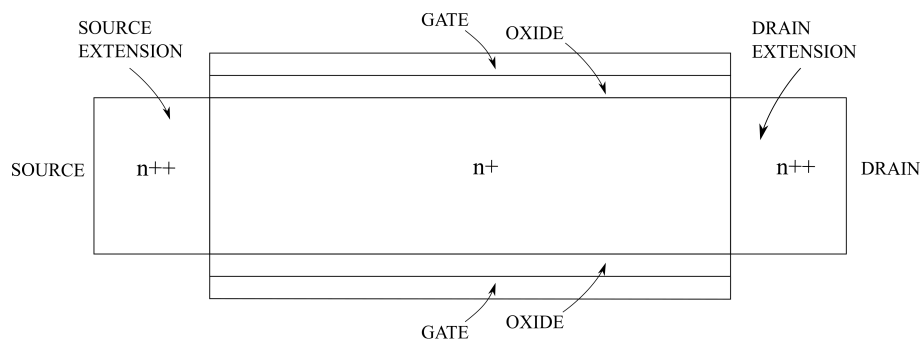


Figure 6. Cross-sectional view of improved cylindrical GAAFET through addition of source and drain extensions.

Apart from engineering the gate oxide structures, the designer could also increase the number of gates. If two gates are present, the structure is defined as a twin gate transistor (Figure 7). Such a structure allows implementing logic gates easily since two inputs are present [34]. The twin gate structure can also be applied to a double channel GAAFET, as shown in Figure 7b. A fabricated twin gate double channel GAAFET showed an I_{on}/I_{off} ratio of 7×10^8 , a *DIBL* of 83 mV/V, and a *SS* of 105 mV/dec [33]. Besides silicon and polysilicon channel junctionless GAAFETs, devices composed of other materials were also reported: a gallium arsenide junctionless GAAFET was simulated, leading a *SS* value near to the theoretical limit (58.2 mV/dec at 293.15 K) [27]. A germanium junctionless GAAFETs was compared to a silicon one, and it provided lower *DIBL*, *SS* and I_{on}/I_{off} ratio (data in Table 1) [35]. The channel material composition also influences the threshold voltage sensitivity to the temperature: considering silicon, gallium arsenide, indium arsenide, and indium phosphide, the minimum and maximum threshold voltage variations were observed for indium arsenide and silicon, respectively [37].

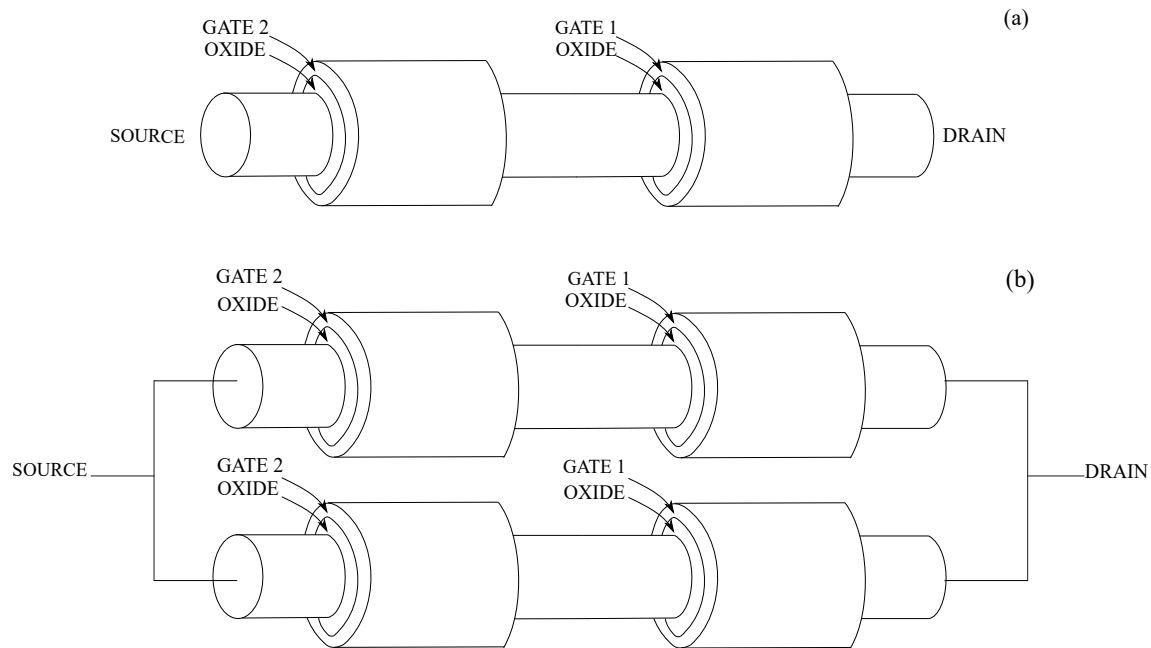


Figure 7. 3D Structure of (a) twin gate single channel GAAFET, (b) twin gate double channel GAAFET.

It is possible to use strain technology in order to further increase the device performance; a layer of SiN is deposited and, depending on the deposition conditions, the strain could be compressive or tensile [36]. The figures of merit of reported junctionless GAAFETs are presented in Table 1.

Table 1. Reported figure of merits of junctionless GAAFETs. L_{ch} and W_{ch} are the channel length and width, respectively.

GAAFET	L_{ch} (nm)	W_{ch} (nm)	N_D (cm^{-3})	SS (mV/dec)	DIBL (mV/V)	I_{on}/I_{off}	Ref.	Year
Si	-	21	1.5×10^{19}	70	35	$>10^6$	[25]	2013
Si	20	10	2×10^{19}	70.94	60.40	4.3×10^5	[35]	2014
Ge	20	10	2×10^{19}	67.88	39.6	5×10^5	[35]	2014
PolySi	20	45	-	105	83	7×10^8	[33]	2015
Si (tensile)	-	20	-	65	-	$>10^9$	[36]	2016

3.3. FinFET

Figure 8a shows a schematic of a bulk junctionless FinFET. The device can also be fabricated on the top of an insulator layer, as shown in Figure 8b. In that case we define it as an SOI FinFET. Dimensions of these transistors strongly affect their performance. Considering bulk junctionless FinFETs, increasing the fin width (W) from 6 nm to 15 nm can lead to a variation of approximately 60% and 42% for $DIBL$ and SS , respectively; changing the gate length (L_G) from 12 nm to 21 nm can lead to a variation of approximately 52% for $DIBL$ and 14% for SS [12]. Variations in the fin height (H) are more critical in terms of analog performance [19]. With respect to the inversion mode device, the junctionless FinFET presents lower I_{off} . This is attributed to the low carrier concentration and high electric field in the middle of the channel in the *OFF* state. As compared to SOI FinFETs, the bulk structure presents an additional degree of freedom in the design: by varying the doping concentration of the substrate from $1 \times 10^{18} \text{ cm}^{-3}$ to $1 \times 10^{19} \text{ cm}^{-3}$, a change of 30% in the threshold voltage can be obtained [4]. Furthermore, it also provides lower SS and $DIBL$. From an analytical point of view, it can be modeled from conventional triple gate (TG) structures [3,20]. An alternative structure is the so-called SON (Silicon On Nothing). In this structure, the silicon layer is isolated from the substrate

through a selective etching. This design choice implies a more complex fabrication process with respect to the bulk structure [5].

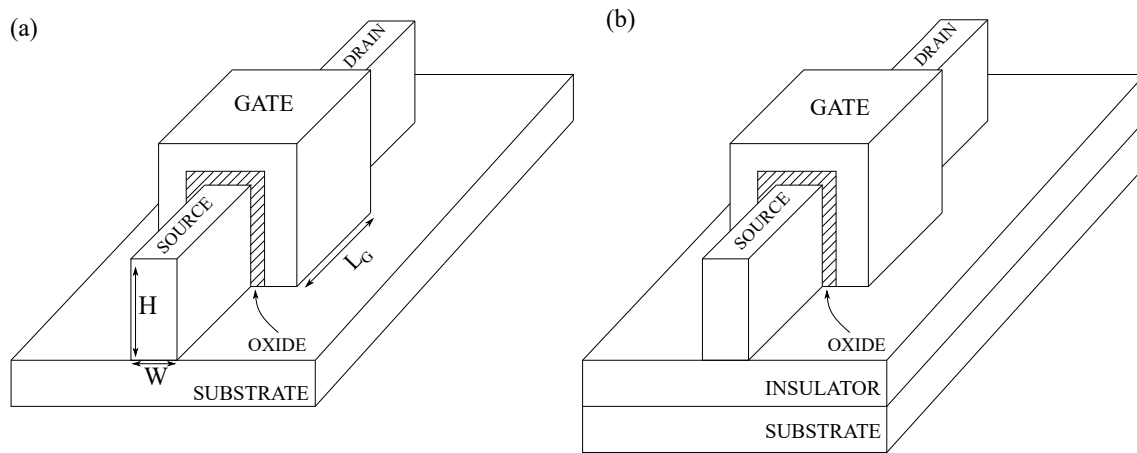


Figure 8. 3D FinFET structure: (a) bulk, (b) SOI.

The designer could follow different approaches in order to optimize junctionless FinFETs: work function engineering of the gate to reduce I_{off} (by changing the gate work function from 4.5 eV to 5.4 eV, I_{off} can be reduced by five order of magnitudes) [7]; spacer engineering to improve performance (e.g., dual-k spacers architecture can provide an improvement in I_{on} by 72.5% and in $DIBL$ by 37.8%) [9]; doping engineering by using a Gaussian doped channel, which can lead to an increase in I_{on} by 21.1% [10,13], or a lightly doped channel, which allows for better gate control on the device [11]; gate oxide engineering to provide higher performance (in terms of I_{on}/I_{off} and $DIBL$) by the implementation of complex hetero gate oxide structures [8]. For example, the double hetero gate oxide (DHGO) presented in Figure 9 can obtain a higher I_{on}/I_{off} with respect to conventional and triple/quadruple hetero gate oxide (THGO/QHGO) structures.

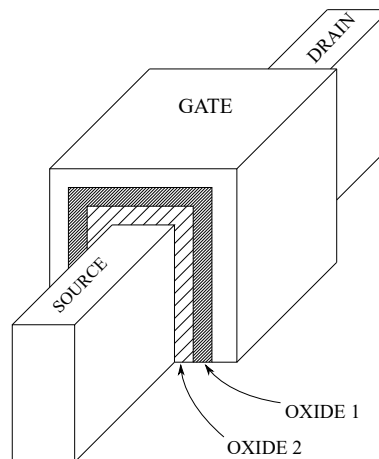


Figure 9. 3D double hetero gate oxide FinFET structure.

Besides the number of hetero gate oxides regions, it is also important to consider their dielectric constant value: for high values ($k = 40$) the $DIBL$ is reduced and the analog performance is degraded [14]. Instead, dual-k structures with intermediate values of the dielectric constant ($k = 22$, HfO_2) provide better performance with respect to those with low dielectric constant ($k = 3.9$, SiO_2) when considering random dopant fluctuation in the fin [16]. The latter is a critical phenomenon, especially for junctionless FinFETs, since they are more likely to be affected by random dopant variability [17]. Moreover, random dopant fluctuations and work function variability are considered to be more dominant with device dimension scaling [18]. It is important to note that the results reported

for the junctionless FinFETs do not necessarily hold for the other junctionless transistors: for instance, the threshold voltage of junctionless FinFETs is more sensitive against work function variations as compared to that of junctionless GAAFETs [15].

FinFETs were analyzed by considering different materials for the device layer. A FinFET made of polycrystalline silicon is reported as a cost-effective solution with respect to silicon devices [22]. A GaAs FinFET with I_{off} of $1 \times 10^{-15} A$ compared to a silicon FinFET with an I_{off} of $1 \times 10^{-8} A$ was proposed. The better performance was attributed to the higher depletion of carriers when the device is in the OFF state [21]. More complex structures were reported: InGaAs junctionless FinFET with alloyed Ni-InGaAs source and drain [23]. Table 2 presents the main figure of merits of the reported FinFETs.

Table 2. Reported figure of merits of junctionless FinFETs. EOT is the equivalent gate oxide thickness, while k is the gate oxide dielectric constant.

FinFET	L_G (nm)	H (nm)	EOT (nm)	N_D (cm^{-3})	SS (mV/dec)	$DIBL$ (mV/V)	I_{on}/I_{off}	Ref.	Year
Bulk (HfO_2 , $k = 22$)	15	10	1	1.5×10^{19}	73.1	40.4	1×10^5	[6]	2013
SOI (HfO_2 , $k = 22$)	15	10	1	1.5×10^{19}	84.1	119.2	-	[6]	2013
Bulk	15	10	1	1.5×10^{19}	-	-	2.9×10^7	[7]	2014
Bulk (HfO_2 , $k = 22$)	15	10	1	1×10^{18}	78.27	95.48	-	[5]	2017
SOI (HfO_2 , $k = 22$)	15	10	1	1×10^{18}	87.3	121.65	-	[5]	2017
SON (HfO_2 , $k = 22$)	15	10	1	1×10^{18}	63.2	82.68	1×10^5	[5]	2017
SOI (SiO_2 , $k = 3.9$)	5	6	1	1×10^{19}	61.5	20	-	[14]	2017
SOI (TiO_2 , $k = 40$)	5	6	1	1×10^{19}	63.3	12.5	-	[14]	2017
Single (SiO_2 , $k = 3.9$)	13	6.4	0.64	1×10^{19}	66.659	23	$\sim 1.3 \times 10^8$	[16]	2017
Dual ($k = [3.9, 22]$)	13	6.4	0.64	1×10^{19}	64.959	11	$\sim 2.7 \times 10^8$	[16]	2017
InGaAs	60	28	2.1	1×10^{19}	96	106	5×10^5	[23]	2018
w/o HGO ($k = 3.9$)	14	5	1.5	5×10^{19}	70	52	1×10^9	[8]	2019
DHGO ($k = 22$)	14	5	1.5	5×10^{19}	64	20	4.13×10^{12}	[8]	2019
THGO ($k = 9$)	14	5	1.5	5×10^{19}	64	20	2.08×10^{12}	[8]	2019
QHGO ($k = 7.5$)	14	5	1.5	5×10^{19}	64	20	2.7×10^{11}	[8]	2019

3.4. Single Gate

The single gate junctionless transistor presents two types of structures, i.e. bulk and SOI, as shown in Figure 10. The bulk structure provides more control on the device characteristics because of the possibility to dope and bias the bulk well [38]. When considering an n-type JLT with p-type bulk, it is possible to improve the hot carrier effect, thus reducing the I_{off} current by positively biasing the well. On the other hand, by increasing the bulk bias, the threshold voltage can be decreased while increasing $DIBL$ and SS . The degradation is even more relevant if the channel length is below 20 nm [40]. If the substrate doping concentration is high, then the I_{off} current is minimized [44]. Moreover, it has to be considered that bulk junctionless transistors present reduced effective thickness, as compared to SOI; if a bulk SGJLT has a physical thickness of 10 nm, the effective thickness is 5 nm, because of the built-in junction potential [38]. With respect to the SOI structure, the bulk SGJLT presents improved analog performance: improved output transconductance, output resistance, Early voltage, and intrinsic gain [39]. When compared to junction transistors, the junctionless ones were observed to be more sensitive to the T_{Si}/W_{Si} ratio, and to provide a lower I_{on} . This is attributed to the highly doped channel, which increases the scattering effect, thus lowering the mobility [42].

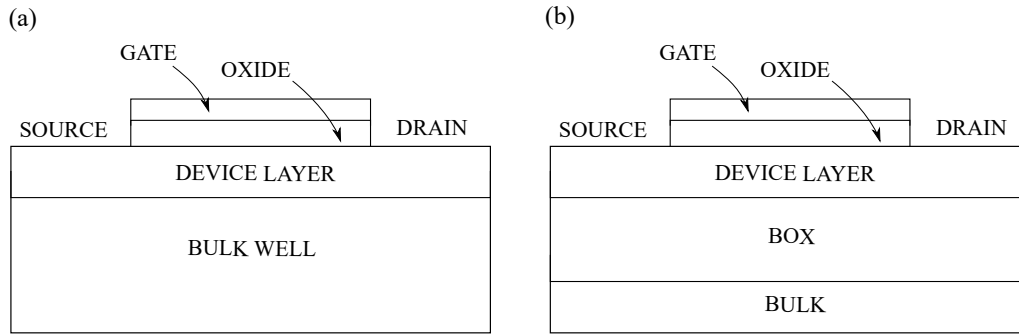


Figure 10. Cross-sectional view of a single gate junctionless transistor: (a) bulk, (b) SOI.

More options are available to the designers in order to optimize the SGJLT; gate work function engineering can lead to an improvement of 29% in the I_{on}/I_{off} ratio [41], while a non-uniform (Gaussian) doping concentration through the device layer can reduce the I_{off} [43].

As for FinFETs and GAAFETs, an improvement of the electrostatic characteristics of the transistor can be obtained by implementing high-k spacers, as shown in Figure 11a. The high-k spacers enhance the fringing electric fields; as a result the device is depleted not only below the gate but also laterally. This implies an increment of the effective channel length, which, in terms, improves the SS [45]. Designers can also enhance the transistor mobility and currents through S/D engineering and dual-k spacers structures [46,47].

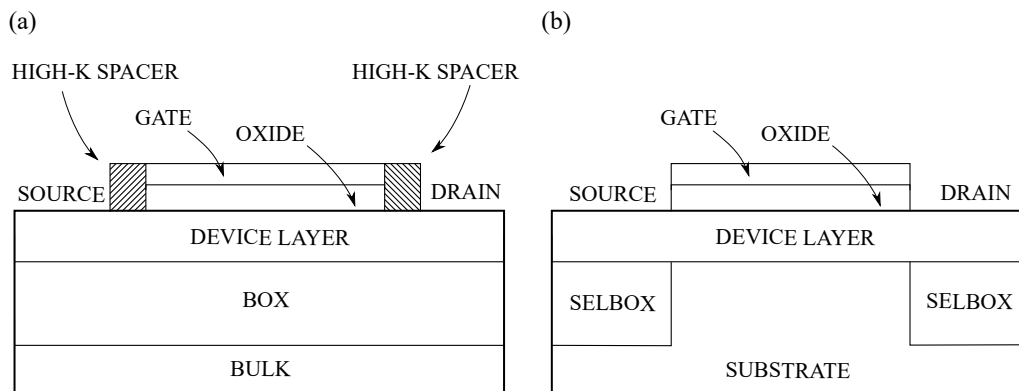


Figure 11. Cross-sectional view of: (a) Single Gate junctionless transistor (SGJLT) with high-k spacers. (b) SGJLT with SELBOX.

A variant of the conventional SOI structure is the SELBOX (selective buried oxide), as shown in Figure 11b. This oxide configuration improves the transistor thermal isolation, allowing for an increment for the I_{on}/I_{off} of 6 orders of magnitude (from 2.31×10^3 to 1.5×10^9) [48]. Moreover, the SELBOX architecture increases the gate control on the device, since a pn junction is formed between the highly doped channel and the substrate. The junction enhances the device layer depletion. Designers could also add a metal layer on the top of the BOX layer. This enables the formation of a Schottky junction that could help to fully deplete the transistor in the OFF state [50]. Regarding leakages in junctionless transistors, one of the most critical cause is associated to the parasitic BJT (bipolar junction transistor), as depicted in Figure 12. As electrons tunnel from the valence band to the conduction band (band-to-band-tunneling), they leave holes in the channel that can raise its potential. This phenomenon triggers a parasitic BJT between the source, the channel, and the drain in the OFF state [49].

The holes that accumulated in the floating body of the channel can cause a forward bias of the junction associated to the source/channel regions; if this bias turns on the parasitic BJT, then a large leakage current is observed. A possible solution is to employ thin film transistors (Section 3.6), which can reduce the band-to-band-tunneling and, therefore the associated leakage.

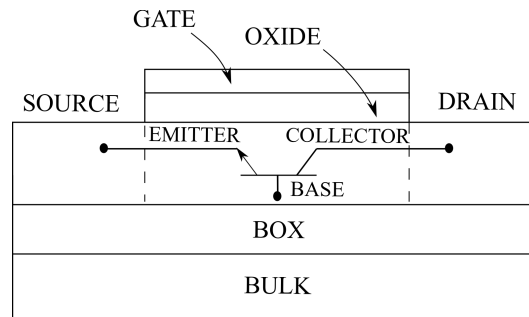


Figure 12. Parasitic bipolar junction transistor (BJT) in single gate junctionless transistor.

3.5. Double Gate

Figure 13 shows the structure of a double gate junctionless transistor. Many models were proposed, and the difference among them depends on the approximations that are involved in the derivation and the considered effects. For instance, many models do not consider short channel and quantum effects [53,55,58,66], while others are only valid for certain doping concentrations and device layer thickness ranges [59,61]. Quantum effects are critically important, because they can affect the threshold voltage [74]. The main issue is modeling the transition between the depletion and the accumulation regions, since the physical behavior is not the same in the two operating regions [56]. A technique involving high doping concentration in the device layer can be considered to reduce the model complexity. This assumption allows for simplifying the depletion width modeling or using the separation of variable in the Poisson equation [62,67].

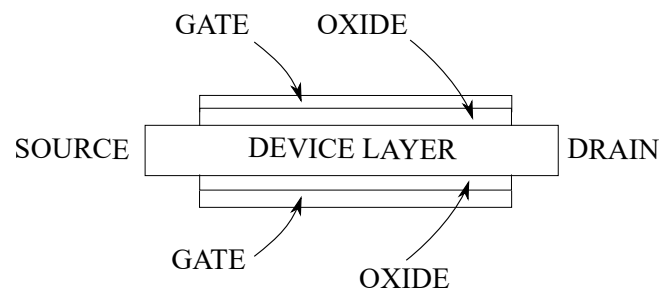


Figure 13. Cross-sectional view of a double gate junctionless transistor.

A model that describes the current in all of the conduction regimes was proposed in [51]. It was validated for symmetrical long channel DG JLTs and describes the device behavior with a continuous current model. Regarding p-type devices, a threshold voltage model was proposed by [52]. They observed that the threshold voltage increases in absolute value as the device layer thickness, the doping concentration and the oxide thickness are increased. Extracting the threshold voltage and the current is therefore important in order to decide the doping concentration, and the gate oxide and device layer thicknesses [54]. Regarding the device performance, it could be negatively affected by the BTBT, which increases the leakage current. A design choice that improves the performance is the implementation of a thicker gate oxide near the gate edges (Figure 14). It was observed that by modifying the gate oxide structure, the energy bands of the carriers under the gate are modified as well, resulting in a reduction of the leakage current [69].

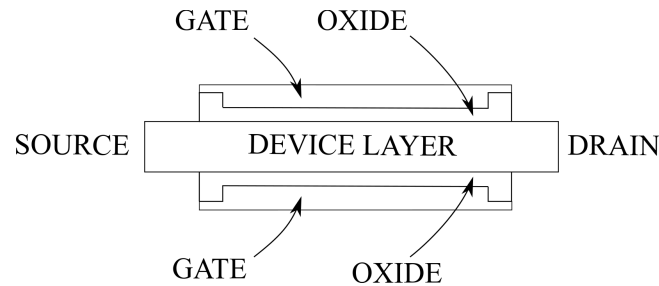


Figure 14. Modified Double Gate junctionless transistor (DG JLT). The gate oxide is thicker near to the gate edges.

The leakage current is lower in double gate junctionless transistors than in SGJLTs [43]. As reported in Table 3, the DGJLT presents better performance both for uniform and non-uniform (Gaussian) doping concentrations.

Table 3. Comparison between SGJLT and Double Gate (DGJLT) in terms of I_{off} for uniform ($1 \times 10^{19} \text{ cm}^{-3}$) and non-uniform (Gaussian) doping concentration [43]. T_{Si} is the device layer thickness.

Structure	L_{ch} (nm)	T_{Si} (nm)	N_D (cm^{-3})	σ (nm)	I_{off} ($\text{A}/\mu\text{m}$)
Single Gate	20	10	uniform	0	2.16×10^{-4}
Double Gate	20	10	uniform	0	1.49×10^{-11}
Single Gate	20	10	non-uniform	6	1.31×10^{-9}
Double Gate	20	10	non-uniform	6	1.48×10^{-15}

Designers could also implement stacked-oxide structures. When compared to the conventional architecture, they present higher I_{on}/I_{off} , lower SS and $DIBL$ [57,65]. By choosing a high dielectric constant material (e.g., HfO_2), a reduction of the leakage current as well as an improvement of the analog parameters could be observed [63,70]. Besides gate oxide engineering, spacer engineering could lead to a performance improvement. Spacers have an influence on the lateral extension of the depletion width and, therefore, on the effective channel length [72,73]. A simpler approach is doping concentration engineering. It was reported that a concentration of $1 \times 10^{18} \text{ cm}^{-3}$ can significantly reduce the threshold voltage sensitivity by 70–90% with respect to the device layer and gate oxide thickness [68]. Graded doping profile can reduce I_{off} by six orders of magnitude [71]. To correctly model JLTs, it is important to also model the carrier mobilities. The main issue is that the bulk mobility is lower than the accumulation one, because of screening effects. The accumulation mobility can be extracted by taking the second derivative of the $1/I_{acc}$ curve. The bulk mobility can be computed by knowing the flat band voltage [64]. The mobility values can be degraded in case high voltages are applied [60]. Moreover, the implementation of complex equations (Schrödinger) is required, as well as the knowledge of parameters, such as impurities and surface roughness scattering mechanisms [75].

3.6. Thin Film

Thin film junctionless transistors are characterized by an ultra-thin channel thickness ($\leq 10 \text{ nm}$) and very high doping concentration ($\geq 1 \times 10^{19} \text{ cm}^{-3}$). The thin film is better for obtaining the full depletion in the *OFF* state, while the high doping concentration ensures high current to flow in the device [77]. An important characteristics of these transistors is their device layer material composition; the majority of reported thin film transistors has polycrystalline silicon as channel material [79,82,84,85]. Therefore, they are identified based on the channel thickness (ultra-thin) and material composition (polysilicon). When considering polysilicon instead of silicon, an important difference arises: the polycrystalline silicon is composed of many crystallites connected by grain boundaries, as shown in

Figure 15a. When electrons get trapped in these boundaries (Figure 15b), a space charge potential Φ_B is formed. The stability of this potential depends on the applied drain voltage. If the latter is too high, trapped electrons could become unstable. The electrons instability influences the grain boundaries potential, which causes oscillation in the drain conductance. This phenomenon is more critical in TFTs with double gates, since the higher mobility allows for the electrons to easily destroy the trapped ones, and increase the oscillation [81]. Designers can limit this phenomenon by increasing the doping concentration [76].

When compared to junction TFTs, the junctionless ones present smaller transconductance g_m and drain conductance g_d . This implies larger Early voltage, improved low frequency noise and higher signal-to-noise ratio (SNR) [78,83]. The performance of thin film junctionless transistors mainly depends on the film thickness and the doping concentration. A high doping concentration ensures high I_{on} , but it also lowers the SS since high carriers concentrations could screen the electric field induced by the gate. The SS also decreases with reduction in device layer thickness [86]. In addition, the temperature can significantly affect the device performance; when the temperature increases, the threshold voltage decreases (in absolute value) and the SS increases. This is attributed to the fact that the energy band gap E_g decreases with temperature, thus increasing the carrier concentration [80]. Table 4 presents the figure of merits of the reported thin film junctionless transistors.

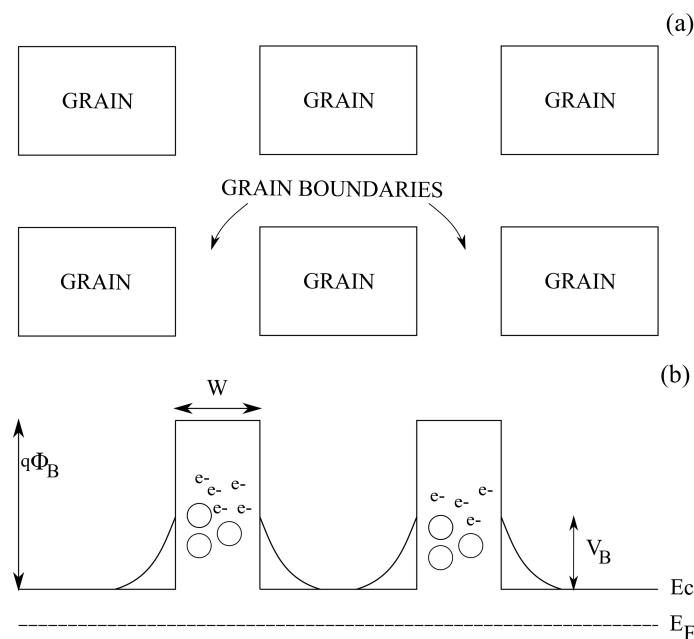


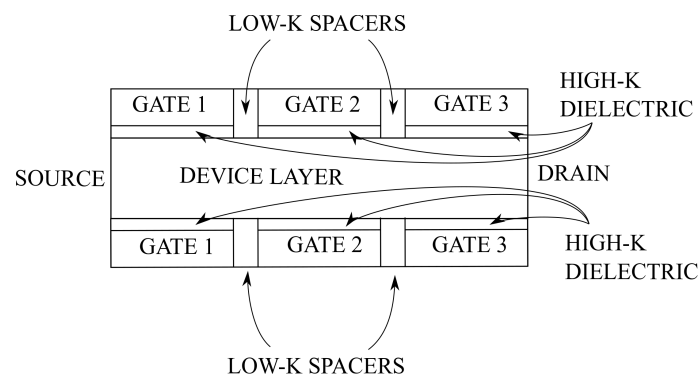
Figure 15. (a) Crystallites organization in polycrystalline films. (b) Energy band diagram showing the trapped electrons in the grain boundaries.

Table 4. Reported figure of merits of junctionless thin film transistors.

Thin Film	L_{ch} (nm)	T_{Si} (nm)	N_D (cm^{-3})	SS (mV/dec)	DIBL (mV/V)	I_{on}/I_{off}	Ref.	Year
Single Gate	400	10	$\geq 1 \times 10^{19}$	240	-	$> 1 \times 10^7$	[76]	2011
NW GAA	1000	12	-	199	-	5.2×10^6	[82]	2011
NW GAA (IM)	1000	12	-	184	-	-	[82]	2011
Single Gate	400	9	-	309	161	8×10^7	[83]	2012
Single Gate (IM)	400	50	-	326	277	3.2×10^4	[83]	2012
NW GAA	60	2	3×10^{19}	61	6	1×10^8	[84]	2013
Single Gate	1000	10	-	329	-	1.4×10^5	[79]	2014
Double Gate	1000	10	-	160	-	1.1×10^7	[79]	2014
NW GAA	200	0.65	$8 \times 10^{18} (N_A)$	43	< 0.4	$> 1 \times 10^8$	[85]	2017

3.7. Tunnel FET

Figure 16 shows the structure of a junctionless tunnel field effect transistor. The device is uniformly and highly doped. The middle gate acts as a control gate, while fixed voltages are applied at the side gates. When considering an n-type device, the tunneling effect can be triggered by correctly fixing the voltages on the side gates, where the source, channel, and drain regions (n-n-n) are converted into a (p-i-n) structure. When a certain control voltage is applied, the barrier between the source and the channel becomes narrower. As a result, current flows because of tunneling. Therefore, the conduction mechanism is different with respect to the other JLTs, since it is not based on depletion. The high-k dielectric below the gate (Si_3N_4 , $k = 7.5$) improves the internal electric field, and, thus, the gate control [94]. The low-k spacers (SiO_2 , $k = 3.9$) are used to isolate the gates; by increasing the dielectric constant of the low-k spacers, it is possible to reduce I_{off} [87]. Increasing the device layer doping concentration leads to an increment of both I_{on} and I_{off} , with the latter being more sensitive to doping variations. Decreasing the doping concentration leads to an improvement of the SS, since its value decreases from 290 mV/dec to 47 mV/dec as the doping concentration decreases from $2 \times 10^{19} cm^{-3}$ to $1 \times 10^{19} cm^{-3}$. Therefore, one of the main advantages of junctionless TFETs is the possibility to achieve sub 60 mV/dec SS. Channel length reductions cause an increment of DIBL, and so of the I_{off} [87].

**Figure 16.** Cross-sectional view of a junctionless tunnel field effect transistor.

Regarding double gate junctionless TFETs (Figure 17), the increment of the dielectric constant k leads to an improvement of I_{on} . Increasing the insulation layer thickness causes an improvement in both I_{on} and SS. However, this design choice leads to an increment of the parasitic capacitances [88,92]. To improve the robustness of junctionless TFETs, it is possible to selectively introduce dielectric

materials in the gate oxide, which can reduce the variations in the coupling capacitance, allowing for higher immunity in terms of sensitivity [93]. The performance can be further increased by implementing dual-material gate (Figure 17a) or heterojunctionless structures (Figure 17b). The energy bandgap of these structures leads to higher I_{on} and I_{on}/I_{off} , and lower SS [89–91]. Besides silicon, other materials were used for the device layer: a junctionless TFET made of indium arsenide was proposed [96]. The figure of merits of the reported junctionless transistors are collected in Table 5.

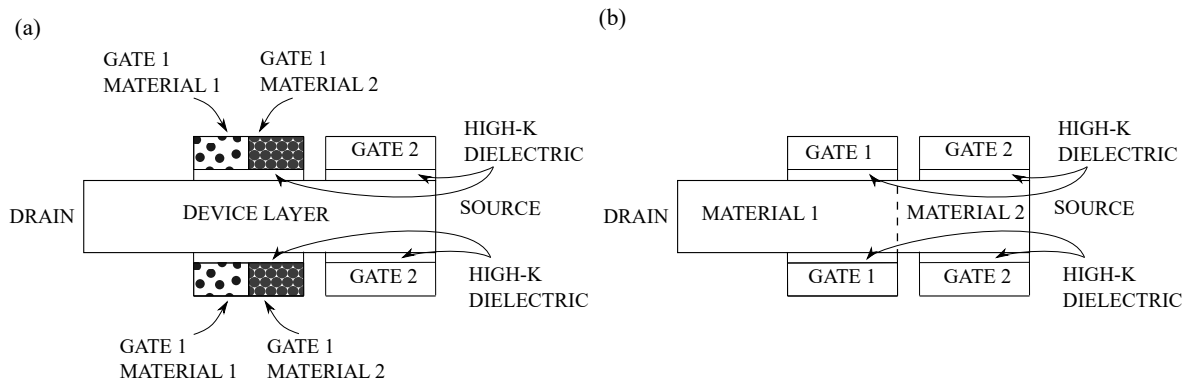


Figure 17. Cross-sectional view of: (a) JLT Tunnel FET (JLT TFET) with dual-material gate. (b) JLT TFET heterojunctionless.

Table 5. Reported figure of merits of junctionless tunnel field effect transistors.

Tunnel FET	L_{ch} (nm)	T_{Si} (nm)	N (cm^{-3})	SS (mV/dec)	$DIBL$ (mV/V)	I_{on}/I_{off}	Ref.	Year
DG	25	5	2×10^{19}	24	38	4.08×10^9	[95]	2013
DG (La_2O_3 , $k = 30$)	20	5	1×10^{19}	~ 87	—	$\sim 3.5 \times 10^8$	[88]	2013
DG (HfO_2 , $k = 25$)	20	5	1×10^{19}	~ 91	—	$\sim 3 \times 10^8$	[88]	2013
DG (TiO_2 , $k = 80$)	20	5	1×10^{19}	~ 70	—	$\sim 6 \times 10^8$	[88]	2013
DG ($AlGaAs : Si$)	20	5	1×10^{19}	~ 41	—	$\sim 1 \times 10^8$	[90]	2014
DG	20	5	1×10^{19}	~ 23	—	$\sim 1 \times 10^{10}$	[92]	2014
DG	20	5	1×10^{19}	84	—	8×10^7	[89]	2014
DG (Ge)	20	5	1×10^{19}	26	—	2×10^{10}	[89]	2014
DG ($GaAs : Si$)	20	5	1×10^{19}	74	—	2×10^8	[89]	2014
DG ($Si : Si_3Ge_7$)	20	5	1×10^{19}	32	—	8×10^6	[89]	2014
DG ($Si : InAs$)	20	5	1×10^{19}	44	—	8×10^5	[89]	2014
DG ($GaAs : Ge$)	20	5	1×10^{19}	16	—	2×10^{12}	[89]	2014
SG ($InAs$)	20	10	1×10^{19}	7	86	$\sim 2 \times 10^{10}$	[96]	2016
DG ($AlGaAs : Si$) (HfO_2)	20	5	1×10^{19}	48.2	—	$\sim 1 \times 10^8$	[94]	2017
DG ($AlGaAs : Si$) (La_2O_3)	20	5	1×10^{19}	47.2	—	$\sim 1 \times 10^8$	[94]	2017
DG ($AlGaAs : Si$) (TiO_2)	20	5	1×10^{19}	43.9	—	$\sim 1 \times 10^8$	[94]	2017
Dual-Material DG	20	5	1×10^{19}	60	—	—	[97]	2019

4. Conclusions

In this work, junctionless transistors that were proposed over the last decade were studied. In particular, the influence of the technological parameters on the main figure of merits (I_{on}/I_{off} , $DIBL$, and SS) were analyzed. Design techniques, such as oxide/doping/spacers engineering, have been

reported. Depending on the design choices, all of the typologies of junctionless transistors can present a high I_{on}/I_{off} ratio, as well as quasi-ideal subthreshold swing and optimal values of $DIBL$. Therefore, it is not possible to determine the best junctionless transistor solely based on the performance parameters. In general, a flexible optimization is associated to the more complex structures. The TFET is difficult to design, since the gate voltages need to be set carefully, and the work function differences must guarantee the tunnel behavior. The DGJLT has a less complex structure compared to TFET, and it presents an additional degree of freedom and enhanced gate control with respect to SGJLT and TFT. The SGJLT has a simple structure, but its performance is not comparable with the other junctionless transistors because of its reduced flexibility in terms of structure engineering. The TFT only presents high performance parameters if the device layer is highly doped and made of very thin polysilicon. FinFETs provide more flexibility in terms of structure engineering as compared to nanowires. The electrostatic control of both nanowires and FinFETs can be increased by surrounding the entire channel with the gate (GAA configuration). Regardless of the structure, junctionless transistors present easier fabrication process and competitive performance when compared to the junction transistors. As junctionless transistors are capable of reaching quasi-ideal subthreshold swing, optimal $DIBL$ values, and high I_{on}/I_{off} ratio, it is expected that they will replace junction-based electronic devices in the following decade. Junctionless transistors are, therefore, the main candidates to become the conventional field effect transistors of the future.

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Abbreviations

The following abbreviations are used in this manuscript:

AM	Accumulation Mode
BJT	Bipolar Junction Transistor
BTBT	Band-To-Band Tunneling
BOX	Buried Oxide
DG	Double Gate
DIBL	Drain-Induced Barrier Lowering
FET	Field Effect Transistor
GAA	Gate-All-Around
IM	Inversion Mode
JLT	Junctionless Transistor
JT	Junction Transistor
LFN	Low Frequency Noise
NW	Nanowire
SELBOX	Selective Buried Oxide
SG	Single Gate
SNR	Signal-To-Noise Ratio
SOI	Silicon-On-Insulator
SON	Silicon-On-Nothing
SS	Subthreshold Swing
TFET	Tunnel Field Effect Transistor
TFT	Thin Film Transistor
TG	Triple Gate

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