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Unlimited Power Division Ratio of Microstrip Balanced-to-Unbalanced Gysel-Type Arbitrary Power Divider

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Abstract: A microstrip balanced-to-unbalanced (BTU) Gysel-type arbitrary power divider without the high-impedance transmission-line (TL) section is proposed to eliminate the power division ratio (PDR) limit of the conventional microstrip BTU power dividers. The proposed circuit includes five moderate-impedance TLs having the same characteristic impedance in addition to a grounded resistor. The arbitrary PDR is easily obtained by varying the electrical length of the TLs without changing the characteristic impedances, especially the large PDR, which is difficult to achieve by means of conventional BTU power dividers. When the PDR is ∞ , the proposed circuit becomes a balun. The closed-form design equations are derived and discussed. To verify the proposed circuit, three prototypes I, II, and III are designed and fabricated for PDRs of 10 dB, 20 dB, and ∞ dB, respectively. The measured PDRs are in good agreement with the simulations. The measured isolation between the output ports is higher than 31 dB for prototypes I and II. The measured insertion loss of the balun prototype is 0.194 dB. Furthermore, the common-mode suppression of greater than 32 dB and the return loss of higher than 22 dB are obtained for various PDRs.

Keywords: balanced to unbalanced; Gysel-type power divider; wide power division ratio range

1. Introduction

Power dividing is widely adopted for various microwave applications such as antenna feeding networks, balanced amplifiers, and mixers [1]. Compared to the Wilkinson power divider, the Gysel-type power divider has the advantage of high power-handling capability because of its grounded resistor to sink the created heat effectively. Besides, the out-of-phase type of power dividers can be used in various circuits such as current bleeding mixers for low noise applications and performance improvement of the balanced circuits [2].

Due to the advantages of good common-mode suppression and high immunity to environmental and device electronic noise, the balanced circuits have been studied, such as balanced filter [3–5], balanced power divider [6–8], and balanced coupler [9–11]. However, for a system with both balanced and unbalanced devices, external baluns are required for the connection between the conventional power divider and balanced circuits, which increase the circuit size. In order to solve this problem, the balanced-to-unbalanced (BTU) power divider is proposed to connect both balanced and unbalanced components. Moreover, the BTU power divider can divide one pair of differential-mode signals into the isolated single-ended ports, and common-mode rejection can also be realized [12–17]. The BTU power



divider with an arbitrary power division ratio (PDR) is more useful and has the flexibility to divide the power arbitrarily. Thus far, the PDR of the existing microstrip BTU power divider is only controlled by means of the characteristic impedances of the different transmission-line (TL) sections [18–22]. For a large PDR, a high-impedance TL is required. Due to the realizable impedance range of 20–120 Ω for microstrip lines, the maximum PDR of the existing microstrip BTU power divider is 6.8 dB [18].

In this paper, a BTU Gysel-type arbitrary power divider without the high-impedance TL is proposed to eliminate the PDR limit of the conventional microstrip BTU power dividers, along with out-of-phase characteristics at two unbalanced output ports and high power-handling capacity. The proposed circuit includes five moderate-impedance TLs having the same characteristic impedance in addition to a grounded resistor. The arbitrary PDR can be easily obtained by varying the electrical length of the TLs without changing the characteristic impedances. Design formulas are derived, and both the theoretical and experimental results are given and discussed.

2. Circuit Structure and Design Theory

The schematic of the proposed BTU arbitrary power divider is depicted in Figure 1. It is composed of one half-wavelength transmission line (i.e., electrical length of $\theta_1 = 180^\circ$), two-section transmission lines with the electrical length θ_2 , two-section transmission lines with the electrical length θ_3 , and an isolation resistor *R*. The isolation resistor is grounded, which makes the created heat sinking of the resistors possible. Besides, all the transmission lines have the same characteristic impedance Z_1 . The PDR is controlled by means of the electrical lengths of θ_2 and θ_3 . The balanced input port *A* comprises ports 1 and 4 terminated with Z_{01} , and the output ports 2 and 3 are two unbalanced ports terminated with Z_{02} .



Figure 1. The proposed balanced-to-unbalanced (BTU) arbitrary power divider.

2.1. Analysis of Impedance Matching and Isolation Conditions

To obtain the perfect impedance matching and isolation conditions, the proposed power divider between ports 2 and 3 can be separated into two paths, as shown in Figure 1, and the *ABCD* matrix of two paths can be obtained as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{23_Path1} = \begin{bmatrix} \cos\theta_3 & jZ_1\sin\theta_3 \\ j\sin\theta_3/Z_1 & \cos\theta_3 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 1/R & 1 \end{bmatrix} \begin{bmatrix} \cos\theta_2 & jZ_1\sin\theta_2 \\ j\sin\theta_2/Z_1 & \cos\theta_2 \end{bmatrix},$$
(1)

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{23_Path2} = \begin{bmatrix} \cos\theta_2 & jZ_1\sin\theta_2 \\ \frac{j\sin\theta_2}{Z_1} & \cos\theta_2 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_{01}} & 1 \end{bmatrix} \begin{bmatrix} \cos\theta_1 & jZ_1\sin\theta_1 \\ \frac{j\sin\theta_1}{Z_1} & \cos\theta_1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_{01}} & 1 \end{bmatrix} \begin{bmatrix} \cos\theta_3 & jZ_1\sin\theta_3 \\ \frac{j\sin\theta_3}{Z_1} & \cos\theta_3 \end{bmatrix}.$$
(2)

The ABCD parameters of two paths are derived as

$$A_{23 \text{ Path1}} = \cos \theta_2 \cos \theta_3 - \sin \theta_2 \sin \theta_3 + jZ_1 \cos \theta_2 \sin \theta_3 / R, \tag{3a}$$

$$B_{23 \text{ Path1}} = -Z_1^2 \sin \theta_2 \sin \theta_3 / R + jZ_1 \cos \theta_2 \sin \theta_3 + jZ_1 \cos \theta_3 \sin \theta_2, \qquad (3b)$$

$$C_{23_Path1} = \cos\theta_2 \cos\theta_3 / R + j\cos\theta_3 \sin\theta_2 / Z_1 + j\cos\theta_2 \sin\theta_3 / Z_1,$$
(3c)

$$D_{23_Path1} = \cos\theta_2 \cos\theta_3 - \sin\theta_2 \sin\theta_3 + jZ_1 \cos\theta_3 \sin\theta_2 / R,$$
(3d)

$$A_{23}_{\text{Path}2} = \sin\theta_2 \sin\theta_3 - \cos\theta_2 \cos\theta_3 - j2Z_1 \cos\theta_3 \sin\theta_2 / Z_{01}, \tag{4a}$$

$$B_{23}Path2} = 2Z_1^2 \sin \theta_2 \sin \theta_3 / Z_{01} - jZ_1 \cos \theta_2 \sin \theta_3 - jZ_1 \cos \theta_3 \sin \theta_2,$$
(4b)

$$C_{23_Path2} = -2\cos\theta_2\cos\theta_3/Z_{01} - j\cos\theta_2\sin\theta_3/Z_1 - j\cos\theta_3\sin\theta_2/Z_1,$$
(4c)

$$D_{23_Path2} = \sin \theta_2 \sin \theta_3 - \cos \theta_2 \cos \theta_3 - j2Z_1 \cos \theta_2 \sin \theta_3 / Z_{01}.$$
 (4d)

To meet the requirement of perfect isolation ($S_{23} = 0$) and perfect matching at output ports ($S_{22} = 0$ and $S_{33} = 0$), the following relations need to satisfy [22]

$$B_{23}Path1 + B_{23}Path2 = 0, (5)$$

$$Z_{02} = \frac{B_{23}\text{Path1}}{D_{23}\text{Path1} - D_{23}\text{Path2}} = \frac{B_{23}\text{Path2}}{D_{23}\text{Path2} - D_{23}\text{Path1}}.$$
(6)

By substituting (3b) and (4b) into (5), the following equation is obtained.

$$2Z_1^2 \sin \theta_2 \sin \theta_3 / Z_{01} - Z_1^2 \sin \theta_2 \sin \theta_3 / R = 0.$$
(7)

Equation (7) can be simplified as

$$R = Z_{01}/2.$$
 (8)

By substituting (3b), (3d), (4d) and (8) into (6), the following equation is obtained:

$$-Z_1^2 \sin \theta_2 \sin \theta_3 / R + jZ_1 \cos \theta_2 \sin \theta_3 + jZ_1 \cos \theta_3 \sin \theta_2$$

= $Z_{02}(2\cos \theta_2 \cos \theta_3 - 2\sin \theta_2 \sin \theta_3 + jZ_1 \cos \theta_3 \sin \theta_2 / R + jZ_1 \cos \theta_2 \sin \theta_3 / R)$ (9)

For simplicity, Z_1 and Z_{02} are set to be equal to R.

$$Z_1 = Z_{02} = R. (10)$$

Then, the relation between θ_2 and θ_3 is derived with Equation (9) as

$$2\cos\theta_2\cos\theta_3 = \sin\theta_2\sin\theta_3. \tag{11}$$

It is obtained from Equation (11) that

$$\tan \theta_2 \tan \theta_3 = 2. \tag{12}$$

Thus, the perfect impedance matching and isolation conditions for the proposed power divider are obtained as (8), (10), and (12).

2.2. Analysis of Power Transmission from Input Port to Output Ports

Due to the fact that when the differential port *A* (combined by ports 1 and 4) is excited, all the input power is transmitted solely to the terminations at ports 2 and 3 [23]. There is no power dissipation in the isolation resistor at the center frequency. The voltage V_R (as shown in Figure 1) for the resistor *R* is zero at the center frequency; therefore, the schematic in Figure 1 is simplified as shown in Figure 2 for the analysis of the power transmission characteristics of the proposed power divider at the center frequency. If the PDR between ports 2 and 3 is k^2 :1, $V_2 = -kV_3$. The voltage relations of the two output

branch lines for the differential excitation case (i.e., $V_4 = -V_1$) can be obtained by using the *ABCD* transmission matrix concept as (13).

$$V_1 = V_2 \cos \theta_2 + V_2 \sin \theta_2 \cot \theta_3 + j V_2 Z_1 \sin \theta_2 / Z_{02},$$
(13a)

$$V_4 = -V_1 = V_3 \cos \theta_3 + V_3 \sin \theta_3 \cot \theta_2 + j V_3 Z_1 \sin \theta_3 / Z_{02}.$$
 (13b)



Figure 2. Transmission part of the proposed BTU arbitrary power divider.

By using the relations of $V_4 = -V_1$ and $Z_1 = Z_{02}$, it is obtained as

$$V_2\cos\theta_2 + V_2\sin\theta_2\cot\theta_3 + jV_2\sin\theta_2 = -(V_3\cos\theta_3 + V_3\sin\theta_3\cot\theta_2 + jV_3\sin\theta_3).$$
(14)

By equating the real part and imaginary part of (14), the PDR can be derived as

$$k = -\frac{V_2}{V_3} = \frac{\sin\theta_3}{\sin\theta_2}.$$
(15)

It can be seen from Equation (15) that the PDR of the proposed BTU power divider is only determined by the electrical lengths of the TLs (i.e., θ_2 and θ_3) when $Z_1 = Z_{02} = R = Z_{01}/2$.

By substituting (15) into (11), the following equation is obtained:

$$2\sqrt{1-\sin^2\theta_2}\sqrt{1-k^2\sin^2\theta_2} = k\sin^2\theta_2.$$
 (16)

Equation (16) is solved as

$$\sin \theta_2 = \sqrt{\frac{4k^2 + 4 - \sqrt{(4k^2 + 4)^2 - 48k^2}}{6k^2}}.$$
(17)

Thus, the design equations of the proposed power divider are obtained as (8), (10), (12), and (17).

2.3. S-Parameter Analysis

To derive the standard *S*-parameter of the proposed circuit, by using the topology shown in Figure 2, the *ABCD* matrix between ports 1 and 4 can be obtained as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{14} = \begin{bmatrix} 1 & 0 \\ Y_{L1} & 1 \end{bmatrix} \begin{bmatrix} \cos \theta_1 & jZ_1 \sin \theta_1 \\ jY_1 \sin \theta_1 & \cos \theta_1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_{L2} & 1 \end{bmatrix},$$
(18)

where

$$Y_{L1} = \frac{Y_1(Y_{02} - jY_1 \cot \theta_3 + jY_1 \tan \theta_2)}{Y_1 + Y_1 \tan \theta_2 \cot \theta_3 + jY_{02} \tan \theta_2},$$
(19a)

$$Y_{L2} = \frac{Y_1(Y_{02} - jY_1 \cot \theta_2 + jY_1 \tan \theta_3)}{Y_1 + Y_1 \tan \theta_3 \cot \theta_2 + jY_{02} \tan \theta_3},$$
(19b)

with $Y_1 = 1/Z_1$ and $Y_{02} = 1/Z_{02}$.

Substituting (10) into (18) and using (12), the ABCD matrix between ports 1 and 4 is derived as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{14} = \begin{bmatrix} -1 & 0 \\ -\frac{Y_1(Y_{02}-jY_1\cot\theta_3+jY_1\tan\theta_2)}{Y_1+Y_1\tan\theta_2\cot\theta_3+jY_{02}\tan\theta_2} - \frac{Y_1(Y_{02}-jY_1\cot\theta_2+jY_1\tan\theta_3)}{Y_1+Y_1\tan\theta_3\cot\theta_2+jY_{02}\tan\theta_3} & -1 \end{bmatrix} = \begin{bmatrix} -1 & 0 \\ -Y_{02}(\tan\theta_3-j+j2)-Y_{02}(\tan\theta_2-j+j2) \\ -Y_{02}(\tan\theta_3+j2) & -1 \end{bmatrix} = \begin{bmatrix} -1 & 0 \\ -Y_{02} & -1 \end{bmatrix}$$
(20)

Using the conversion from *ABCD* matrix to *S*-parameters, the *S*-parameters in terms of ports 1 and 4 are obtained with (20) as

$$\begin{bmatrix} S_{11} & S_{14} \\ S_{41} & S_{44} \end{bmatrix} = \begin{bmatrix} -1/2 & -1/2 \\ -1/2 & -1/2 \end{bmatrix}.$$
 (21)

Moreover, when either port 1 or 4 is excited, the two divided waves at ports 2 and 3 are 180° out of phase. To realize the PDR of k^2 :1 between the output ports, S_{21} and S_{31} can be obtained using (13). According to the definition of *S*-parameters and the use of (15), S_{21} and S_{31} are finally simplified as follows,

$$S_{21} = \frac{V_2}{\sqrt{2}V_1} = \frac{k}{\sqrt{2}(\sqrt{1 - k^2 \sin^2 \theta_2} + ke^{j\theta_2})},$$
(22)

$$S_{31} = \frac{-V_3}{\sqrt{2}V_1} = \frac{-1}{\sqrt{2}(\sqrt{1 - k^2 \sin^2 \theta_2} + ke^{j\theta_2})}.$$
(23)

Considering the perfect isolation between ports 2 and 3 ($S_{ss23} = 0$) and the perfect matching at output ports ($S_{ss22} = 0$, $S_{ss33} = 0$), as mentioned in Section 2.1, the standard scattering matrix S_{std} is derived as

$$[S_{\text{std}}] = \begin{bmatrix} -1/2 & S_{21} & S_{31} & -1/2 \\ S_{21} & 0 & 0 & -S_{21} \\ S_{31} & 0 & 0 & -S_{31} \\ -1/2 & -S_{21} & -S_{31} & -1/2 \end{bmatrix}.$$
 (24)

Based on the standard S-parameters (24), the mixed-mode scattering matrix can be obtained as [19]

$$[S_{\rm mm}] = \begin{bmatrix} S_{\rm ddAA} & S_{\rm dsA2} & S_{\rm dsA3} & S_{\rm dcAA} \\ S_{\rm sd2A} & S_{\rm ss22} & S_{\rm ss23} & S_{\rm sc2A} \\ S_{\rm sd3A} & S_{\rm ss32} & S_{\rm ss33} & S_{\rm sc3A} \\ S_{\rm cdAA} & S_{\rm csA2} & S_{\rm csA3} & S_{\rm ccAA} \end{bmatrix} = \begin{bmatrix} 0 & \sqrt{2}S_{21} & \sqrt{2}S_{31} & 0 \\ \sqrt{2}S_{21} & 0 & 0 & 0 \\ \sqrt{2}S_{31} & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 \end{bmatrix},$$
(25)

where S_{sd} denotes differential-mode to single-ended transmission coefficients; S_{sc} denotes common-mode to single-ended suppression coefficients; S_{dd} , S_{cc} , and S_{cd} denote differential return loss, common-mode reflection, and differential-mode to common-mode conversion coefficient, respectively; and S_{ss} indicates a single-ended *S*-parameter.

3. Parameter Analysis

Based on the previous theory analysis, the design parameters of the proposed power divider can be easily calculated. For a given PDR, θ_2 and θ_3 can be calculated by using (17) and (12), respectively.

Figure 3 gives the calculated values of θ_2 and θ_3 for the different PDRs from 0 to 30 dB when $Z_1 = Z_{02} = R = Z_{01}/2$. It shows that the PDRs are controlled by means of the electrical lengths of θ_2 and θ_3 . For various PDRs from 0 to 30 dB, θ_2 and θ_3 are always less than 90°, which implies that the size of the proposed BTU power divider will be less than that of the existing BTU power divider [18,19].



Figure 3. Electrical length versus power division ratio (PDR).

To verify the design Equation (8), (10), (12), and (17), three sets of design parameters are calculated according to the PDRs of 0 dB, 10 dB, and 20 dB. In these three cases, all the electrical parameters of the TLs are the same, except for the values of θ_2 and θ_3 with $Z_{02} = Z_1 = R = 50 \Omega$, $Z_{01} = 2Z_{02} = 100 \Omega$. Two quarter-wavelength impedance transformers are applied for matching Z_{01} to the standard 50- Ω port, which has the characteristic impedance of $\sqrt{2}Z_{02}$. The calculated values of θ_2 for the PDRs of 0 dB, 10 dB, and 20 dB are 54.74°, 18.18°, and 5.73°, respectively. For the three cases, the values of θ_3 are 54.74°, 80.67°, and 87.13°, respectively. The mixed scattering parameters are given in Figure 4. When port *A* is excited in differential mode, the $|S_{sd2A}|$ values at f_0 in Figure 4a for the three cases are -3.010, -0.414, and -0.043 dB, respectively, and the $|S_{sd3A}|$ values are -3.010 dB, -10.415 dB, and -20.046 dB, leading to the desired PDRs of 0 dB, 10 dB, and 20 dB. Perfect isolation between ports 2 and 3 and perfect impedance matching at ports 2 and 3 are achieved at f_0 for various PDRs, as shown in Figure 4b.



Figure 4. Mixed scattering parameters for three cases of PDR. (**a**) S_{sd} and S_{dd} . (**b**) Output ports isolation and return loss. (**c**) S_{sc} , S_{cc} , and S_{dc} . (**d**) Phase difference between output ports.

When port *A* is excited in the common mode, $|S_{ccAA}|$ at f_0 is always 0 dB, and the transmission parameters of $|S_{cc2A}|$ and $|S_{cc3A}|$ at f_0 are all less than -65 dB, implying that no power transfers from the common-mode port *A* to ports 2 and 3, as shown in Figure 4c. Figure 4d shows that the phase difference between S_{sd3A} and S_{sd2A} is constant at 180° for a PDR of 0 dB. As the PDR increases, the out-of-phase bandwidth will decrease.

4. Implementation and Performance

For the verification of the proposed theory, three prototypes I, II, and III are designed with a center frequency of $f_0 = 1.0$ GHz for PDRs of 10 dB, 20 dB, and ∞ dB, respectively. The circuit is implemented on the PTFE/woven-glass substrate with a relative permittivity of 2.65 and a thickness of 1.5 mm.

4.1. Prototype I for a PDR of 10 dB

In this case, the output-port termination impedance Z_{02} is selected as 50 Ω . According to Section 2, it is determined that $Z_1 = R = Z_{02} = 50 \Omega$, $Z_{01} = 100 \Omega$, and $\theta_1 = 180^\circ$. The values of θ_2 and θ_3 are calculated by using Equations (12) and (17) as 18.18° and 80.67°, respectively. Using the TL synthesis tool ADS Linecalc, the physical dimensions of TLs are calculated. In order to take account of the distributed inductance effect of via holes for optimal physical dimensions of TLs, final dimensions are obtained by using the HFSS EM simulation. The final dimensions of the prototype I are given in Table 1. As shown in Figure 5, two $\lambda/4$ impedance transformers with the width of W_1 are used for matching the impedance Z_{01} of 100- Ω to 50- Ω input-port impedance. The lengths of two $\lambda/4$ impedance transformers are L_1 and L_7 , respectively. The width of the branch lines is W_2 for the characteristic impedance of $Z_1 = 50 \Omega$. Besides, based on the available chip resistors, the grounded resistance *R* is selected as 51 Ω .

Table 1. Dimensions of the prototype I (unit: mm; referring to Figure 5).

L_1	L_2	L_3	L_4	L_5	L_6	L_7	W_1	W_2
48.7	9.05	50.0	11.3	37.65	93.1	48.7	2.3	4.1



Figure 5. Photograph of the fabricated 10-dB BTU power divider.

The simulated and measured mixed *S*-parameters of the proposed 10-dB BTU power divider are shown in Figure 6. At the center frequency of $f_0 = 1.0$ GHz, the measured $|S_{sd2A}|$, as shown in Figure 6a, is -0.472 dB and $|S_{sd3A}|$ is -10.478 dB, meeting the requirement for a PDR of 10 dB. At f_0 , the measured differential return loss is 24.2 dB, and the fractional bandwidth (FBW) of the return loss better than 10 dB is about 23.4% (from 0.896 GHz to 1.133 GHz). Figure 6b shows that the measured isolation between output ports 2 and 3 at f_0 is 38.2 dB, and it is better than 15 dB over 0.842 GHz to 1.203 GHz (35.3%). In Figure 6c, the common-mode reflection $|S_{ccAA}|$ is greater than -1 dB from 0.766 GHz to 1.237 GHz (47.0%). The mode conversion coefficient at the balanced port $|S_{dcAA}|$ is less than -15 dB over the entire frequency range of interest. The common-mode suppression is better than 15 dB from 0.869 GHz to 1.092 GHz (22.7%) with a maximum common-mode suppression of 36.5 dB at 0.979 GHz. In Figure 6d, the measured phase difference between output ports 2 and 3 is $180^{\circ} \pm 5^{\circ}$ in the frequency range from 0.944 GHz to 1.100 GHz. An excellent out-of-phase characteristic around the center frequency is obtained.



Figure 6. Performances of the proposed 10-dB BTU power divider. (**a**) $|S_{sd2A}|$, $|S_{sd3A}|$, and $|S_{ddAA}|$. (**b**) Output ports isolation and return loss. (**c**) $|S_{ccAA}|$, $|S_{sc2A}|$, $|S_{sc3A}|$, and $|S_{dcAA}|$. (**d**) Phase difference between the output ports.

4.2. Prototype II for a PDR of 20 dB

Compared to prototype I, only θ_2 and θ_3 need to change for a PDR of 20 dB. Using Equations (12) and (17), θ_2 and θ_3 are calculated and obtained as 5.73° and 87.13°, respectively. The photograph of the fabricated prototype II is shown in Figure 7. The dimensions of the prototype II are given in Table 2.



Figure 7. Photograph of the fabricated 20-dB BTU power divider.

L_1	L_2	L_3	L_4	L_5	L_6	L_7	W_1	W_2
48.7	2.55	51.0	9.3	36.9	85.8	48.7	2.3	4.1

Table 2. Dimensions of the prototype II (unit: mm; referring to Figure 7).

The simulated and measured mixed *S*-parameters of the proposed 20-dB BTU power divider are shown in Figure 8. At the center frequency of $f_0 = 1.0$ GHz, the measured $|S_{sd2A}|$, as shown in Figure 8a, is -0.233 dB and $|S_{sd3A}|$ is -20.121 dB; therefore, the measured PDR is 19.89 dB. At f_0 , the measured differential return loss is 25.1 dB. The return loss is better than 10 dB from 0.891 GHz to 1.090 GHz (a FBW of about 20.0%). Figure 8b shows that the measured isolation between output ports 2 dB and 3 dB at f_0 is 31.4 dB, and it is better than 15 dB from 0.817 GHz to 1.157 GHz (34.4%). In Figure 8c, the common-mode suppression is better than 15 dB from 0.894 GHz to 1.109 GHz (21.5%) with a maximum common-mode suppression of 32.5 dB. The mode conversion coefficient at the balanced port is better than 16.5 dB over the entire frequency range from 0.7 GHz to 1.3 GHz. The common-mode reflection $|S_{ccAA}|$ is greater than -1 dB from 0.766 GHz to 1.237 GHz (47.0%). In Figure 8d, the measured phase difference between output ports 2 and 3 is $180^\circ \pm 5^\circ$ from 0.98 GHz to 1.10 GHz. The out-of-phase characteristic around f_0 is also obtained.



Figure 8. Performances of the proposed 20-dB BTU power divider. (a) $|S_{sd2A}|$, $|S_{sd3A}|$, and $|S_{ddAA}|$. (b) Output ports isolation and return loss. (c) $|S_{ccAA}|$, $|S_{sc2A}|$, $|S_{sc3A}|$, and $|S_{dcAA}|$. (d) Phase difference between the output ports.

4.3. Prototype III for a PDR of ∞ dB

For a PDR of ∞ dB, the electrical lengths of θ_2 and θ_3 are 0° and 90°, respectively. Meanwhile, the termination at port 3 and the isolation resistor are in parallel, which could be merged in a single resistor (i.e., $R = 50 \Omega / 50 \Omega$). However, the 25- Ω resistors do not exist as discrete components.

So, the available chip resistor $R = 24 \Omega$ is chosen for use. Then, the proposed BTU power divider becomes a balun, as shown in Figure 9. The dimensions of the fabricated balun are given in Table 3. The simulated and measured mixed *S*-parameters of the proposed balun (i.e., the prototype III) are shown in Figure 10.



Figure 9. Photograph of the fabricated balun.

Table 3. Dimensions of the prototype III (unit: mm; referring to Figure 9).



Figure 10. Performances of the proposed balun. (a) $|S_{sd2A}|$, $|S_{ss22}|$ and $|S_{ddAA}|$. (b) $|S_{ccAA}|$, $|S_{sc2A}|$, and $|S_{dcAA}|$.

In Figure 10a, the measured $|S_{sd2A}|$, $|S_{ddAA}|$, and $|S_{ss22}|$ at f_0 are -0.194 dB, -22.1 dB, and -44.7 dB, respectively. The FBW for the measured return loss better than 10 dB is about 24.7% from 0.886 GHz to 1.136 GHz. In Figure 10b, the common-mode suppression is better than 15 dB from 0.840 GHz to 1.156 GHz (31.7%) with a maximum common-mode suppression of 33.6 dB. The measured $|S_{dcAA}|$ is less than -13 dB from 0.7 GHz to 1.3 GHz with a minimum common-mode to differential-mode conversion coefficient of -36.6 dB.

4.4. Performance Comparison

The comparison of the proposed BTU arbitrary power divider with previous works is summarized in Table 4. The PDR of the proposed BTU power divider is considerably larger than that of [18–21], which is attributed to the proposed configuration without a need for the high-impedance transmission lines (HITL). The cost of the large PDR is the FBW of the proposed BTU power divider less than that of [18,19,21], which is reasonable and acceptable. The size of the proposed BTU power divider is less

than that of [18–21], which is mainly because θ_2 and θ_3 values are always less than 90° for various PDRs. Furthermore, good common-mode suppression (CMS), high isolation, and large return loss are also obtained for arbitrary PDRs.

Ref.	Туре	Phase	HITL	f ₀ (GHz)	PDR (dB)	CMS (dB)	Isolation (dB)	RL (dB)	FBW (%)	Size $(\lambda_{g} \times \lambda_{g})$
[18]	BTU	OOP	Needed	2	3	>20	~18	~25	~43	0.73×0.45
[19]	BTU	OOP	Needed	2	5	34.9	27.7	27.7	~44	0.48×0.48
[20]	UTB	IP	Needed	2	3	>20	>20	~22	~21	0.72×0.51
[21]	UTB	IP	Needed	2	3	35.4	41.2	37.8	~37	0.75×0.51
Prototype I	BTU	OOP	None	1	10	36.5	38.2	24.2	23.4	0.45×0.29
Prototype II	BTU	OOP	None	1	20	32.5	31.4	25.1	20.0	0.44×0.28
Prototype III	BTU	OOP	None	1	∞	33.6	-	22.1	24.7	0.42×0.30

 Table 4. Performance comparison.

UTB: Unbalanced-to-balanced. UTU: Unbalanced-to-unbalanced. OOP: Out-of-phase. IP: In-phase. HITL: High impedance transmission lines. PDR: Power division ratio. CMS: Common mode suppression. RL: Return loss. FBW: Fractional bandwidth.

5. Conclusions

In this paper, a BTU Gysel-type power divider with arbitrary PDR and out-of-phase characteristics has been presented. It can be easily synthesized with the prescribed PDR. The proposed configuration includes five-section of moderate-impedance TLs, which have the same characteristic impedances but different electrical lengths. The PDR is controlled by the electrical lengths of the TLs, which can avoid the limitation of the high impedance TLs on the PDR. The FBW is 20.0–24.7% for various PDRs. Furthermore, the proposed BTU Gysel-type power divider is also useful for high-power applications.

Further work is required to broaden the bandwidth. Based on the proposed configuration, the research on dual-band BTU arbitrary power divider could be carried out.

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