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LC Impedance Source Bi-Directional Converter with Reduced Capacitor Voltages

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Abstract: This paper proposes an LC (Inductor and Capacitor) impedance source bi-directional DC–DC converter by redesigning after rearranging the reduced number of components of a switched boost bi-directional DC–DC converter. This new converter with a conventional modulation scheme offers several unique features, such as a) a lower number of components and b) reduced voltage stress on the capacitor compared to existing topologies. The reduction of capacitor voltage stress has the potential of improving the reliability and enhancing converter lifespan. An analysis of the proposed converter was completed with the help of a mathematical model and state-space averaging models. The converter performance under different test conditions is compared with the conventional bi-directional DC–DC converter, Z-source converter, discontinuous current quasi Z-source converter, continuous current quasi Z-source converter, improved Z-source converter, switched boost converter, current-fed switched boost converter, and quasi switched boost converter in the Matlab Simulink environment. MATLAB/Simulink results demonstrate that the proposed converter has lesser components count and reduced capacitors' voltage stresses when compared to the topologies mentioned above. A 24 V to 18 V LC-impedance source bi-directional converter and a conventional bidirectional converter are built to investigate the feasibility and benefits of the proposed topology. Experimental results reveal that capacitor voltage stresses, in the case of proposed topology are reduced by 75.00% and 35.80% in both boost and buck modes, respectively, compared to the conventional converter circuit.

Keywords: bi-directional converter; LC impedance source converter; DC–DC power converter; bi-directional power flow

1. Introduction

The study, development, and applications of bidirectional power converters are gaining a lot of attention due to their vital role in areas like renewable energy systems, DC microgrids, hybrid energy storage systems, smart mobility, etc. A bidirectional DC-DC converter (BDC) allows power flow in both directions. This functionality is not available in a traditional unidirectional DC-DC converter. Because of this flexibility, BDCs are widely used in several applications, such as battery-powered electric vehicles (BEVs) or hybrid electric vehicles (HEVs), power trains, uninterruptable power supplies (UPS), smart grids, charging stations for BEVs and plug-in hybrid electric vehicles (PHEV), aerospace, defense, aerospace, and non-conventional energy sources such as photovoltaic (PV) arrays, fuel cells (FCs), and wind turbines. Specifically, BDCs are widely adopted by the electric vehicle industry to achieve objectives, such as battery charging/discharging and energy recovery during regeneration modes of operation in electric vehicles. In case of the BEVs, electric energy needs to flow in both directions, i.e., from the motor to the battery and vice versa in regenerative mode. To avoid pollutant emissions, the electric vehicle must be powered only by batteries or other electrical sources (fuel

cells, solar panels, etc.) [1–4]. In all the above-mentioned applications, a BDC is preferred for saving space by eliminating a separate boost and buck converter. A BDC can offer some benefits, like cost reduction, improved power density, and effective utilization of the converter [4]. Figure 1 shows the typical structure of the bidirectional DC–DC converters. The BDC, shown in Figure 2, helps to enhance the system efficiency and performance by interfacing with power and energy storage devices [5]. It also avoids a couple of individual unidirectional converters for achieving bidirectional power flow. The BDC's mode of operation (buck or boost) is mainly decided by power flow direction and voltage levels of sources/energy storage elements. Accordingly, the controller must be designed to regulate the voltage/current of the system. While designing DC–DC converters, the main functional objectives are high power density and high efficiency. The high density can be achieved by increasing the switching frequency [6] due to the reduction in reactive components size. However, the problem is that increasing the switching frequency increases the switching losses, which leads to efficiency reduction. This problem can be addressed by adopting wide-bandgap power devices along with suitable gate drivers instead of conventional Si devices.

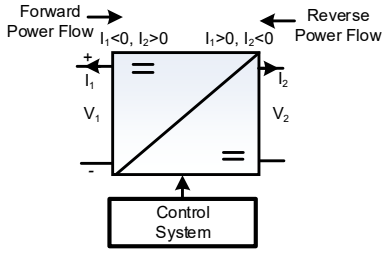


Figure 1. Structure of bi-directional DC–DC converters.

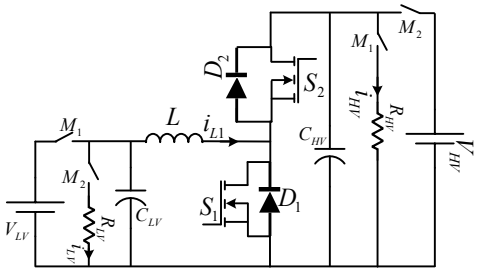


Figure 2. Conventional bidirectional converter (BDC).

In general, conventional step-up DC–DC converters are classified into isolated and non-isolated converters. Isolated converters like fly-back, push–pull, forward, half-bridge, and full-bridge converters have a high voltage gain by keeping a high enough transformer turns ratio. However, there is a problem with voltage spikes due to transformer leakage inductance, which leads to high power losses across the switch. On the other hand, in non-isolated converters, a high duty cycle is required to get a high voltage gain, which leads to decreasing efficiency due to reverse recovery problems [7]. In addition, non-isolated converters also have the problem of voltage stress nearly equal to the output voltage, causing a reduction of the device's reliability. Many DC–DC converter topologies are introduced to mitigate the problems mentioned above, such as interleaving topologies for the reduction of current ripple [8,9], soft-switching techniques to mitigate voltage spikes and efficiency improvement [10], and cascading boost converters [11] and incorporating a coupled inductor [12] in the conventional boost topology to get a high conversion gain. Input current ripples are reduced with the help of an interleaving concept, which leads to improving the source life. Additionally, it offers the flexibility of current sharing to enhance the power handling capacity [8,9].

On the other hand, several other converter topologies are suggested in the literature; most of these are designed to meet the various objectives, such as reliability, capacitor voltage reduction, and input current ripple reductions, by placing an impedance network between input DC source and

switching network in various fashions. An X-shaped LC impedance network, as shown in Figure 3a, is placed to get the voltage boosting capability by operating a switching network in the shoot-through mode [13]. As an alternative to the Z-source converter, the same authors proposed a quasi Z-source (qZS) converter in two variants based on input current, namely continuous input current q-ZS (qZS-CC) and discontinuous input current q-ZS (qZS-DC) [14,15] with a reduced current and capacitor voltage stresses, respectively. The main variation between these two topologies is the input side inductor connection with the supply. In case of qZS-CC, the inductor is placed directly in series with the source, and it tries to always maintain constant input current, whereas the source current is of discontinuous nature in the case of qZS-DC, which increases the stress on the source [15]. Later, Yu Tang et al. proposed an improved Z-source (IZS) converter [16] with reduced capacitor stresses. In this paper, the authors claim that the utilization of a low voltage capacitor reduces the inrush current, the resonance between the Z-source inductor and capacitors, and the cost and volume of the system compared to a conventional Z-source converter [17]. The switched boost converter is proposed with a reduced passive components count, achieved by replacing one pair of LCs with power semi-conductor devices to have the same kind of buck-boost conversion, as shown in Figure 3b [18]. However, this topology uses more power semiconductor devices compared to the topologies mentioned above.

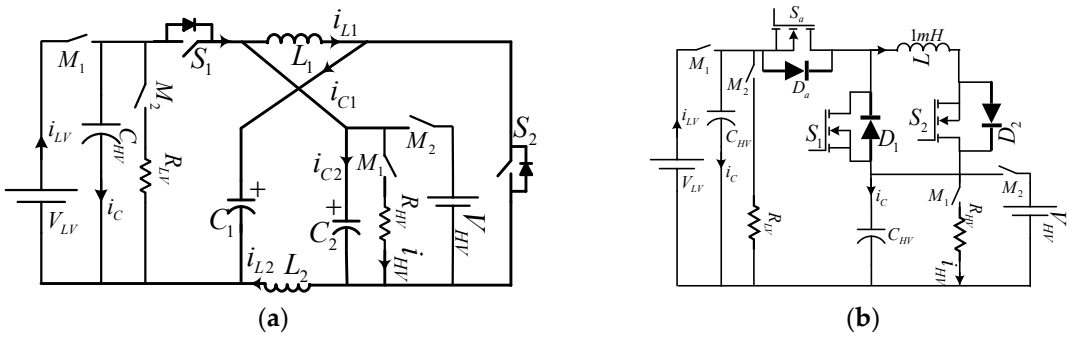


Figure 3. Impedance DC–DC converters. (**a**) Z-source DC–DC converter, (**b**) switched boost DC–DC converter.

A SL-ZS converter is proposed with an enhanced gain by placing switched inductors instead of inductors in the impedance network [19]. However, this topology suffers from a large component count (six power diodes and two inductors higher than the ZS converter) in the switching network. Alternatively, the SL-qZS converter proposed in [20], consists of switched inductors in place of standard inductors in the qZS converter to reduce the capacitor voltage and startup inrush current compared to the SL-ZS converter. However, the downside of this topology is a higher component count. Hossein Fathi et al. [21] proposed an enhanced boost ZS converter (EB-ZSC), achieved by replacing the impedance network with switched impedance to enhance the conversion gain further. Although this topology increases gain, it suffers from a higher component count (four inductors, four capacitors, and five power diodes). Additionally, this topology suffers from the usage of sophisticated control platforms to achieve smoother voltage control in the case of adjustable speed-controlled drive applications. Moreover, with a similar concept of variations in the impedance network either in ZS or qZS as discussed above, there are several other impedance source topologies, such as a diode-assisted qZS (DA-qZS) converter [22], a capacitor-assisted qZS (CS-qZS) converter [22], and an enhanced boost quasi ZS (EB-qZS) converter [23], which are proposed in the literature. Though these topologies are mainly proposed for DC–AC power conversion applications due to high reliability (operation during shoot-through mode), they are equally applicable for bi-directional applications and are widely used in micro/nano-grid applications [18,23].

For most of these topologies, it has been suggested to incorporate switched-inductor, switched-capacitor, and hybrid switched-capacitor/switched-inductor structures resulting in high boosting factors. However, the effect of nonlinearity can be increased by increasing the energy storage

elements in the circuit, which leads to a higher output current and voltage distortion [24]. Additionally, introducing more energy storage elements in the circuit affects the control complexity, total cost, size, volume, losses, and weight of the converter [25,26]. Moreover, these topologies are suffering from the usage of more capacitors and higher capacitor voltage stresses. Additionally, the voltage across most of the capacitors is generally more than the supply voltage in the case of impedance source topologies in order to perform the voltage boost functionality. Hence, high-voltage Z-capacitors should be used, which may increase the volume and system cost. Capacitors are prone to failure in the field operation of power electronic converters [27]. Hence, due to the stricter reliability constraints brought by aerospace, automotive, defense, space, and energy industries, the stresses and usage of capacitors should be reduced to enhance the converter's reliability [28]. Therefore, to enhance the life and converter reliability, either reduction in capacitors usage or voltage stresses on the capacitor is highly recommended [29,30].

In this paper, the LC impedance bi-directional DC–DC converter (LC-BDC) is proposed by placing one inductor between source and half-bridge, and one capacitor between source and the load, as shown in Figure 4 [31]. These small passive components are arranged in such a way that the converter offers several features, such as lower capacitor voltages, which in turn reduces the cost, size, and volume of the converter and also increases the reliability while achieving the desired functionality. This topology reduces the voltage stresses on the device due to the usage of small passive components compared to existing converters in the case of SiC converters, which are less immune to parasitic components. The paper is organized as follows: the working principle, modes of operation, mathematical modeling, and state-space average models of the proposed topology are discussed in Section 2. The concept validation using simulation and experimentation, along with the respective results, are presented in Section 3. Additionally, to demonstrate the effectiveness of the proposed topology, a detailed comparative analysis of the proposed converter and conventional converter is carried out along with the results of the proposed converter. Moreover, a separate simulation-based comparative analysis of the proposed LC converter with eight similar boost/buck-boost converter topologies is presented in Section 4. Finally, conclusions are presented in Section 5 of this paper.

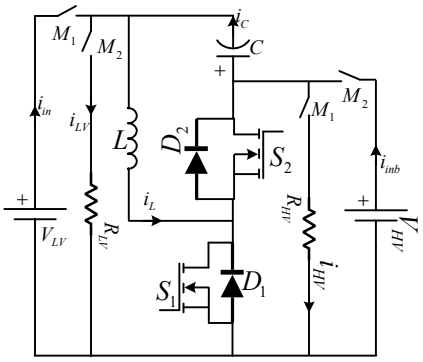


Figure 4. LC impedance bi-directional DC–DC converter (LC-BDC).

2. Proposed System

The LC bidirectional converter shown in Figure 4 is an advanced version of a conventional bidirectional converter and switched boost bidirectional converter, designed to reduce the voltage stresses on the capacitor. The primary function of the inductor is to store energy during the converter "on" period and release the stored energy during the "off" period of the primary device. The inductor is also used to eliminate the current ripple. Another energy storage element, the capacitor, is used to eliminate the ripple in the output voltage in both cases, namely the conventional BDC and the proposed BDC. Switches M_1 and M_2 are unidirectional switches used to realize the bidirectional power flow in the test setup which operate in a complementary fashion. For the forward direction of power flow, M_1 must be in the "on" state, and S_1 acts as the main switch operating at switching frequency, while D_2

acts as a freewheeling diode. Similarly, M_2 must be in the "on" position for the reverse direction of power flow, and S_2 acts as the main switch, which operates at switching frequency, while D_1 acts as a freewheeling diode. V_{LV} and R_{HV} are source and load in boost mode, and V_{HV} and R_{LV} are source and load in buck mode. The gating signals for boost switch (G_1) and buck switch (G_2) complement each other. The duty cycle of boost switch (S_1) and buck switch (S_2) is denoted as δ_1 and δ_2, respectively. T_s represents the switching period of switches S_1 and S_2.

2.1. Boost Operation

The equivalent circuit and idealized waveforms in boost mode of the LC-BDC converter are depicted in Figures 5 and 6, respectively. The converter operation is considered to be in boost mode, during which the switch (S_1) is pulse-modulated and the diode D_2 freewheels. The boost mode operation is further categorized into two sub-modes of operation over a switching period, and the equivalent circuit of each sub-mode is depicted as shown in Figure 7.

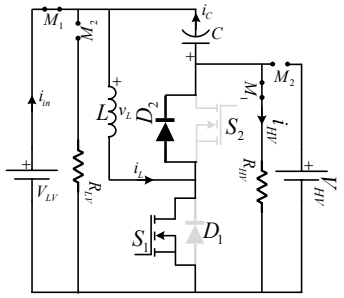


Figure 5. LC bi-directional DC–DC converter in boost mode.

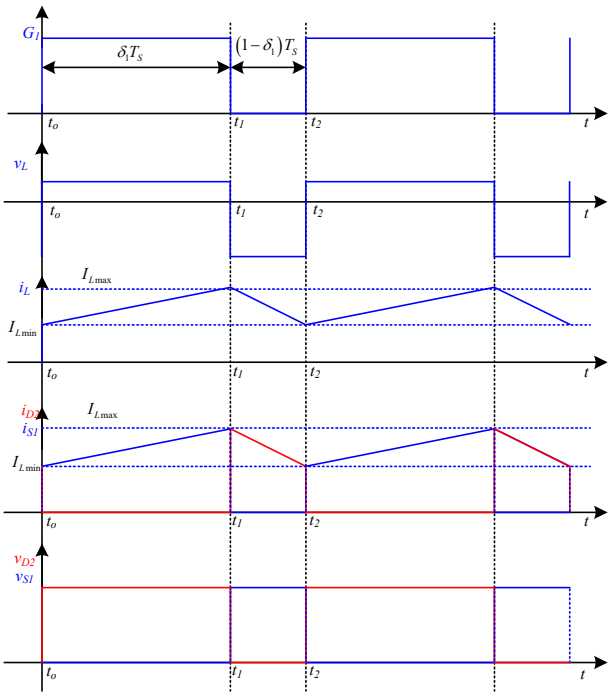


Figure 6. Characteristic waveforms during various boost modes of operation.

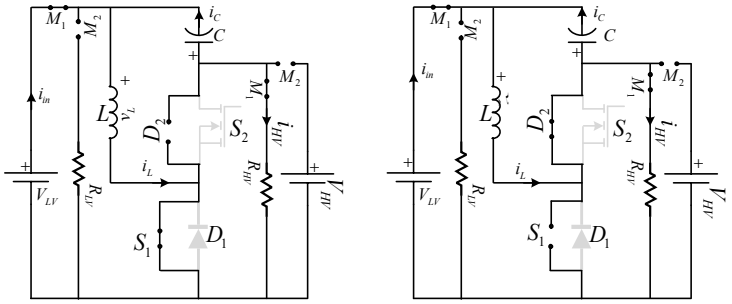


Figure 7. Equivalent circuit of boost operation (**a**) in mode 1 and (**b**) in mode 2.

2.1.1. Mode 1 ($t_0 < t < t_1$): (S_1 ON, D_2 OFF)

In this mode, switch S_1 is turned on by applying a gate signal. The inductor L starts charging linearly through switch S_1, and the capacitor C will discharge through load R_{HV}. Hence, the diode D_2 goes into the "off" state. The equivalent circuit during this mode of operation is shown in Figure 7a. The current through the inductor $L(i_L)$ and the voltage across the capacitor C are given by

$$V_L = V_{LV} = L\frac{di_L}{dt} \tag{1}$$

$$i_L(t) = \frac{V_{LV}}{L}(t - t_0) + i_L(t_0) \tag{2}$$

$$i_C = -\frac{v_{HV}}{R_{HV}} \tag{3}$$

$$v_C(t) = i_{HV}(t)R_{HV} - V_{LV} \tag{4}$$

This mode of operation ends when the gate pulses to switch S_1 are withdrawn.

2.1.2. Mode 2 ($t_1 < t < t_2$): (S_1 OFF, D_2 ON)

At the instant when the gate pulses of switch S_1 are removed, the switch S_1 goes into the "off" state due to which the voltage across the inductor brings the diode D_2 into the forward-biased state. The equivalent circuit during this mode is shown in Figure 7b. In this mode, both inductor and source feed power to the load, and the inductor charges the capacitor. Hence, there is a formation of the LC tank in this mode, which can offer zero voltage switching to the upper switch with the proper selection of the snubber capacitor. In this mode, the current through $L(i_L)$ reaches its minimum value. The current flowing through the inductor $L(i_L)$ and the voltage across the capacitor C are given by

$$V_L = V_{LV} - V_{HV} = L\frac{di_L}{dt} \tag{5}$$

$$i_L(t) = \frac{V_{LV} - V_{HV}}{L}(t - t_1) + i_L(t_1) \tag{6}$$

$$v_C(t) = i_{HV}(t)R_{HV} - V_{LV} \tag{7}$$

$$i_{Cc}(t) = i_L(t) - i_{HV}(t) \tag{8}$$

This mode ends at $t = Ts$ when the gate signal is provided to S_1 in the next switching cycle. Similar operation (Mode 1 and Mode 2) continues for several switching cycles until a power flow is required in the forward direction

2.2. Buck Mode of Operation of LC-BDC Converter

BDC operates in buck mode when there is a requirement of power flow in the reverse direction, and its equivalent circuit is shown in Figure 8. The converter operation is considered to be in reverse buck mode, during which the switch S_2 is pulse-modulated and the diode D_1 in a freewheeling mode. The buck mode of operation is further categorized into two sub-modes (i.e., mode 3 and mode 4) of operation over a switching period. The operating mode from mode 3 to mode 4 in buck mode is similar to the mode 2 to mode 1 of the boost mode of operation, respectively. Figure 9 illustrates the characteristic waveforms of the converter in buck mode, and its equivalent circuits in each sub-mode are depicted as shown in Figure 10.

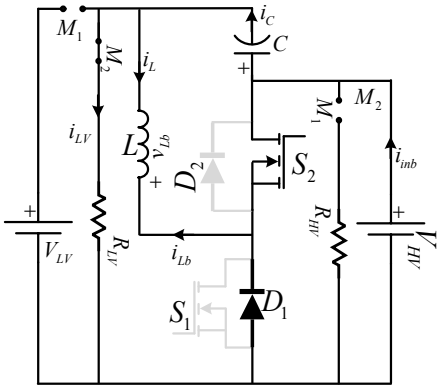


Figure 8. Equivalent circuit in buck mode.

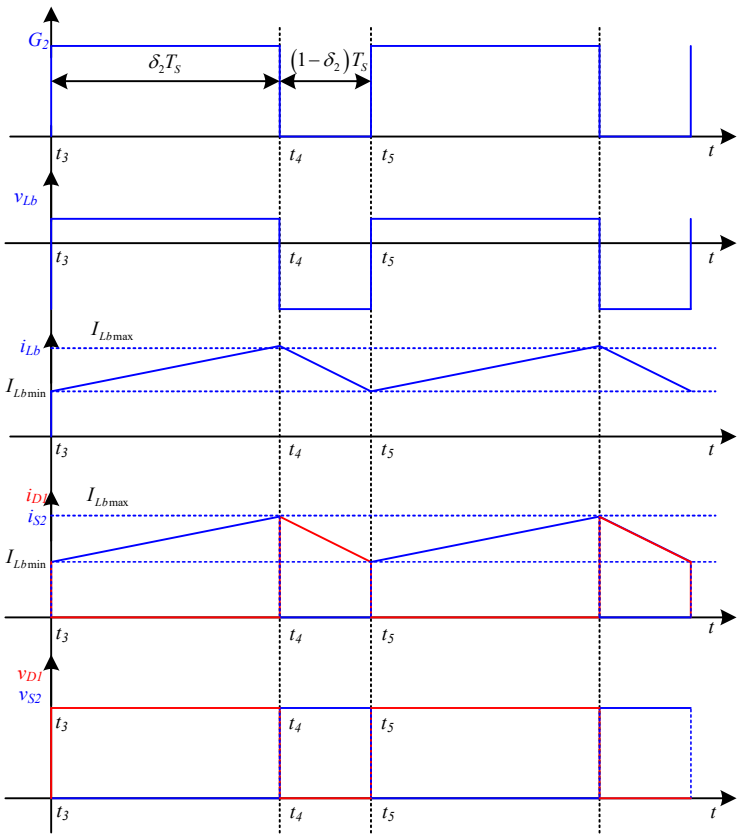


Figure 9. Characteristic waveforms during various modes in buck operation.

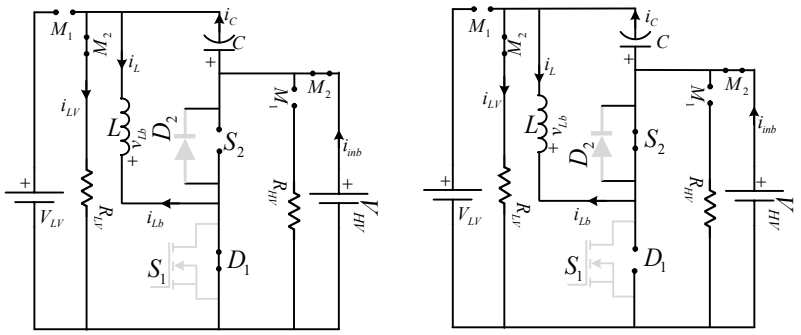


Figure 10. Equivalent circuit of buck operation (**a**) in mode 3 and (**b**) in mode 4.

2.2.1. Mode 3 ($t_3 < t < t_4$): (S_2 ON, D_1 OFF)

This mode starts at $t = t_3$ when the gate signal is given to S_2. At this instant, the main switch S_2 comes into conduction, and the diode D_1 goes into the "off" state. The supply V_{HV} then directly energizes the inductor L. The capacitor is also discharged through the inductor. It leads to the formation of the LC tank, as shown in Figure 10a, similar to mode 2. This feature offers the resonating switching functionality to the upper switch. The current flowing through $L(i_L)$ and the voltage across capacitor C (v_C) are given as

$$v_{Lb}(t) = V_{HV} - v_{LV} \tag{9}$$

$$i_{Lb}(t) = \frac{V_{HV} - v_{LV}}{L}(t - t_3) + i_{Lb}(t_3) \tag{10}$$

$$v_C(t) = V_{HV} - i_{LV}(t)R_{LV} \tag{11}$$

$$i_C(t) = i_{inb}(t) - I_{Lb}(t) \tag{12}$$

This mode continues until the gate pulse of S_2 is withdrawn at $t = t_4$.

2.2.2. Mode 4 ($t_4 < t < t_5$): (S_2 OFF, D_1 ON)

This mode starts at $t = t_4$ when the gate pulses to the main switch are removed. Hence S_2 goes into the "off" state. The voltage across the inductor brings diode D_1 into "on" state, and it continues until $t = t_5$. The energy stored in inductor L discharges through the load. The capacitor charges from the source. During this mode, the current flowing through the inductor L and voltage across the capacitor C can be expressed as

$$v_{Lb}(t) = -i_{LV}(t)R_{HV} \tag{13}$$

$$i_{Lb}(t) = \frac{-v_{LV}}{L}(t - t_4) + i_{Lb}(t_4) \tag{14}$$

$$v_C(t) = V_{HV} - i_{LV}(t)R_{LV} \tag{15}$$

$$i_C(t) = i_{inb}(t) \tag{16}$$

This mode ends at $t = T_s$ when the gate signal is given to S_2 in the next switching cycle. Similar operation of mode 3 and mode 4 continues, for several switching cycles, until power flow is required in the reverse direction.

2.3. State Space Analysis

This section presents the development of a small-signal AC model followed by the derivation of the state-space model equations for one complete switching cycle. For this analysis, few assumptions are considered; (i) the converter is operating in continuous conduction mode, and (ii) there is no trace resistance. For the proposed converter, the state variables are the current through the inductor i_L

and the voltage across the coupling capacitor V_C. A complete derivation of the state-space model and small-signal analysis for boost mode is presented. A similar derivation method can also be used for buck mode. With the inclusion of the parasitic components during both "on" and "off" states, the system can be represented with the help of the state-space model as follows.

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{(r_{on}+r_L)}{L} & 0 \\ 0 & -\frac{1}{C(R+r_C)} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{-R}{(R+r_C)C} \end{bmatrix} \begin{bmatrix} V_{LV} \\ i_{Load} \end{bmatrix} \tag{17}$$

during "off" state:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} \left(\frac{-Rr_c}{(R+r_C)} - r_L\right)\frac{1}{L} & \frac{-R}{(R+r_C)}\frac{1}{L} \\ \frac{R}{(R+r_C)C} & \frac{1}{(R+r_C)C} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{Rr_c}{(R+r_C)} \\ 0 & \frac{-R}{(R+r_C)} \end{bmatrix} \begin{bmatrix} V_{LV} \\ i_{Load} \end{bmatrix} \tag{18}$$

Here, r_{on}—on-state resistance of switching device, r_L—the equivalent series resistance of the inductor, and r_C—equivalent series resistance of the capacitor.

The state-space average model of the converter can be written as follows.

$$\dot{x} = [A_1\delta_1 + A_2(1-\delta_1)]x + [B_1\delta_1 + B_2(1-\delta_1)]U \tag{19}$$

Here, $x = \begin{bmatrix} i_L \\ v_{cc} \end{bmatrix}$, $A_1 = \begin{bmatrix} -\frac{(r_{on}+r_L)}{L} & 0 \\ 0 & -\frac{1}{C(R+r_C)} \end{bmatrix}$, $B_1 = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{-R}{(R+r_C)C} \end{bmatrix}$, $A_2 = \begin{bmatrix} \left(\frac{-Rr_c}{(R+r_C)} - r_L\right)\frac{1}{L} & \frac{-R}{(R+r_C)}\frac{1}{L} \\ \frac{R}{(R+r_C)C} & \frac{1}{(R+r_C)C} \end{bmatrix}$, $B_2 = \begin{bmatrix} \frac{1}{L} & \frac{Rr_c}{(R+r_C)} \\ 0 & \frac{-R}{(R+r_C)} \end{bmatrix}$, $u = \begin{bmatrix} V_{LV} \\ i_{Load} \end{bmatrix}$

Define:

$$\delta_1 T_s = t_1 - t_0 \& t_2 - t_1 = (1-\delta_1)T_s \tag{20}$$

The duty ratio of the main switch S_1 is defined as

$$\delta_1 = \frac{t_1 - t_0}{t_2} \tag{21}$$

The turn-off duty cycle of the main switch S_1 is

$$\delta'_1 = \frac{t_2 - t_1}{t_2} \tag{22}$$

Substituting the duty ratio values from (20)–(22) in Equations (17)–(19) and then incorporating the perturbation effect into the state variables and other variables around the steady-state values gives

$$i_L = I_L + \hat{i}_L, v_{LV} = V_{LV} + \hat{v}_{LV}, v_C = V_C + \hat{v}_C, v_{HV} = V_{HV} + \hat{v}_{HV}, \delta_1 = D_1 + d_1 \tag{23}$$

where D_1 is the duty ratio of the main switch under steady-state condition. After solving the above state-space equation, the steady-state gains of the converter can be obtained as

$$V_C = \frac{D_1 V_{LV}}{1-D_1} \& I_L = \frac{I_{HV}}{1-D_1} \tag{24}$$

Comparing small-signal AC parameters while ignoring the considerably very small second-order quantities, and then solving the equations gives the following two transfer functions.

2.3.1. Control-to-Output Transfer Function

From the small-signal AC model, the control-to-output (output voltage to duty ratio) transfer function can be found under the condition of $\hat{v}_{in} = 0 \& \hat{i}_L = 0$, which is shown in Equation (25).

$$\frac{\hat{v}_o}{1-\hat{d}_1} = \frac{[-R(R+r_c)\times(1+CSr_c)\times \begin{pmatrix} RV_{LV}r_L - R^2V_{LV}{D_1}^2 - R^2V_{LV} + RV_{LV}r_{on} + V_{LV}r_Lr_c + V_{LV}r_cr_{on} + 2R^2V_{LV}D_1 + 2I_{load}R^2r_L \\ +I_{load}R^2r_c + I_{load}R^2r_{on} - 2I_{load}R^2D_1(r_L+r_c) + I_{load}R^2{D_1}^2r_c - I_{load}R^2{D_1}^2r_{on} + LRSV_{LV} \\ +LSV_{LV}r_c + 2I_{load}Rr_Lr_c + I_{load}Rr_cr_{on} + I_{load}LR^2S + I_{load}LRSr_c - 2I_{load}RD_1r_Lr_c - I_{load}LR^2SD_1 \\ -I_{load}R{D_1}^2r_cr_{on} - I_{load}LRSD_1r_c \end{pmatrix}]}{\left[\begin{pmatrix} Rr_L + Rr_c + r_Lr_c - 2R^2D_1 + R^2 \\ +R^2{D_1}^2 - RD_1r_c + RD_1r_{on} + D_1r_cr_{on} \end{pmatrix}\times \begin{pmatrix} CLR^2S^2 - CR^2SD_1r_c + Cr_{on}R^2SD_1 + CR^2Sr_c + Cr_LR^2S + R^2{D_1}^2 - 2R^2D_1 + R^2 \\ +2CLRS^2r_c - CRSD_1r_c^2 + 2Cr_{on}RSD_1r_c + CRSr_c^2 + 2Cr_LRSr_c + LRS - RD_1r_c \\ +r_{on}RD_1 + Rr_c + r_LR + CLS^2r_c^2 + Cr_{on}SD_1r_c^2 + Cr_L{Sr_c}^2 + LSr_c + r_{on}D_1r_c + r_Lr_c \end{pmatrix}\right]} \tag{25}$$

By neglecting parasitic components, it can be simplified as

$$\begin{aligned} \frac{\hat{v}_{HV}}{1-\hat{d}_1} &= \frac{RV_{LV} - LSV_{LV} - 2RV_{LV}D_1 + RV_{LV}{D_1}^2 - I_{load}LRS + I_{load}LRSD_1}{(D_1-1)^2(CLRS^2 + LS + R{D_1}^2 - 2RD_1 + R)} \\ \Rightarrow \frac{v_{HV}}{1-\hat{d}_1} &= \frac{RV_{LV}(1-D_1)^2 - LSV_{LV} - (1-D_1)I_{load}LRS}{(D_1-1)^2(CLRS^2 + LS + R(1-D_1)^2)} \end{aligned} \tag{26}$$

2.3.2. Control-to-Input Transfer Function

From the small-signal AC model, the inductor current-to-control (input current to duty ratio) transfer function can be found under the condition of $\hat{v}_{LV} = 0 \& \hat{i}_{Load} = 0$, which is shown in Equation (27).

$$\frac{\hat{i}_{in}}{1-\hat{d}_1} = \frac{-(R+r_c)\begin{pmatrix} 2R^2V_{LV} - I_{load}R^3{D_1}^2 - RV_{LV}r_c - I_{load}R^3 + V_{LV}r_cr_{on} + 2I_{load}R^3D_1 + 2R^2V_{LV}D_1 + I_{laod}R^2r_L + I_{load}R^2r_{on} + I_{laod}Rr_Lr_c \\ +I_{load}Rr_cr_{on} - CR^3SV_{LV}D_1 - CI_{load}R^3Sr_L - CI_{laod}R^3Sr_C - CR^2SV_{LV}r_L - CRSV_{LV}r_c^2 - 2CR^2SV_{LV}r_c + CSV_{LV}r_c^2r_{on} \\ -CI_{laod}LR^3S^2 - CLR^2S^2V_{LV} + CR^3SV_{LV}V{D_1}^2 - CI_{load}LR^2Sr_C - CI_{load}R^3S{D_1}^2r_C + CI_{load}R^3S{D_1}^2r_{on} - CRSV_{LV}r_Lr_C \\ +CRSV_{LV}r_cr_{on} - CLRS^2V_{LV}r_c + 2CI_{load}R^3SD_1r_L + 2CI_{load}R^3SD_1r_C + CR^2SV_{LV}D_1r_c + CI_{loaad}RSr_Lr_c^2 + CI_{load}RSr_c^2r_{on} \\ +CI_{load}R^2Sr_cr_{on} + CI_{load}LR^3S^2D_1 + 2CI_{load}R^2SD_1r_Lr_c + CI_{load}LR^2S^2D_1r_c + CI_{load}R^2S{D_1}^2r_{on}r + RV_{LV}r_{on} \end{pmatrix}}{\left[\begin{pmatrix} Rr_L + Rr_c + r_Lr_c - 2R^2D_1 + R^2 \\ +R^2{D_1}^2 - RD_1r_c + RD_1r_{on} + D_1r_cr_{on} \end{pmatrix}\times \begin{pmatrix} CLR^2S^2 - CR^2SD_1r_c + Cr_{on}R^2SD_1 + CR^2Sr_c + Cr_LR^2S + R^2{D_1}^2 - 2R^2D_1 + R^2 \\ +2CLRS^2r_c - CRSD_1r_c^2 + 2Cr_{on}RSD_1r_c + CRSr_c^2 + 2Cr_LRSr_c + LRS - RD_1r_c + r_{on}RD_1 \\ +Rr_c + r_LR + CLS^2r_c^2 + Cr_{on}SD_1r_c^2 + Cr_LSr_c^2 + LSr_c + r_{on}D_1r_c + r_Lr_c \end{pmatrix}\right]} \tag{27}$$

By neglecting parasitic components, it can be simplified as

$$\begin{aligned} \frac{\hat{i}_{in}}{1-\hat{d}_1} &= \frac{2V_{LV} - I_{load}R(1-D_1) + CRV_{LV}S}{(1-D_1)(CLRS^2 + LS + R{D_1}^2 - 2RD_1 + R)} \\ \Rightarrow \frac{i_{in}}{1-\hat{d}_1} &= \frac{RV_{LV}(1-D_1)^2 - LSV_{LV} - I_{load}(1-D_1)}{(1-D_1)(CLRS^2 + LS + R(1-D_1)^2)} \end{aligned} \tag{28}$$

2.3.3. Step and Bode Responses of LC-BDC

From the derived transfer functions, the step responses of various variables are presented in Figure 11. From these results, it can be understood that the variations in input currents and capacitor voltages for both line and load disturbance are low in the case of the proposed converter compared to the existing converter. Moreover, the step responses reveal that the proposed LC-BDC converter response is the same for inductor current and capacitor current and capacitor voltage against the duty ratio, whereas input current transients against duty ratio variations are reduced in LC-BDC. It can also be noted that in the case of supply variations, the transient responses of the inductor current, output voltage, load current, and capacitor voltage are improved.

2.3.4. Ripple Capacitor Voltage

From the charge balance equation and further simplification of the above Equation (25) in the steady-state, the capacitor ripple voltage can be calculated as

$$\Delta v_{Ccboost} = \frac{D_1V_{HV}}{CRF_S} \tag{29}$$

From (29), the capacitor value can be sized to minimize the voltage ripple across the capacitor.

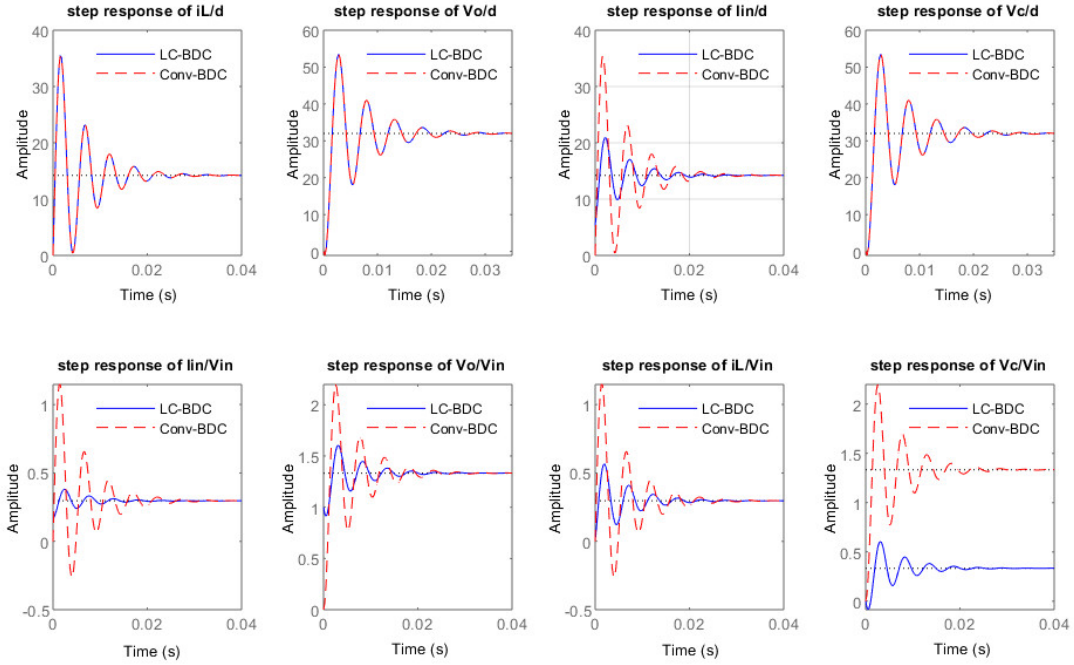


Figure 11. Step responses of the inductor current, output voltage, load current, and capacitor voltage transfer functions with respect to duty ratio and input voltage of LC-BDC and conventional converter.

3. Experimental Results and Discussion

The proposed LC impedance bi-directional dc-dc converter has been successfully validated through experiments in both boost and buck modes. The parameters considered for the experimental validations are summarized in Table 1. The experimental setup of the proposed converter is shown in Figure 12. The system performance is evaluated in both steady-state and transient conditions while feeding power to two series-connected 12 V, 50 W lamp load under various test conditions for the 18 V DC to 24 V DC conversion in forwarding boost mode, and 24 V DC to 18 V DC conversion in reverse buck mode. The inductor current, load current, and capacitor voltage waveforms are captured in both boost and buck modes for both conventional and proposed converters. Comparative analysis through experimental results was carried out, as explained below. In the case of the conventional converter, there is a need for two capacitors (C_{HV} plays a vital role in boost mode, and C_{LV} plays a vital role in buck mode), whereas, in the case of the proposed converter, there is a need for only one capacitor C, which can take care of the functionality of the above mentioned two capacitors in the respective modes. It can be observed that two capacitors are used in the realization of the conventional converter, whereas only one capacitor is used for the realization of the proposed LC-BDC, as shown in Table 1.

Table 1. Parameters of the proposed converter.

	Proposed		**Conventional**	
Parameter name	Boost Mode (LV to HV)	Buck Mode (HV to LV)	Boost Mode (LV to HV)	Buck Mode (HV to LV)
Input voltage (V)	18	24	18	24
Output voltage (V)	24	18	24	18
Output voltage ripple, %	≤0.50	≤0.50	≤0.50	≤0.50
Load	12 V, 50 W of 2 Lamps in series	12 V, 50 W of 2 Lamps in series	12 V, 50 W of 2 Lamps in series	12 V, 50 W of 2 Lamps in series
Output current (A)	4	3.20	4	3.20
Switching frequency (kHz)	10	10	10	10
Inductor	0.5 mH		0.5 mH	
Filter capacitors	500 µF/500 V(HV Side)	500 µF/500 V (LV Side)	500 µF/500 V (intermediate stage)	

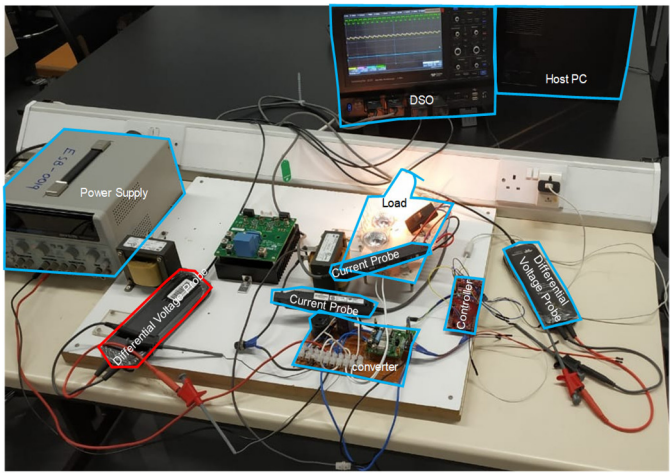


Figure 12. Experimental Setup of Power Converter.

The gate signal of the lower switch, inductor current, load current, and capacitor voltage for four switching cycles are captured and presented in Figures 13–16. From Figure 14, it can be seen that the peak value of the inductor current is 6.17 A in the conventional converter, whereas it is 6.07 A in the proposed converter for the same load current, as shown in Figure 15. From Figure 16, it can be seen that the voltage across the capacitor is 23.20 V in the case of the conventional converter, whereas it is 5.10 V in the case of the proposed converter. Hence, there is 78.02% of capacitor voltage reduction in the proposed converter as compared to the conventional converter for the same input/output voltage conversion.

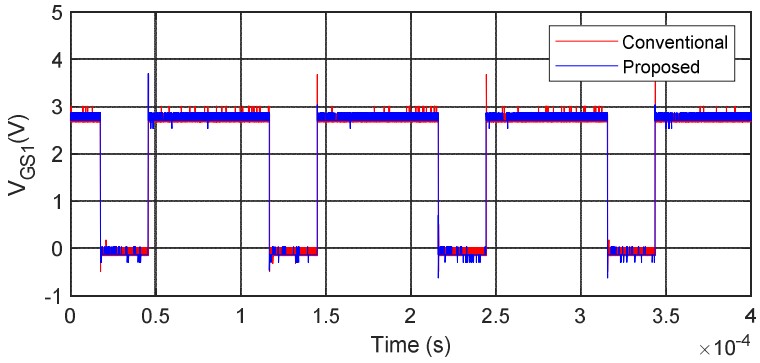


Figure 13. Gate voltage of lower switch (S_1) in LC-BDC (Blue), and conventional BDC (red).

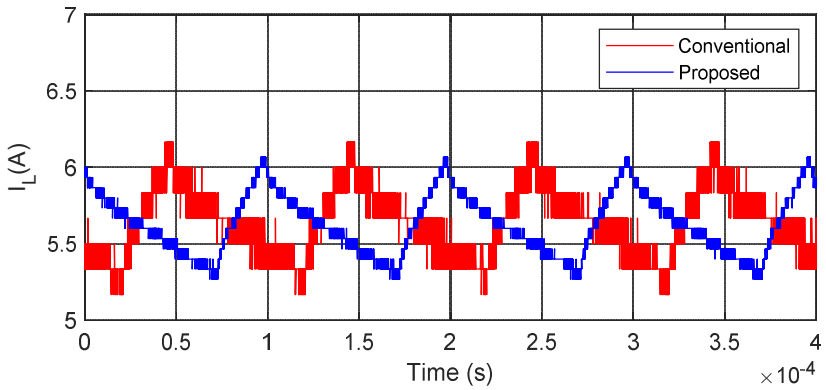


Figure 14. Inductor current in LC-BDC (Blue), and conventional BDC (red).

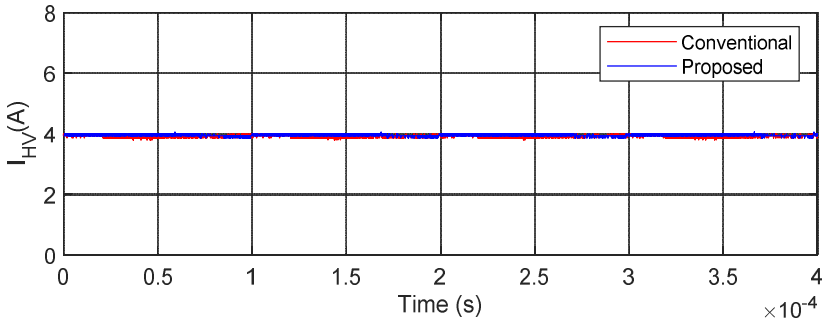


Figure 15. Load current in LC-BDC (Blue), and conventional BDC (red).

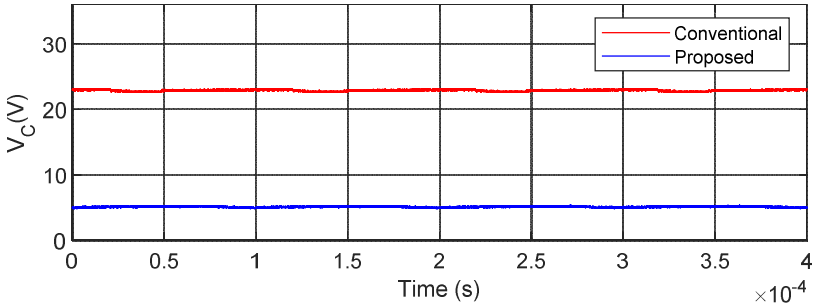


Figure 16. Capacitor voltages in LC-BDC (Blue), and conventional BDC (Red).

In Figures 17–19, respectively, a zoomed view of respective parameters is presented during both "on" and "off" state. From these figures, peak values during both transient and steady-state can be measured as listed in Table 2.

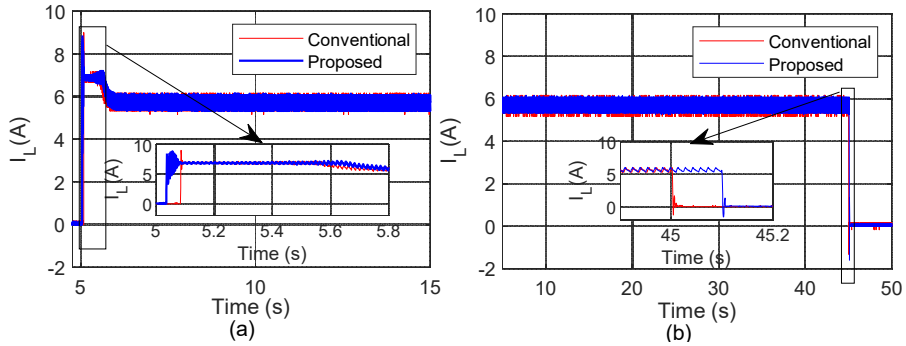


Figure 17. Inductor current of LC-BDC (blue) and conventional BDC (red) converter during (**a**) "on" and (**b**) "off" states.

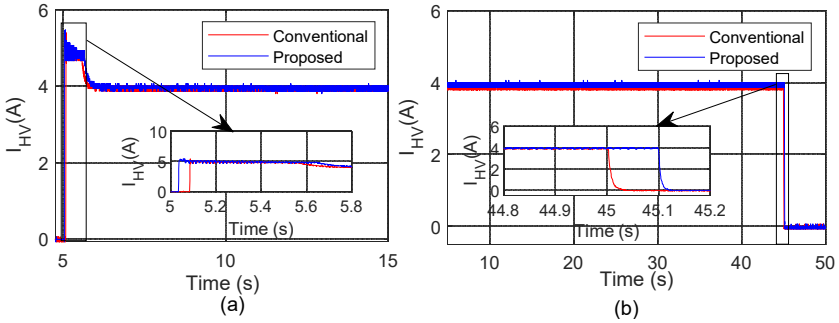


Figure 18. Load current of LC-BDC (blue) and conventional BDC (red) converter during (**a**) "on" and (**b**) "off" states.

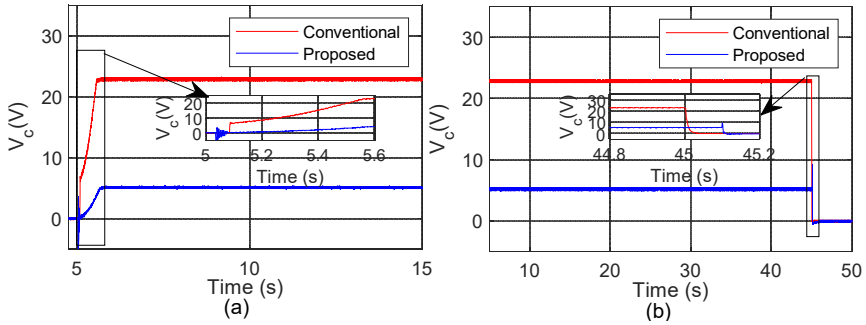


Figure 19. Capacitor voltage of LC-BDC (blue) and conventional BDC (red) converter during (**a**) "on" and (**b**) "off" states.

Table 2. Comparison of the various parameter during both transient and steady state for the proposed and conventional converters.

Peak Values	Conventional		Proposed	
	Transient	Steady State	Transient	Steady State
Capacitor voltage	23.20 V	23.20 V	4.80 V	5.20 V
Inductor current	8.80 A	6.00 A	8.80 A	6.00 A
Load Current	5.20 A	4.00 A	5.20 A	4.00 A

Form Table 3, it can be observed that the proposed converter not only offer its best performance during steady-state conditions but also the exhibits same best performance during transient conditions in terms of capacitor voltage stresses.

Table 3. Comparison of ripple values of capacitor voltage, inductor current and load current for the proposed and conventional converters.

Ripples	Conventional	Proposed
Capacitor voltage	0.50 V	0.34 V
Input current	0.99 A	0.79 A
Load Current	0.13 A	0.13 A

For the ripple content investigation, a zoomed view of the inductor current, load current, and capacitor voltages are presented in Figures 20–23, respectively. The summary of the ripple content for both converter topologies is tabulated in Table 3. From this table, it can be understood that there is a 0.4% reduction of ripple content in capacitor voltages and inductor current for the same content of load current ripples.

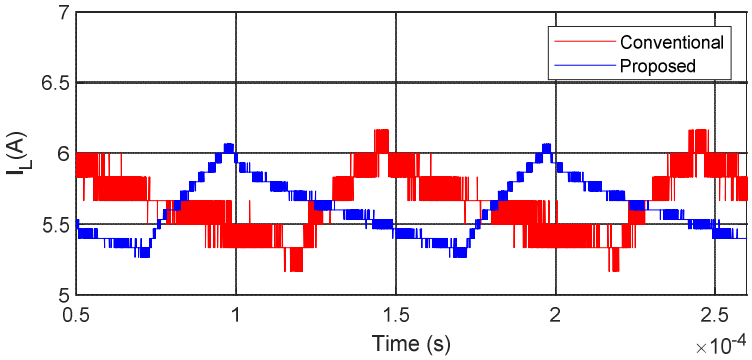


Figure 20. Zoomed view of inductor current for ripple analysis LC-BDC (blue), and conventional converter (red).

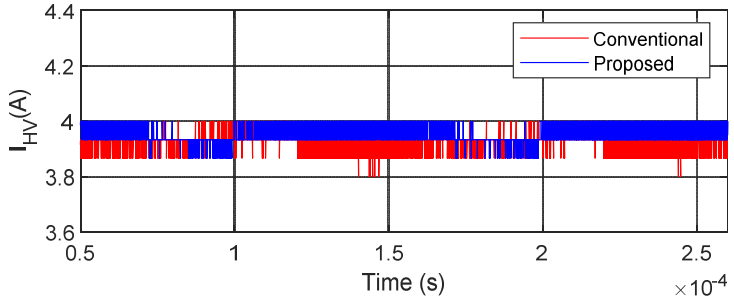


Figure 21. Zoomed view of load current for ripple analysis in LC-BDC (blue), and conventional converter (red).

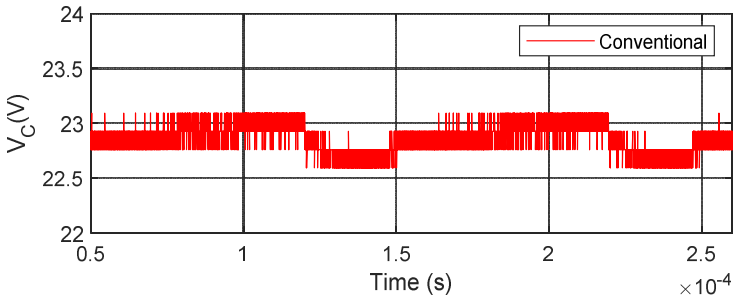


Figure 22. Zoomed view of capacitor voltage in the conventional converter for ripple analysis.

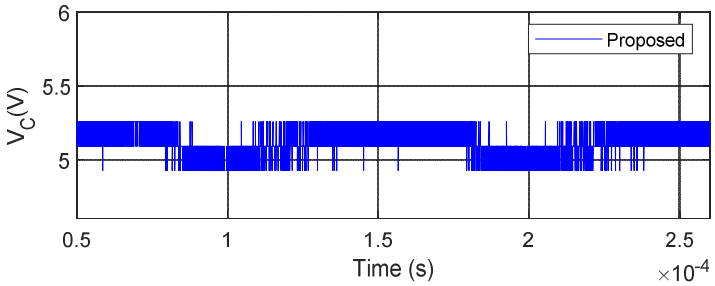


Figure 23. Zoomed view of capacitor voltage in the proposed converter for ripple analysis.

For the reverse buck mode of operation, the gating signal of the upper switch, inductor current, load current, and capacitor voltage for four switching cycles have been captured, as presented in Figures 24–27. From Figure 25, it can be seen that the peak value of the inductor current is 3.61 A in the case of conventional converter, whereas it is 3.62 A in the case of the proposed converter for the same load current as shown in Figure 26. From Figure 27, it can be seen that the voltage across the capacitor is 16.40 V in the case of conventional converter, whereas it is 7.80 V in the case of the proposed converter. A capacitor voltage reduction of 35.80% can be witnessed in this mode of operation.

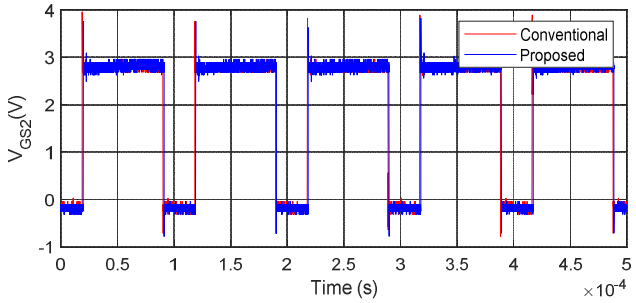


Figure 24. Gate voltage of upper switch (S_2) in LC-BDC (Blue), and conventional BDC (red).

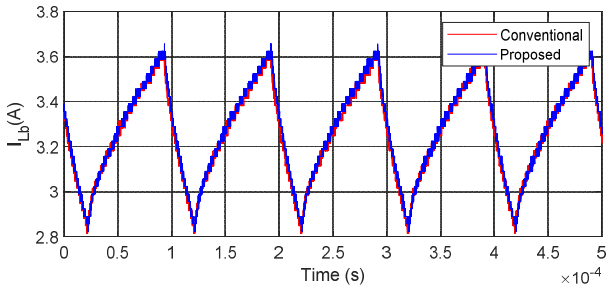


Figure 25. Inductor current in LC-BDC (Blue), and conventional BDC (red).

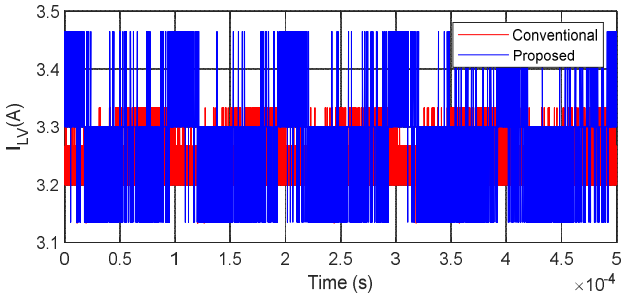


Figure 26. Load current in LC-BDC (Blue), and conventional BDC (red).

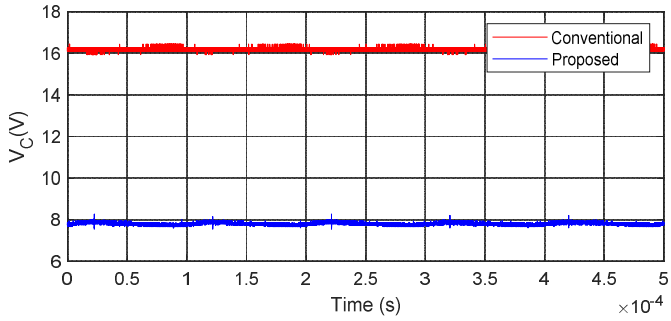


Figure 27. Capacitor voltages in LC-BDC (Blue), and conventional BDC (red).

For the critical investigation, results have been captured under various test conditions to assess the proposed converter suitability for various applications like smooth turn-on, faster load turn-off, and converter on- and off-switching with variable duty. During these conditions, captured inductor current, load current, and capacitor voltage are shown in Figures 28–30, respectively. Moreover, in these figures, a zoomed view of respective parameters is presented during both turn-on and turn-off. From these figures, peak values during both transient and steady states can be measured as listed in Table 4. Form the Table 4, and it can be observed that the proposed converter not only offers its best performance during steady-state conditions but also exhibits the same best performance during transient conditions in terms of capacitor voltage stresses.

Table 4. Comparison of the various parameter during both transient and steady states for the proposed and conventional converters.

Peak Values	Conventional		Proposed	
	Transient	Steady State	Transient	Steady State
Capacitor voltage	5.60 V	16.40 V	6.20 V	7.80 V
Inductor current	4.54 A	3.65 A	4.62 A	3.68 A
Load Current	4.54 A	3.65 A	4.62 A	3.68 A

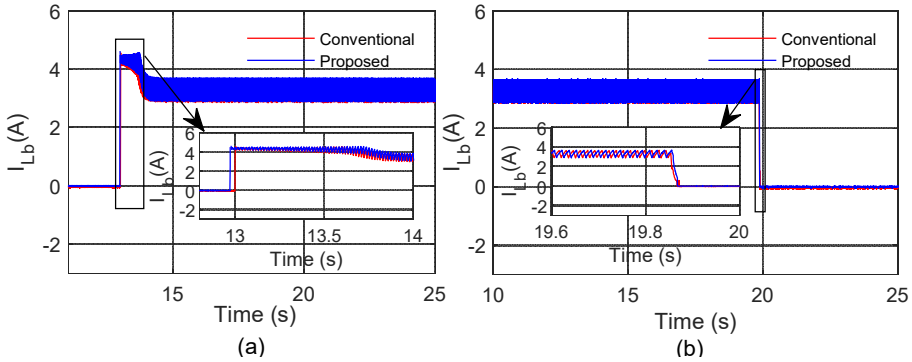


Figure 28. Inductor current of LC-BDC (blue) and conventional BDC (red) converter during (**a**) turn on (**b**) turn off.

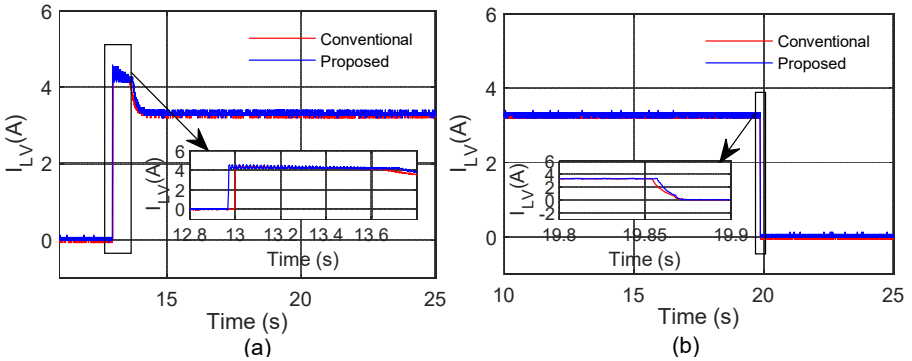


Figure 29. Load current of LC-BDC (blue) and conventional BDC (red) converter during (**a**) turn on and (**b**) turn off.

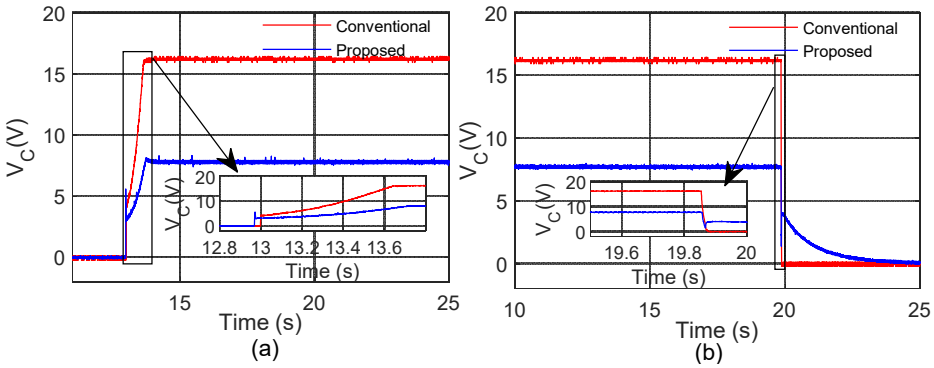


Figure 30. Capacitor voltage of LC-BDC (blue) and conventional BDC (red) converter during (**a**) turn on and (**b**) turn off.

For the ripple content investigation, a zoomed view of the inductor current, load current, and capacitor voltages are presented in Figures 31–34, respectively. The summary of the ripple content in both the converters is tabulated in Table 5. From this table, it can be extracted that there is a 0.3% reduction of ripple content in capacitor voltages ripples for the same load current.

Table 5. Comparison of Ripple Values for The Proposed and Conventional Converters in Buck Mode.

Ripples	Conventional	Proposed
Capacitor voltage	1.40%	1.10%
Inductor current	16.65%	16.65%
Load Current	4.70%	5.00%

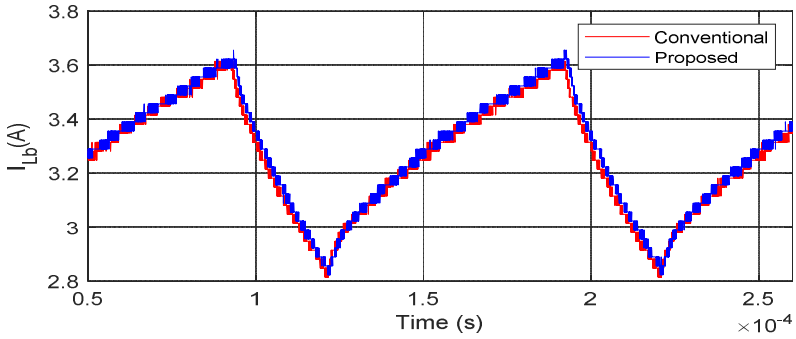


Figure 31. Zoomed view of inductor current for ripple analysis LC-BDC (blue), and conventional converter (red).

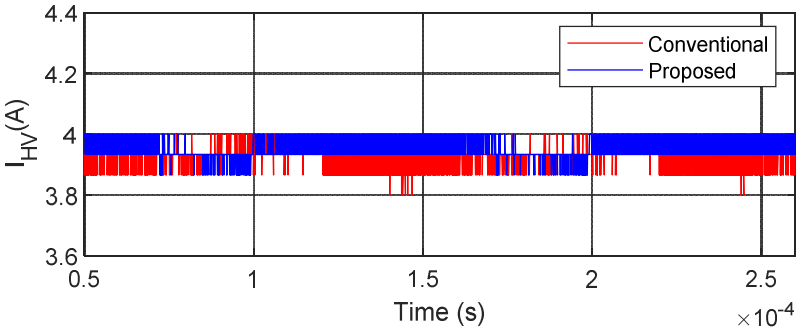


Figure 32. Zoomed view of load current for ripple analysis in LC-BDC (blue), and conventional converter (red).

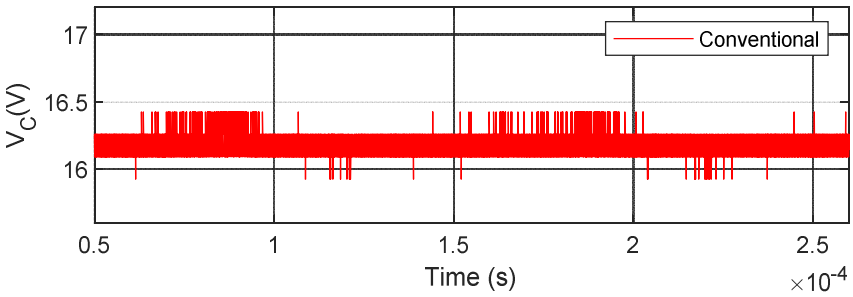


Figure 33. Zoomed view of capacitor voltage in the conventional converter for ripple analysis.

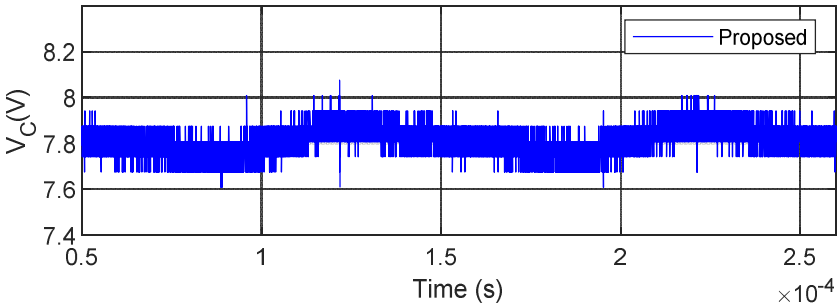


Figure 34. Zoomed view of capacitor voltage in the proposed converter for ripple analysis.

4. Comparative Analysis

Another set of simulations is performed to investigate the performance of the above topologies, and simulation parameters are listed in Table 6 as mentioned below. By using these sets of simulations, various performance parameters such as voltage gains, capacitor voltages, and losses were investigated.

These simulations are carried out for various output voltages ranging from 36 V to 108 V with the dc input voltage of 24 V, i.e., voltage gain ranging from 1.5 to 4.5. With the help of this data, a comparative analysis is presented in the following subsections.

Table 6. Parameters considered for comparative analysis.

Parameter	Value
Input DC Voltage	24 V
Switching Frequency	10 kHz
Output line voltage (RMS)	36 V–108 V
Load Power	500 W

4.1. No. of Components

As mentioned earlier, by changing the impedance network configurations, various topologies are proposed, and hence each topology has a different number of components. The number of components used for different topologies are listed and presented as a bar chart shown in Figure 35. From this chart, it is clear that the proposed converter and conventional BDC require fewer components compared to other topologies.

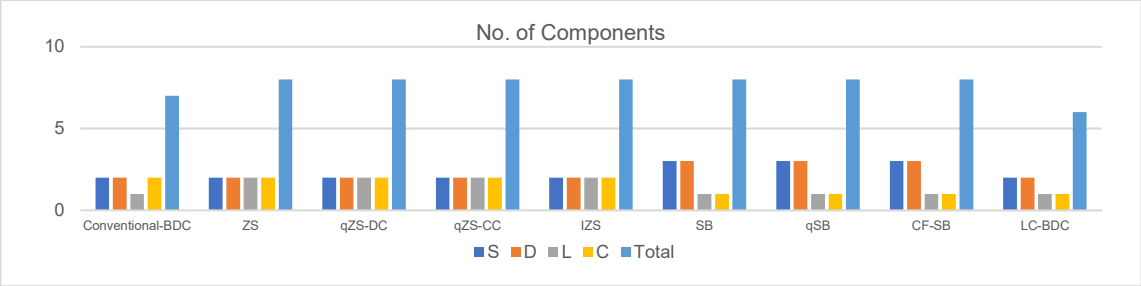


Figure 35. Bar chart of no. of components used in different topology.

4.2. Capacitor Voltage Stress

Since capacitors used in various topologies are different, total voltage stresses in all capacitors are calculated for comparison purposes. Here in Figure 36, the total capacitor stresses are plotted, while 24 V DC is converted into a range of DC voltage ranging from 36 V to 108 V. From this figure, it is clear that capacitor stresses are low in the case of the proposed converter.

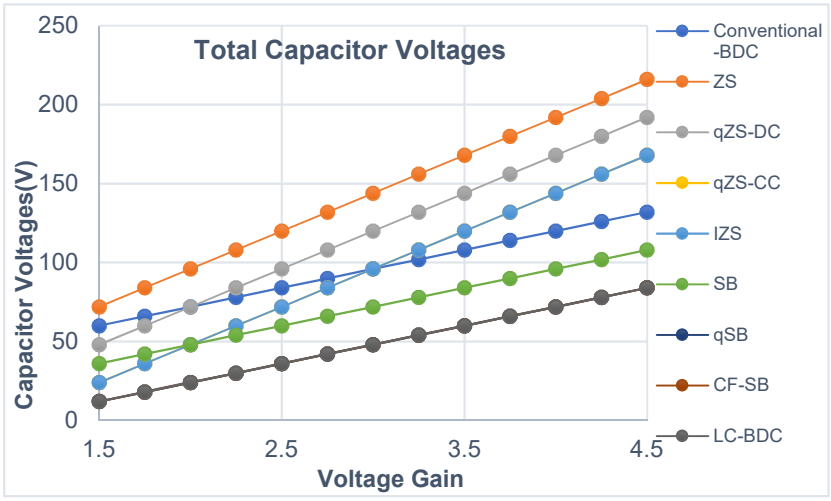


Figure 36. Total capacitor stress in different topology.

4.3. Efficiency Analysis and Loss Comparison

To perform the converter efficiency analysis, the parasitic resistance of inductors and capacitors, and the diode forward conduction losses are considered in this paper. The parasitic resistance of inductor and capacitor are r_L and r_C, respectively, and forward conduction loss of diode due to forward voltage (V_F) was assumed to be the same in all topologies for comparative analysis. The impact of the parasitic resistances and the forward voltage drop of the main power devices (MOSFETs) are also considered in this manuscript. Equivalent circuits of all the considered buck-boost bi-directional converters with the inclusion of various parasitic components are presented in Figure 37 for the efficiency calculations. Formulas derived for losses and efficiencies are presented in Table 7.

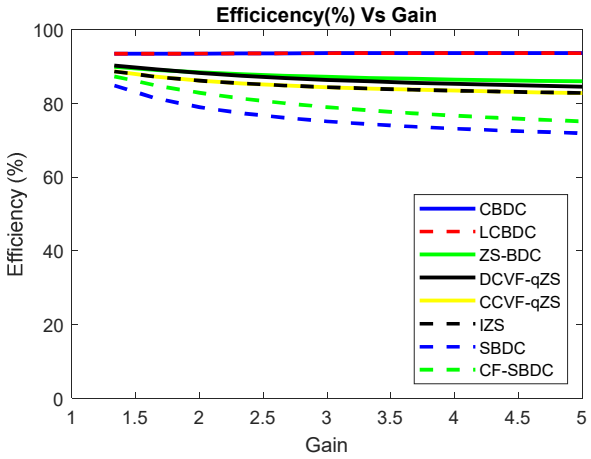


Figure 37. Efficiency comparison of various topologies.

Table 7. Comparison of various parameters (device, inductor and capacitor RMS currents, overall losses, and efficiency) of existing and proposed topologies.

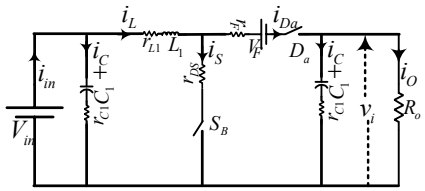
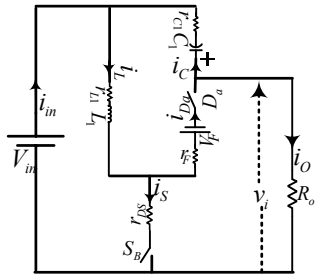
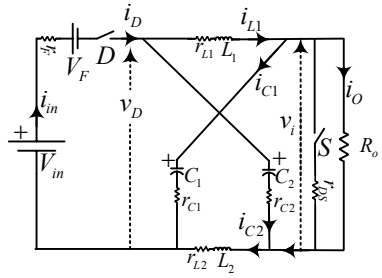
Topology	Equivalent Circuit Diagram	RMS Currents of Various Components	Parameters
Conv-BDC		$I_{srms} = \frac{I_o\sqrt{D}}{1-D}$ $I_{Drms} = \frac{I_o}{\sqrt{1-D}}$ $I_{Lrms} = \frac{I_o}{1-D}$ $I_{Crms} = I_o\sqrt{\frac{D}{1-D}}$	$\eta = \frac{1}{1+\left\{\frac{r_L+Dr_{DS}}{(1-D)^2R_L}+\frac{R_F+Dr_c}{(1-D)R_L}+\frac{V_f}{V_o}+F_sC_oR_L\right\}}$ $M_{VDS} = \frac{1}{(1-D)\left\{\frac{r_L+Dr_{DS}}{(1-D)^2R_L}+\frac{R_F+Dr_c}{(1-D)R_L}+\frac{V_f}{V_o}+F_sC_oR_L\right\}}$
LC-BDC		$I_{Srms} = \frac{I_o\sqrt{D}}{1-D}$ $I_{Drms} = \frac{I_o}{\sqrt{1-D}}$ $I_{Lrms} = \frac{I_o}{1-D}$ $I_{Crms} = I_o\sqrt{\frac{D}{1-D}}$	$\eta = \frac{1}{1+\left\{\frac{r_L+Dr_{DS}}{(1-D)^2R_L}+\frac{R_F+Dr_c}{(1-D)R_L}+\frac{V_f}{V_o}+F_sC_oR_L\right\}}$ $M_{VDS} = \frac{1}{(1-D)\left\{\frac{r_L+Dr_{DS}}{(1-D)^2R_L}+\frac{R_F+Dr_c}{(1-D)R_L}+\frac{V_f}{V_o}+F_sC_oR_L\right\}}$
ZS-BDC		$I_{Srms} = \frac{I_o\sqrt{D}}{1-2D}$ $I_{Drms} = \frac{(1-D)^{3/2}}{(1-2D)}I_o$ $I_{Lrms} = \frac{1-D}{1-2D}I_o$ $I_{Crms} = \frac{\sqrt{D(1-D)}}{(1-2D)}I_o$	$\eta = \frac{1}{1+\left\{\begin{array}{l}\frac{Dr_{Ds}}{(1-2D)^2R_L}+\frac{(1-D)^2}{(1-2D)}\frac{V_f}{V_o}+\frac{(1-D)^3}{(1-2D)^2}\frac{R_F}{R_L}++2\left(\frac{1-D}{1-2D}\right)^2\frac{r_L}{R_L}\\+\frac{F_sC_oR_L}{2}+\frac{r_{LF}}{R_L}+2\frac{D(1-D)}{(1-2D)^2}\frac{r_c}{R_L}+\frac{(M_{Vdc}-1)^2}{12\left(L_fF_s\right)^2}(1-2D)^2r_{CF}R_L\end{array}\right\}}$ $M_{VDS} = \frac{(1-D)}{(1-2D)\left\{\begin{array}{l}\frac{Dr_{Ds}}{(1-2D)^2R_L}+\frac{(1-D)^2}{(1-2D)}\frac{V_f}{V_o}+\frac{(1-D)^3}{(1-2D)^2}\frac{R_F}{R_L}++2\left(\frac{1-D}{1-2D}\right)^2\frac{r_L}{R_L}\\+\frac{F_sC_oR_L}{2}+\frac{r_{LF}}{R_L}+2\frac{D(1-D)}{(1-2D)^2}\frac{r_c}{R_L}+\frac{(M_{Vdc}-1)^2}{12\left(L_fF_s\right)^2}(1-2D)^2r_{CF}R_L\end{array}\right\}}$

Table 7. *Cont.*

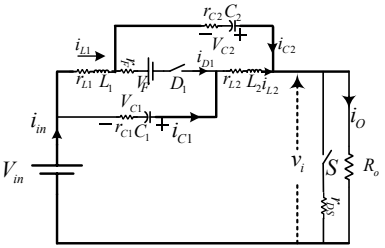
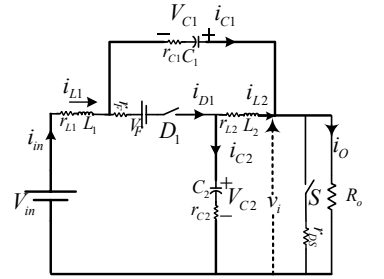
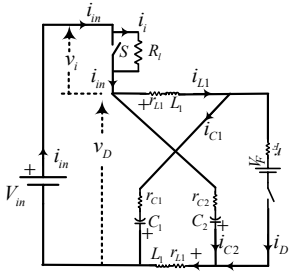
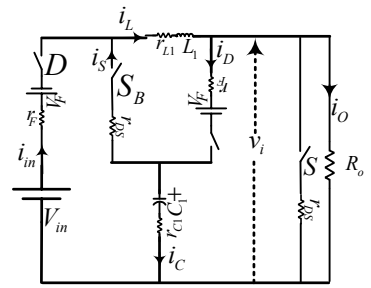
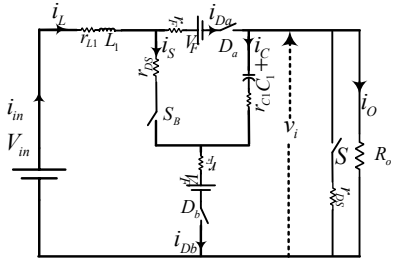
Topology	Equivalent Circuit Diagram	RMS Currents of Various Components	Parameters
DCVF-qZS BDC		$I_{Srms} = \frac{I_o\sqrt{D}}{1-2D}$ $I_{Drms} = \sqrt{1-D}I_o$ $I_{Lrms} = \frac{1-D}{1-2D}I_o$ $I_{Crms} = \frac{\sqrt{D(1-D)}}{(1-2D)}I_o$	$\eta = \frac{1}{1+\left\{\begin{array}{l}\frac{Dr_{Ds}}{(1-2D)^2R_L} + (1-D)\frac{V_f}{V_o} + (1-D)^2\frac{R_F}{(1-D)R_L} + 2\left(\frac{1-D}{1-2D}\right)^2\frac{r_L}{R_L} \\ + \frac{F_sC_oR_L}{2} + \frac{r_{LF}}{R_L} + \frac{(M_{Vdc}-1)^2}{12\left(L_fF_s\right)^2}(1-2D)^2r_{CF}R_L + 2\frac{D(1-D)}{(1-2D)^2}\frac{r_c}{R_L}\end{array}\right\}}$ $M_{VDS} = \frac{(1-D)}{(1-2D)\left\{\begin{array}{l}\frac{Dr_{Ds}}{(1-2D)^2R_L} + (1-D)\frac{V_f}{V_o} + (1-D)^2\frac{R_F}{(1-D)R_L} + 2\left(\frac{1-D}{1-2D}\right)^2\frac{r_L}{R_L} \\ + \frac{F_sC_oR_L}{2} + \frac{r_{LF}}{R_L} + \frac{(M_{Vdc}-1)^2}{12\left(L_fF_s\right)^2}(1-2D)^2r_{CF}R_L + 2\frac{D(1-D)}{(1-2D)^2}\frac{r_c}{R_L}\end{array}\right\}}$
CCVF-qZS BDC		$I_{Srms} = \frac{I_o\sqrt{D}}{1-2D}$ $I_{Drms} = \frac{\sqrt{1-D}}{(1-2D)}I_o$ $I_{Lrms} = \frac{1-D}{1-2D}I_o$ $I_{Crms} = \frac{\sqrt{D(1-D)}}{(1-2D)}I_o$	$\eta = \frac{1}{1+\left\{\begin{array}{l}\frac{Dr_{Ds}}{(1-2D)^2R_L} + \frac{(1-D)}{(1-2D)}\frac{V_f}{V_o} + \frac{(1-D)}{(1-2D)^2}\frac{R_F}{R_L} + \frac{F_sC_oR_L}{2} + \frac{r_{LF}}{R_L} \\ + 2\left(\frac{1-D}{1-2D}\right)^2\frac{r_L}{R_L} + 2\frac{D(1-D)}{(1-2D)^2}\frac{r_c}{R_L} + \frac{(M_{Vdc}-1)^2}{12\left(L_fF_s\right)^2}(1-2D)^2r_{CF}R_L\end{array}\right\}}$ $M_{VDS} = \frac{(1-D)}{(1-2D)\left\{\begin{array}{l}\frac{Dr_{Ds}}{(1-2D)^2R_L} + \frac{(1-D)}{(1-2D)}\frac{V_f}{V_o} + \frac{(1-D)}{(1-2D)^2}\frac{R_F}{R_L} + \frac{F_sC_oR_L}{2} + \frac{r_{LF}}{R_L} \\ + 2\left(\frac{1-D}{1-2D}\right)^2\frac{r_L}{R_L} + 2\frac{D(1-D)}{(1-2D)^2}\frac{r_c}{R_L} + \frac{(M_{Vdc}-1)^2}{12\left(L_fF_s\right)^2}(1-2D)^2r_{CF}R_L\end{array}\right\}}$
IZS-BDC		$I_{Srms} = \frac{I_o\sqrt{D}}{1-2D}$ $I_{Drms} = \frac{(1-D)^{1/2}}{(1-2D)}I_o$ $I_{Lrms} = \frac{1-D}{1-2D}I_o$ $I_{Crms} = \frac{\sqrt{D(1-D)}}{(1-2D)}I_o$	$\eta = \frac{1}{1+\left\{\begin{array}{l}\frac{Dr_{Ds}}{(1-2D)^2R_L} + \frac{(1-D)}{(1-2D)}\frac{V_f}{V_o} + \frac{(1-D)}{(1-2D)^2}\frac{R_F}{R_L} + \frac{F_sC_oR_L}{2} + \frac{r_{LF}}{R_L} \\ + 2\left(\frac{1-D}{1-2D}\right)^2\frac{r_L}{R_L} + 2\frac{D(1-D)}{(1-2D)^2}\frac{r_c}{R_L} + \frac{(M_{Vdc}-1)^2}{12\left(L_fF_s\right)^2}(1-2D)^2r_{CF}R_L\end{array}\right\}P_o}$ $M_{VDS} = \frac{(1-D)}{(1-2D)\left\{\begin{array}{l}\frac{Dr_{Ds}}{(1-2D)^2R_L} + \frac{(1-D)}{(1-2D)}\frac{V_f}{V_o} + \frac{(1-D)}{(1-2D)^2}\frac{R_F}{R_L} + \frac{F_sC_oR_L}{2} + \frac{r_{LF}}{R_L} \\ + 2\left(\frac{1-D}{1-2D}\right)^2\frac{r_L}{R_L} + 2\frac{D(1-D)}{(1-2D)^2}\frac{r_c}{R_L} + \frac{(M_{Vdc}-1)^2}{12\left(L_fF_s\right)^2}(1-2D)^2r_{CF}R_L\end{array}\right\}P_o}$

Table 7. *Cont.*

Topology	Equivalent Circuit Diagram	RMS Currents of Various Components	Parameters
SB-BDC		$I_{Srms} = \frac{I_o\sqrt{D}}{1-2D}$ $I_{Drms} = \frac{(1-D)^{1/2}}{(1-2D)} I_o$ $I_{Lrms} = \frac{1}{1-2D} I_o$ $I_{Crms} = \frac{2\sqrt{D(1-D)}}{(1-2D)} I_o$	$\eta = \frac{1}{1+\left\{ \begin{array}{l} \frac{2Dr_{Ds}}{(1-2D)^2 R_L} + \frac{(1-D)}{(1-2D)} \frac{2V_f}{V_o} + \frac{(1-D)}{(1-2D)^2} \frac{2R_F}{R_L} \\ +F_s C_o R_L + \left(\frac{1}{1-2D}\right)^2 \frac{r_L}{R_L} + \frac{4D(1-D)}{(1-2D)^2} \frac{r_c}{R_L} \end{array} \right\} P_o}$ $M_{VDS} = \frac{(1-D)}{(1-2D)\left\{ \begin{array}{l} \frac{2Dr_{Ds}}{(1-2D)^2 R_L} + \frac{(1-D)}{(1-2D)} \frac{2V_f}{V_o} + \frac{(1-D)}{(1-2D)^2} \frac{2R_F}{R_L} \\ +F_s C_o R_L + \left(\frac{1}{1-2D}\right)^2 \frac{r_L}{R_L} + \frac{4D(1-D)}{(1-2D)^2} \frac{r_c}{R_L} \end{array} \right\} P_o}$
CFSB-BDC		$I_{Srms} = \frac{I_o\sqrt{D}}{1-2D}$ $I_{Drms} = \frac{(1-D)^{1/2}}{(1-2D)} I_o$ $I_{Lrms} = \frac{1}{1-2D} I_o$ $I_{Crms} = \frac{2\sqrt{D(1-D)}}{(1-2D)} I_o$	$\eta = \frac{1}{1+\left\{ \begin{array}{l} \frac{2Dr_{Ds}}{(1-2D)^2 R_L} + \frac{(1-D)}{(1-2D)} \frac{2V_f}{V_o} + \frac{(1-D)}{(1-2D)^2} \frac{2R_F}{R_L} \\ +F_s C_o R_L + \left(\frac{1}{1-2D}\right)^2 \frac{r_L}{R_L} + \frac{4D(1-D)}{(1-2D)^2} \frac{r_c}{R_L} \end{array} \right\} P_o}$ $M_{VDS} = \frac{(1-D)}{(1-2D)\left\{ \begin{array}{l} \frac{2Dr_{Ds}}{(1-2D)^2 R_L} + \frac{(1-D)}{(1-2D)} \frac{2V_f}{V_o} + \frac{(1-D)}{(1-2D)^2} \frac{2R_F}{R_L} \\ +F_s C_o R_L + \left(\frac{1}{1-2D}\right)^2 \frac{r_L}{R_L} + \frac{4D(1-D)}{(1-2D)^2} \frac{r_c}{R_L} \end{array} \right\} P_o}$

By using the above-derived formulas, the efficiencies and non-ideal voltage conversion ratios of each topology with respect to gain are presented in Figures 37 and 38, respectively. From these results, it can be observed that the efficiency is higher in conventional BDC and LC-BDC compared to other existing topologies. Moreover, it can be seen that the voltage conversion ratio is more linear in the case of conventional BDC, and the proposed converter compared to other existing topologies. In all existing topologies (except conventional BDC), it can be noted that the performance of the converter is becoming poor as the gain is increased further from the designed gain value.

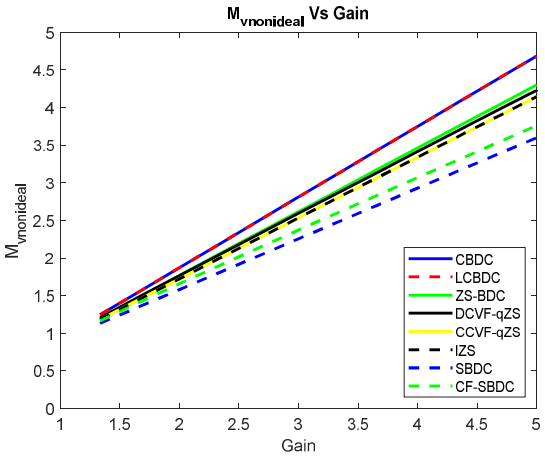


Figure 38. Voltage conversion ratio comparison of various topologies.

5. Conclusions

In this paper, a new LC bi-directional DC–DC converter utilizing small passive components has been proposed and successfully validated. Experimental results proved that there is a reduction of 75% and 35.8% in capacitor voltage for 24 V to 18 V conversion in boost mode, and 18 V to 24 V conversion in buck mode, respectively. Moreover, there is a reduction of one capacitor compared to conventional BDC for the same conversion. In this paper, the proposed converter performance in both transient and steady-state conditions is investigated and presented. This investigation reveals that the proposed converter is able to offer superior performance in both transient and steady-state conditions. Moreover, a comparative analysis of the proposed converter with the conventional BDC, Z-source converter, discontinues current quasi Z-source converter, continues current quasi Z-source converter, improved Z-source converter, switched boost converter, current-fed switched boost converter, and quasi switched boost converter is presented. This comparative analysis proved that the proposed converter offers superior performance compared to existing converters for the same conversion ratio.

Author Contributions: Idea, Conceptualization, Formal Analysis, Investigation, Methodology, Software, Validation, and Writing—Original Draft are the main contributions of D.R.; Funding acquisition, Project administration, Resources, Validation, Visualization and Writing—review & editing are the main contributions of R.D.; H.R. and S.M. contributed in terms of Validation and Writing—review & editing. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

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