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Design of Differential Variable-Gain Transimpedance Amplifier in 0.18 μm SiGe BiCMOS

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Abstract: This paper presents two new inductorless differential variable-gain transimpedance amplifiers (DVGITIA) with voltage bias controlled variable gain designed in TowerJazz's 0.18 μm SiGe BiCMOS technology (using CMOS transistors only). Both consist of a modified differential cross-coupled regulated cascode preamplifier stage and a cascaded amplifier stage with bias-controlled gain-variation and third-order interleaving feedback. The designs have wide measured transimpedance gain ranges of 24.5–60.6 dB Ω and 27.8–62.8 dB Ω with bandwidth above 6.42 GHz and 5.22 GHz for DVGITIA designs 1 and 2 respectively. The core power consumptions are 30.7 mW and 27.5 mW from a 1.8 V supply and the input referred noise currents are 10.3 pA/ $\sqrt{\text{Hz}}$ and 21.7 pA/ $\sqrt{\text{Hz}}$. The DVGITIA designs 1 and 2 have a dynamic range of 40.4 μA to 3 mA and 76.8 μA to 2.7 mA making both suitable for real photodetectors with an on-chip photodetector capacitive load of 250 fF. Both designs are compact with a core area of 100 $\mu\text{m} \times 85 \mu\text{m}$.

Keywords: cross-coupled; differential; inductorless; regulated cascode; third-order interleaving feedback; transimpedance; variable-gain

1. Introduction

The demand for data transmission will increase immensely in the future due to applications such as cloud-computing and the internet of things, causing an insufficient capacity for the current Wi-Fi frequency channels used. Currently, the millimeter wave band is being taken and developed for the 5G communication network. Hence, visible light communication (VLC) offers another solution as the unused visible light spectrum (400 THz–800 THz) can also be used for wireless communication due to the dwindling available RF spectrum [1,2]. The light signal can be transmitted through short distances via light-emitting diodes (LEDs) or long distances via fiber optic cables which are deployed across the world [1,2]. Data is transmitted by modulating the light signal through controllable LEDs [1,2]. The key advantages of VLC include the fact that light signals can be easily confined within opaque walls, thus keeping data transmission secure within a room, rapid replacement of fluorescent lighting to LED lighting as well as the low costs of the LEDs themselves [1,2]. This allows them to be well-suited for a wide variety of near-field wireless communication applications such as secure office/home and vehicle-to-vehicle or vehicle-to-traffic-light communication [1,2].

The transimpedance amplifier (TIA) is a chip block that converts and amplifies current input signal into voltage output [1–3]. Other than for VLC, TIAs can also be utilized in other applications such as magnetic resonance imaging for healthcare, infra-red night vision and even sensors, such as accelerometers and gyroscopes, that have microelectromechanical systems (MEMS) components as

long as there is a current signal output to input into the TIA [3]. However, as different applications require different design specifications [3], this paper focuses on TIA designs for VLC.

The VLC transceiver consists of a transmitter and a receiver module with the transmitter having a photodiode and the receiver having a photodetector to transmit and receive the light signal respectively [3–7]. A key limitation of VLC systems is the low efficiency of the electro-optical conversion for the photodiode and vice versa which is solved by improvements in LED efficiency as well as the need for larger photodetectors in the receiver to absorb sufficient light [1,2]. In the receiver module, the TIA is the first circuit block after the photodetector that converts its current output into voltage [4–7]. As the first block, the TIA determines important parameters such as the bandwidth, noise, sensitivity and dynamic range, for subsequent blocks and thus, for the entire VLC system [3–7]. Silicon-based processes, such as the complementary metal-oxide semiconductor (CMOS) and Silicon–Germanium (SiGe), have been widely used for previous TIA designs due to the fact of its technological maturity, low-cost, high reliability at high frequency and on-chip integrability with photodiodes and photodetectors [4–7]. Both CMOS and bipolar-junction transistors (BJTs) can be made together on the same chip in a SiGe BiCMOS process.

The major challenge for TIA designs is to overcome the gain–bandwidth trade-off, with the bandwidth limited by the large photodetector parasitic capacitive load (C_{pd}) that drags down the frequency of the dominant pole located at the TIA input. Thus, most TIA designs try to compensate C_{pd} by lowering the input impedance Z_{in} of the TIA design [4–8]. A popular technique to do this is through the regulated cascode (RGC) design [4–7], while additional bandwidth-enhancing techniques, such as interleaving feedbacks [6,7], capacitive degeneration [7] and active-inductive peaking [8], are also common to introduce zeros to counter the dominant pole. Another technique is to use parallel pathways, such as via PMOS transistors, from the input to increase transconductance at input and, thus, lower Z_{in} [6,8]. To keep the TIA size small and, thus, low cost, an inductorless design is always preferred as on-chip inductors are large in physical size [4–8].

A differential design is also advantageous over a single-ended design for three reasons. Firstly, the common-mode noise would be cancelled [7,8]. Secondly, other types of noise such as power supply and substrate-coupling noise would be lowered [7,8]. Thirdly, it would not require a large AC-eliminating capacitor within the single to differential converter in order to input a required differential signal into the limiting amplifier (LA) block after the TIA [7,8].

In order to increase the dynamic range of the input signal, the amplifier should have a variable gain function in order to lower the gain when the input signal is high to prevent gain compression and thus non-linearity of the output signal [5,7]. This is because the input signal strength from a usual photodetector with typical responsivity and optical modulation index has a large input signal current range of 150 μ A to 0.9 mA due to the variable user-required optical power from –6 to 2 dBm [7,9].

The variable-gain function can use gain-varying techniques from variable-gain amplifier (VGA) designs. Previous papers have explored having voltage-controlled gain varying transistors in the load of common-source amplifiers [10–12] with separate PMOS and NMOS pathways for dB-linearity [11,12] as well as reconfigurable DC-offset cancellation to remove DC differences between both differential sides [13]. Ideally, when varying gain, the gain-controlling pole and peaking-controlling zero should be adjusted together to ensure a flat frequency response and prevent instability [11,12].

The proposed inductorless differential variable-gain TIA (DVG-TIA) in this paper builds on the authors' previous design in [7], with measurement results from the taped-out chips presented here. Two similar designs are shown, both consisting of a novel cross-coupled regulated cascode input stage and a gain-varying gain stage. The designs are unique for several reasons. Firstly, they take a single-ended input with a single C_{pd} to become a differential output while maintaining the low input impedance of a RGC configuration. Secondly, they have an additional automatic small negative feedback at the input to lower input impedance even further. The bandwidth is maintained throughout the gain stage by using interleaving feedback and capacitive degeneration. Although the designs are

taped-out in TowerJazz's 0.18 μm SiGe BiCMOS technology, only CMOS transistors are used and thus they are compatible with a normal bulk CMOS process [7].

This paper is organized as such. Section 2 discusses the literature review of previous TIA designs and design techniques. Section 3 discusses the two proposed TIA designs in this paper, their design novelty, layout and measurement setup. Section 4 presents the post-layout simulation before chip tape-out as well as the measurement results after chip tape-out. Section 5 discusses the results in Section 4 and compares them with other recent papers and finally Section 6 is the conclusion.

2. Literature Review

2.1. Regulated Cascode TIA

The goal of a TIA design is to lower the input impedance Z_{in} as much as possible and thus the simplest TIA design is a common-gate (CG) with a Z_{in} of $1/g_m$ [4–7], where g_m is the transconductance of the transistor. As shown in Figure 1, an active photodetector is modelled with a C_{pd} load and current input i_{pd} into the TIA input at V_{in} . The regulated cascode (RGC) is a popular TIA design as the internal feedback allows M_1 to act as both a CG and common-source (CS) amplifier, lowering Z_{in} further to $1/g_{M1}(1 + g_{M2}R_2)$.

Figure 1. Standard RGC TIA design with additional cascode transistor M_3 [3–7].

The additional cascode transistor M_3 helps to eliminate the Miller effect that arises due to the CS M_2 transistor by increasing the separation between the input V_{in} from the output V_{rgc} [6,7], thus helping to increase the bandwidth while having little impact on the gain of RGC TIA. The transimpedance gain $Z_{T,RGC}$ and the poles are calculated as [7]:

$$Z_{T,RGC} = \frac{V_{rgc}}{V_{in}} = \frac{R_1}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \quad (1)$$

$$\omega_{p1} = \frac{1}{\{R_3 \parallel (r_{oM1} + R_1)\}(C_{pd} + C_i)}, \quad \omega_{p2} = \frac{1}{R_1 \parallel (r_{oM1} + R_3)C_o} \quad (2)$$

where pole ω_{p1} is located at V_{in} , pole ω_{p2} is located at V_{rgc} , C_i and C_o are the capacitive loads of the transistors at V_{in} and V_{rgc} respectively. The problem with this RGC TIA design is that the dominant pole ω_{p1} is still located at V_{in} due to the insufficient lowering of Z_{in} for a typical C_{pd} value such as 250 fF, causing C_{pd} to still have a significant impact on the bandwidth of the TIA. Thus, further modification on the RGC is required to further lower Z_{in} and isolate C_{pd} from bandwidth determination [4–7].

2.2. Cross-Coupling TIA

Apart from just one feedback in the RGC TIA design, there could be a cross-coupled design as shown in Figure 2 with dual feedbacks to the gates of $M_{1A|1B}$ in order to create more zeros and increase the bandwidth as in [14].

Figure 2. Cross-coupling single-ended TIA design with RGC input design as in [14].

Care must be taken to ensure that the dual feedback loops do not cause instability shown by frequency response peaking and, thus, resulting in oscillation of the amplifier. $R_{1A|1B}$ contributes to both the gain of the TIA as well as to the feedback gain. Hence, to prevent instability and oscillation, the value of $R_{1A|1B}$ and thus the gain is limited. Another disadvantage of this design is that it does not have a differential output.

The cross-coupling design can also be made to be a differential design shown in Figure 3 as in [15]. In this design, components of both sides are identical in size to equalize the DC voltages at V_{out+} and V_{out-} . Since the cross-coupling is also a dual feedback, it likewise helps to generate the opposite small-signal of V_{out+} at V_{out-} although it is not yet entirely equal in magnitude.

Figure 3. Cross-coupling differential TIA design with simple CG input design as in [15].

However, a key disadvantage is that the input of both sides is a simple CG with a higher Z_{in} of $1/g_{M1}$ (without considering the cross-coupling) since there is no CS circuit directly from the input. Furthermore, there is an entire dummy circuit with an additional large C_{pd} on the side without the input signal which both wastes chip area and reduces bandwidth. Lastly, precious voltage headroom is wasted by adding M_2 as a cascode yet simply biasing it with a fixed V_{BIAS} , effectively limiting the gain to reduce the Miller effect. Thus, although the output is a differential signal, it is more costly in terms of price, gain and bandwidth.

3. Design Process of Proposed DVGITIA

3.1. Proposed Input Stage of the DVGITIA Design

The proposed DVGITIA input stages shown in Figure 4 is similar to the authors' previous design in [7], with added feedback transistors $M_{3A|3B}$ and $M_{4A|4B}$ for designs 1 and 2 respectively. It is a

cross-coupled design similar to [14], but it uniquely takes a single-ended input with a single C_{pd} to become a differential output while maintaining the low Z_{in} RGC configuration unlike in [15].

Figure 4. (a) Simplified and (b) transistor-level schematic of the proposed DVGTTA input stage design 1 and (b) design 2.

The transistors $M_{1A|1B}$ act as both a CG and CS, with the input signal just from a single side V_{in} while M_{1B} is still able to be a cascode transistor for the CS M_{2B} . $R_{1A|1B}$ determines the gain of the input stage while R_2 determines the peaking of the frequency response. This is done because it controls the difference in input signal between $M_{2A|2B}$, whereby M_{2A} is the biasing of the M_{1A} CG and M_{2B} is CS of the opposite side. Because there are only three components in the V_{DD} instead of four unlike in [15] while still maintaining the cascode configuration, this allows for greater voltage headroom across the gain resistor $R_{1A|1B}$ and thus, increases gain for the TIA. Even though the functions of transistors on both sides are different, they are the same size to equalize DC similar to [15].

An additional novelty is that there is an automatic small negative feedback in both designs back to the input at V_{in} that introduces another zero at V_{in} and lowers Z_{in} further, compensating the large C_{pd} load and increasing the bandwidth. As shown in Figure 4, the difference in designs 1 and 2 is that for design 1, the feedback is directly from V_{mid+} and V_{mid-} to the gates of $M_{3A|3B}$, while in design 2, it is from the nodes V_{g2-} and V_{g2+} respectively, in the gain stage. For design 1, the advantage is that the feedback path is shorter in layout since it is from the same stage at V_{mid} , yet this would cause additional parasitic capacitance at V_{mid} which is a more sensitive node along the signal path than V_{g2} . Conversely, for design 2, the feedback has a longer path in layout yet does not burden V_{mid} . Although the difference seems minor, it affects the location of the poles and zeros, hence, affecting the frequency response in which would be shown later.

The calculated $Z_{in}(0)$ of the first DVGTTA input stage is:

$$Z_{in,DVGTTA} = \frac{1}{g_{M1A}} \times \frac{1}{(1 + g_{M2B}R_{1B})(1 + g_{M3A}R_{1A})} \quad (3)$$

where $g_{M1A|1B} = 11\text{mS}$, $g_{M2A|2B} = 8.5\text{mS}$, $g_{M3A|3B} \approx g_{M4A|4B} \approx 1\text{mS}$ from simulation results. Both designs 1 and 2 do not have very different Z_{in} . Hence, the calculated $Z_{in,DVGTTA}$ is lower than $Z_{in,RGC}$.

To find the input stage gain, the transfer functions of all feedback loops are listed in Table 1:

Table 1. Table of gain functions at DC in DVGTTA input stage.

Gain *	V_o/V_i	Transfer Function	Gain *	V_o/V_i	Transfer Function
$A_{CS,M1A}$	V_{mid-}/V_{mid+}	$-g_{M1A}R_{1A}$	$A_{CS,M3A}$	V_{in}/V_{mid+}	$-g_{M3A}R_{1A}$
$A_{CS,M1B}$	V_{mid+}/V_{mid-}	$-g_{M1B}R_{1B}$	$A_{CS,M3B}$	V_{ib}/V_{mid-}	$-g_{M3B}R_{1B}$
$A_{CG,M1A}$	V_{mid+}/V_{in}	≈ 1	$A_{CS,M4A}$	V_{in}/V_{g2-}	$-g_{M4B}R_{G2B}$
$A_{CG,M1B}$	V_{mid-}/V_{ib}	≈ 1	$A_{CS,M4B}$	V_{ib}/V_{g2+}	$-g_{M4A}R_{G2A}$
$A_{CS,M2B}$	V_{ib}/V_{in}	$-g_{M1B}R_{1B}$			

* Care must be taken in defining the gains A; in this paper, the negative sign of CS amplifier gain is inside A.

Hence, by identifying and combining all feedback loops and taking $V_{in} = I_{in} \times Z_{in}$, transimpedance gain $Z_{T,in}$ of the first DVGTTA input stage positive side $Z_{T,in1+}$ and negative side $Z_{T,in1-}$ is calculated as loops from V_{in} to V_{mid+} : loop 1: $\frac{V_{mid+}}{V_{in}}$, loop 2: $\frac{V_{ib}}{V_{in}} \times \frac{V_{mid-}}{V_{ib}} \times \frac{V_{mid+}}{V_{mid-}}$, -loop 3: $\frac{V_{in}}{V_{mid-}}$:

$$Z_{T,in1+}^* = Z_{in} \times \frac{V_{mid+}}{V_{in}} = \left| \frac{1 + g_{M1B}R_{1B}g_{M1B}R_{1B} - g_{M3A}R_{1A}}{g_{M1A}(1 + g_{M2B}R_{1B})(1 + g_{M3A}R_{1A})} \right| \quad (4)$$

*Note that since the signals at V_{in} and V_{mid+} have the same sign, the absolute value is taken for $Z_{T,in1+}$.

Loops from V_{IN} to V_{mid-} : loop 1: $\frac{V_{mid-}}{V_{in}}$, loop 2: $\frac{V_{ib}}{V_{in}} \times \frac{V_{mid-}}{V_{ib}}$, loop 3: $\frac{V_{mid+}}{V_{in}} \times \frac{V_{mid-}}{V_{mid+}}$, -loop 4: $\frac{V_{ib}^*}{V_{mid-}}$:

$$Z_{T,in1-}^* = Z_{in} \times \frac{V_{mid-}}{V_{in}} = - \left| \frac{1 + g_{M1B}R_{1B} + g_{M1A}R_{1A} - g_{M3B}R_{1B}}{g_{M1A}(1 + g_{M2B}R_{1B})(1 + g_{M3A}R_{1A})} \right| \quad (5)$$

*Note that the negative loop is taken from V_{ib} instead of V_{in} for simplification as $A_{CS,M2B}$ is only one-directional, i.e., V_{in}/V_{ib} does not exist. Also, since the signals at V_{in} and V_{mid-} are opposite in phase, thus the negative of the absolute value for $Z_{T,in1-}$ is taken.

For the second DVGTTA input stage $Z_{T,in2+}$ and $Z_{T,in2-}$, the transistors for the negative loops are $M_{4A|4B}$ instead of $M_{3A|3B}$ and the transfer functions are substituted accordingly:

$$Z_{T,in2+} = Z_{in} \times \frac{V_{mid+}}{V_{in}} = \left| \frac{1 + g_{M1B}R_{1B}g_{M1B}R_{1B} - g_{M4A}R_{1A}}{g_{M1A}(1 + g_{M2B}R_{1B})(1 + g_{M4A}R_{1A})} \right| \quad (6)$$

$$Z_{T,in2-} = Z_{in} \times \frac{V_{mid-}}{V_{in}} = - \left| \frac{1 + g_{M1B}R_{1B} + g_{M1A}R_{1A} - g_{M4B}R_{1B}}{g_{M1A}(1 + g_{M2B}R_{1B})(1 + g_{M4A}R_{1A})} \right| \quad (7)$$

The differential gain is the difference between both gains which are of opposite polarities, hence the absolute values are added together to get $Z_{T,in1,diff}$ and $Z_{T,in2,diff}$ of DVGTTA designs 1 and 2.

3.2. Proposed DVGTTA Gain Stage

Both DVGTTA designs 1 and 2 share the same gain stage design as in [7] as shown in Figure 5. There is a source-follower $M_{G1A|1B}$ followed by four CS amplifiers differential pairs $M_{G2,3,4,5}$ that give gains $A_{G2,3,4,5}$, while three interleaving feedback transistor pairs $M_{F2,3,4}$ produce negative feedback gains $A_{F2,3,4}$. The feedbacks introduce zeros at $V_{g2,3,4}$, thus boosting bandwidth by gain peaking [6,7].

A unique advantage of the proposed DVGTTA gain stage is that it allows the same number of interleaving feedbacks as that of gain stages since the last interleaving feedbacks $M_{F4A|4B}$ can be from the opposite sides V_{g4-} and V_{g4+} respectively [6,7]. A single gain varying DC bias V_{PD} controls all gain varying transistors $M_{V1,2,3}$ across the CS amplifiers and lowers the gain at high input signal. This prevents non-linearity when the input signal strength increases which can cause signal distortion or clipping throughout the signal path. Thus, variable-gain increases the dynamic range of the TIA [5,7].

The gains at DC in the gain stage is listed in Table 2.

Figure 5. (a) Simplified and (b) transistor-level schematic of the proposed DVGITIA gain stage for both designs 1 and 2 together with the source follower buffer.

Table 2. Table of gain functions in DVGITIA gain stage.

Gain *	V_o/V_i	Transfer Function	Gain *	V_o/V_i	Transfer Function
$A_{G2,3,4,5}$	$V_{g2,3,4,5}/V_{g1,2,3,4}$	$-g_{M2,3,4,5}R_{G2,3,4,5}$	$A_{F2,3,4}$	$V_{g2,3,4}/V_{g3,4,4}^\#$	$-g_{MF2,3,4}R_{G2,3,4}$

* Care must be taken in defining the gains A; in this paper, the negative sign of CS amplifier gain is inside A. [#] Note that two of the feedbacks are from the same V_{g4+} and V_{g4-} nodes, just across to different stages.

The poles and zeros can be calculated for the gain stage, with $\omega_{G2,3,4,5}$ poles contributed by the gain transistors $M_{G2,3,4,5}$ and $\omega_{F2,3,4}$ poles and zeros contributed by feedbacks $M_{F2,3,4}$:

$$\omega_{G2,3,4,5} = \frac{1}{R_{G2,3,4,5}C_{o,G2,3,4,5}} \quad (8)$$

$$\omega_{F2,3,4} = \frac{1}{R_{G2,3,4}C_{o,G2,3,4}} \quad (9)$$

where $C_{o,G2,3,4,5}$ is the output parasitic capacitances at $V_{g2,3,4,5}$ at both positive and negative sides.

Voltage gain of the gain stage (with both sides being equal) is calculated as:

$$A_{gain} = \frac{A_{G2}A_{G3}A_{G4}A_{G5}\left(1+\frac{s}{\omega_{F2,3,4}}\right)\left(1+\frac{s}{\omega_{D5}}\right)}{\left(1+\frac{s}{\omega_{G2,3,4}}\right)\left(1+\frac{s}{\omega_{F2,3,4,5}}\right)\left(1+\frac{s}{\omega_{D5}}\right)-A_{G2}A_{G3}A_{F2}-A_{G3}A_{G4}A_{F3}+A_{G4}A_{F4}} \quad (10)$$

Hence, the differential gain equation of the entire circuit for DVGITIA designs 1 and 2 are:

$$Z_{T,DVGITIA1,diff} = (Z_{Tin1+} - Z_{Tin1-}) \times A_{gain} \quad (11)$$

$$Z_{T,DVGITIA2,diff} = (Z_{Tin2+} - Z_{Tin2-}) \times A_{gain} \quad (12)$$

After the DVGITIA gain stage, the buffer stage is a simple source-follower $M_{BA|BB}$ with the load being an NMOS current mirror current source $I_{BUF/2}$ of 2 mA on each side to match to 50 Ω .

3.3. Layout and Die Microphotograph

The TIA layout is shown in Figure 6 and it has two three-pin DC pads at the top and bottom and two ground-signal-signal-ground (GSSG) input/output pads on the left/right respectively. The V_{DD} is 1.8 V for both the core TIA and buffer while I_{BUF} is 4 mA. V_{PD} is the voltage biasing for gain variation and varies from 1 V to 1.8 V. The 250 fF C_{pd} load is included on-chip to show that the TIA designs can handle a real photodetector load. All schematic, layout and post-layout simulation results are done with the Cadence software design tool.

Figure 6. (a) TIA layout design with pads and (b) core area only of DVG TIA design 1 and (c) DVG TIA design 2 (both core area: $100\ \mu\text{m} \times 85\ \mu\text{m}$, total area with pads: $350\ \mu\text{m} \times 910\ \mu\text{m}$).

After the finalization of layouts of both DVG TIA designs, they are sent to Tower Semiconductor Ltd. (TowerJazz) foundry for manufacturing, with the die microphotographs of the actual taped-out chips shown in Figure 7.

Figure 7. (a) Die microphotographs of the overall DVG TIA design 1 and 2 layouts, (b) core circuit of DVG TIA design 1 and (c) core circuit of DVG TIA design 2.

3.4. Measurement Setup

The measurement setup is shown in Figure 8. The DC voltage and current biasing for the device under test (DUT) is provided by the Keysight B1500A Semiconductor Device Analyzer which is also able to measure current for V_{DD} power supply. S-parameter and IP1dB analysis is done by the Keysight PNA-X N5247A Network Analyzer.

Figure 8. Measurement setup for S-parameters and input referred 1 dB compression point.

The measured DC currents for V_{DDTIA} and V_{DDBUF} are shown in Table 3:

Table 3. Measured DC currents for voltage power supply.

	I_{DC} for V_{DDTIA} (mA)	Core Power (mW)	I_{DC} for V_{DDBUF} (mA)	Total Power (mW)
DVG TIA design 1	17.08	30.7	10.73	50.1
DVG TIA design 2	15.25	27.5	11.46	48.1

4. Results and Discussion

4.1. Frequency Response from S-parameters

Both simulation and measurement results are presented in this paper for comparison. Measurement data in S-parameters can be converted to differential Z-parameter transimpedance gain through Equation (13) to plot Figure 9.

$$Z_{T,diff} = Z_{41} - Z_{21} = \frac{2S_{41} \times \sqrt{Z_{p01}Z_{p04}}}{(1 - S_{11})(1 - S_{44}) - S_{14}S_{41}} - \frac{2S_{21} \times \sqrt{Z_{p01}Z_{p02}}}{(1 - S_{11})(1 - S_{22}) - S_{14}S_{21}} \Omega \quad (13)$$

where Z_{p01} , Z_{p02} , Z_{p04} are the impedances of ports 1, 2 and 4 in the measurement setup and are all 50Ω , while port 3 is unused. $Z_{T,diff}$ gain in Equation (13) can also be reported in dB Ω as in Figure 9.

Figure 9. (a) Post-layout simulation and measured frequency response of the DVG TIA design 1 and (b) DVG TIA design 2 with varying V_{PD} at 1 V, 1.4 V, 1.6 V and 1.8 V.

As shown in Figure 9, the measured frequency response of both DVG TIA designs 1 and 2 are flat and stable across most of the bandwidth from 10 MHz to 10 GHz. The measured gains for when $V_{PD} = 1$ V and 1.2 V are similar and some gain drop only occurs when it is increased to 1.4 V. Although gain peaking is within 1 dB Ω for simulation, however due to process variation for the tape-out chips,

gain peaking becomes within 2 dB Ω for DVGTIA design 1 (except for $V_{PD} = 1.4$ V) but above the limit for DVGTIA design 2. This could be corrected in a future design by having a variable peaking design that controls a zero to reduce the peaking due to process design kit (PDK) variation. The differences in frequency response between both designs are due to the different automatic feedbacks at V_{in} that cause different pole/zero pairs as mentioned in Section 3.1. In addition, the load of design 2 is slightly larger causing a slightly higher gain.

The maximum gain when $V_{PD} = 1$ V is 60.6 and 62.8 dB Ω for DVGTIA designs 1 and 2 respectively, which reduces to a minimum gain of 24.5 and 27.8 dB Ω respectively when $V_{pd} = 1.8$ V. Hence, the gain variations of DVGTIA designs 1 and 2 are 36.1 dB Ω and 35 dB Ω respectively. This gain variation helps to increase the TIA input dynamic range which will be explained in Section 4.2. The 3 dB bandwidth for DVGTIA design 1 is 6.42 GHz at $V_{PD} = 1$ V, except when $V_{PD} = 1.4$ V where the bandwidth is reduced to 5.03 GHz (3dB above gain at 85 MHz) before the large peaking, which can be ignored if $V_{pd} = 1.4$ V is not used. Bandwidths for the other V_{pd} biasings are larger than 6.42 GHz and thus there is no bandwidth loss during gain variation.

The simple source follower buffer $M_{BA|BB}$ and I_{BUF} , after the gain stage as shown in Figure 5b has a gain drop of 2.7 dB Ω found in post-layout simulation. Hence, when buffer loss is de-embedded, the maximum gains for the chip of DVGTIA designs 1 and 2 are 63.3 dB Ω and 65.5 dB Ω respectively.

The 3 dB bandwidth for DVGTIA design 2 is 5.22 GHz at $V_{pd} = 1$ V which is before the large peaking. If the peaking had been controlled, it could be higher at 7.36 GHz instead. The bandwidth is slightly reduced at $V_{pd} = 1.8$ V to 5.11 GHz which is the lowest among all V_{pd} biasings.

4.2. Input Referred 1dB Compression Point

The input 1 dB compression point (IP1dB) is the input power where the output 1 dB compression point (OP1dB) occurs, which is when the gain became compressed by 1 dB as compared to when the input power P_{in} is low. The IP1dB is a parameter to check the signal linearity of individual amplifiers and for the entire receiver module [16] and is plotted in Figure 10 for both DVGTIA designs.

Figure 10. (a) Post-layout simulation and measured IP1dB compression curve of the DVGTIA design 1 and (b) DVGTIA design 2 with V_{PD} at 1 V, 1.4 V, 1.6 V and 1.8 V.

The variable-gain DVGTIA designs in this paper increases the upper limit of the dynamic range which is determined by the IP1dB when the $V_{PD} = 1.8$ V and gain is tuned to be the lowest. As shown in Figure 10, P_{in} is swept from -30 dBm to 0 dBm. The input 1dB compression point when $V_{pd} = 1$ V is -27 dBm and -27.4 for DVGTIA designs 1 and 2 respectively, with the baseline $P_{in} = -30$ dBm used for comparison. The IP1dB increases when $V_{pd} = 1.8$ V to -7.5 dBm (0.178 mW) and -7 dBm (0.2 mW) for DVGTIA designs 1 and 2 respectively. This proves that IP1dB increases significantly as V_{PD} biasing is increased. The dynamic range for TIA is defined as the input current signal range that it is able to

amplify without significant signal distortion at output. Thus, the upper limit of the input dynamic range in terms of current can be calculated from P_{in} of the IP1dB by taking the power formula [17]:

$$P_{in} = I_{in}^2 Z_{in} \quad (14)$$

where Z_{in} is found to be 19.5Ω and 28.1Ω for DVGTTA designs 1 and 2 respectively, in post-layout simulation. Hence, the dynamic range upper limit is calculated to be 3 mA and 2.7 mA respectively.

4.3. Noise

The lower limit of the dynamic range is determined by the noise level, since the noise of the TIA would distort the input signal if it is too small. The allowable signal-to-noise ratio (SNR) for TIA designs with a maximum bit error rate (BER) of 10^{-12} is 16.9 dB (≈ 49) [18]. The simulated output-referred noise voltage (ORN) is shown in Figure 11.

Figure 11. (a) Post-layout simulation in Cadence of the output referred noise voltage at TIA bandwidth as well as noise contribution at V_{mid} (output of input stage) and V_{g5} (output of gain stage) of DVGTTA design 1 and (b) DVGTTA design 2 with V_{PD} at 1 V, 1.4 V, 1.6 V and 1.8 V.

Taking the ORNV in Figure 11 and the maximum gains at $V_{PD} = 1V$ in Figure 9, the input-referred noise current (IRNC) of DVGTTA designs 1 and 2 are calculated to be $10.3 \text{ pA}/\sqrt{\text{Hz}}$ and $21.7 \text{ pA}/\sqrt{\text{Hz}}$ at bandwidths 6.4 GHz and 5.2 GHz respectively. Hence by taking $\text{SNR} = 49$ and multiplying $\sqrt{\text{Hz}}$ at bandwidth operation, the minimum input current needed is calculated as $40.4 \mu\text{A}$ and $76.8 \mu\text{A}$ for the lower limit of the input dynamic range of DVGTTA designs 1 and 2 respectively.

Sensitivity, which is defined as the minimum input signal S_{min} required to produce an output signal greater than the required signal-to-noise ratio of both DVGTTA designs can also be calculated. The formula for sensitivity is [19]:

$$S_{min} = (S/N)_{min} \times k \times T_o \times BW \times NF \quad (15)$$

where $(S/N)_{min}$ is the signal-to-noise ratio, k is the Boltzmann constant, T_o is the absolute temperature (300 K), BW is the bandwidth and NF is the noise figure.

The simulated noise figures of DVGTTA designs 1 and 2 are found to be 11.4 dB and 33.9 dB at bandwidths 6.4 GHz and 5.2 GHz respectively. By using (15), the sensitivity is calculated to be -47.5 dBm and -25.6 dBm for DVGTTA designs 1 and 2. As shown in Figure 11, the largest contributor of noise is the gain stages of the DVGTTA designs. The larger noise of the DVGTTA designs is due to three reasons. Firstly, there is the on-chip C_{pd} , whereas other designs may have an off-chip or an ideal noiseless C_{pd} in simulation to run together after obtaining the measurement results. Secondly, the designs have multiple stages with the second stage as a source follower being a significant problem.

This is shown in Friis' formula, which can be used to calculate the contribution of each stage in an amplifier to find the total noise factor [20]:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_n - 1}{G_1 G_2 \dots G_{n-1}} \quad (16)$$

where F_n is the noise factor of the n^{th} stage and G_n is the gain of the n^{th} stage.

According to (16), each cascaded stage contributes noise divided by the gains of the previous stages. Since the gain of the source follower is lower than 1, it contributes to more overall noise F_{total} . Thirdly, the cascaded common-source amplifiers in the gain stage are not differential stages with a single current source for both sides that can cancel the common-mode noise but separate common-sources amplifiers on both sides. This would thus increase the gain but prevent noise cancellation.

4.4. Eye Diagram

The measured eye diagrams of the DVGITIA designs 1 and 2 are shown in Figure 12. The input signal is a pseudorandom binary sequence (PRBS) at 5 Gb/s with $V_{pp} = 1$ V. As seen in Figure 12, both eyes are open and clear, with eye heights of approximately 250 mV, eye widths of approximately 150 ps and jitter of less than 100 ps. This proves that the DVGITIA designs can function normally at the high data rate of 5 Gb/s even with an input signal of random sequence. The eye diagrams plotted are single-ended (A/+ side) during measurement using the R&S RTO 1044 oscilloscope.

Figure 12. (a) Measured eye diagrams with 5 Gb/s PRBS input signal of DVGITIA design 1 and (b) DVGITIA design 2.

4.5. Reliability

The reliability of the DVGITIA designs can also be tested. In simulation, the temperature and C_{pd} load can be varied to check if the TIA design still works as an amplifier and outputs a good frequency response. As shown in Figure 13a, DVGITIA design 1 still works well when the temperature is varied from -40 °C to 80 °C. In addition, when C_{pd} increased from 0.25 pF– 2 pF (800%), the bandwidth is reduced only from 6.39 GHz to 4.38 GHz (–31%). This shows that the design is able to withstand a large C_{pd} load as the low Z_{in} is able to shield the C_{pd} impact on the dominant pole. This is a big advantage for this design as a larger photodiode can be used to absorb more light to output a larger and more detectable current input for the TIA. However as shown in Figure 13b, DVGITIA design 2 encounters instability when temperature deviates too far from 27 °C and also when C_{pd} is increased.

Figure 13. (a) Reliability testing in post-layout simulation by increasing C_{pd} and varying temperature as well as differential gain across V_{mid} and V_{g5} for DVGITIA design 1 and (b) DVGITIA design 2.

5. Discussion

5.1. Comparison of Theory and Simulation/Measurement Results

The theoretical equations of the gains for the gain stage (10) of the DVGITIA designs can be calculated and compared with the simulation/measurement results to check if they are accurate. The calculation for DVGITIA design 1 is shown in Table 4, but it is similar for design 2 as well. For DVGITIA design 1, the measured differential $Z_{T,diff1}$ at V_{OUT} is 60.6 dBΩ as in Figure 9a. Using the simulated $Z_{T,diff,input}$ at V_{mid} and $Z_{T,diff,gain}$ at V_{g5} for the gain stage in Figure 13a and the buffer stage gain drop of 2.7 dBΩ, the gain due to the gain stage is calculated to be 16.5 dBΩ (6.7 times gain).

Table 4. Simulation gain calculations for DVGITIA design 1.

Gain	Equation	Sim Value	Gain	Equation	Sim Value
A_{G2}	$-g_{MG2}R_{G2}$	-3.51	A_{F2}	$-g_{MF2}R_{G2}$	-0.23
A_{G3}	$-g_{MG3}R_{G3}$	-2.61	A_{F3}	$-g_{MF3}R_{G3}$	-0.05
A_{G4}	$-g_{MG4}R_{G4}$	-3.20	A_{F4}	$-g_{MF4}R_{G4}$	-0.14
A_{G5}	$-g_{MG5}R_{G5}$	-1.77	Equation (10) gain		13.1 times

There is a source follower stage M_{G1} and R_{G1} that is not accounted for in (10) which has been assumed to have a gain approximately equal to 1, but its gain is closer to 0.5 in reality, as well as including other losses. Hence, half of the gain 13.1 times is 6.5 times which is close to the simulation/measurement results calculated above.

5.2. Figure of Merit

$$FOM_1 = \frac{\text{Gain } (\Omega) \times \text{Bandwidth (GHz)} \times C_{pd} \text{ (pF)}}{\text{Core Power (mW)}} \quad (17)$$

$$FOM_2 = \frac{\text{Gain } (\Omega) \times \text{Bandwidth (GHz)} \times C_{pd} \text{ (pF)} \times \text{Gain Range (dB}\Omega\text{)}}{\text{Core Power (mW)}} \quad (18)$$

Two different figure of merits (FOMs) formulas are shown in (17) and (18) to compare with other recent variable-gain TIA works. FOM_1 consists of four different parameters including the gain, bandwidth and C_{pd} load which are desired to be large as well as the core power which is desired to be small. All these parameters are key for determining the effectiveness of a TIA design. FOM_2 includes the gain range to include the advantage of having a wide gain-variation design.

As shown in Table 5 below, the DVGITIA designs have good FOM_2 values due to their large gain variation which is more than the other comparable designs.

Table 5. Table of comparison with other recent works.

Reference	Unit	[9] ^a	[21] ^b	[22]	[23]	[24]	This Work	
Technology	nm	180 CMOS	130 CMOS	130 BiCMOS	180 CMOS	65 CMOS	180 BiCMOS	
V_{DD}	V	1.8	3	3.3	1.8	1.2	1.8	
C_{pd}	pF	0.9	2	0.02	0.25	0.45	0.25	
Maximum gain	dB Ω	66	78	65.1	69.3	76	60.6 ^c	62.8 ^c
gain	Ω	1995	7943	1793	2917	6310	1072	1380
Minimum gain	dB Ω	48	48	56.7	55.8	60	24.5	27.8
gain	Ω	251	251	684	617	1000	16.8	24.5
Gain range	dB Ω	18	30	8.4	13.5	16	36.1	35
Bandwidth	GHz	1.5	0.64	6.8	1	0.3	6.42	5.22
Core power	mW	27	114	21.2	6	6	30.7	27.5
Core area	mm ²	N.A.	0.283	0.0078	0.0075	0.015	0.0085	
Input-referred noise current	pA/ $\sqrt{\text{Hz}}$	6 ^d	5.6	4.34 ^d	9.33	2 ^d	10.3 ^d	21.7 ^d
FOM_1	Equationn (17)	100	89	12	122	142	56	65
FOM_2	Equationn (18)	1796	2676	97	1641	2272	2022	2293

^a This paper presents simulation results while others present measurement results; ^b core area is not known and it has high power consumption; ^c if gain drop of 2.7 dB Ω of buffer is de-embedded, gains would be 63.3 dB Ω and 65.5 dB Ω respectively; ^d simulation results presented for the input-referred noise current.

Although designs in [21] and [24] also have high FOM_2 , they both only operate on a narrow bandwidth less than 1 GHz, in addition with [24] being a much smaller and more advanced process. The gain-bandwidth trade-off for this paper's designs is acceptable for TIAs that function above 5 GHz. Although both have a slightly higher power consumption and noise due to the large number of CS stages in the gain stage, this allows the largest gain variation to be tuned among all designs and thus resulting in a wide input current dynamic range suitable for the range of current output from a real photodetector [7,10].

6. Conclusions

In conclusion, the authors presented two different inductorless differential variable gain transimpedance amplifier (DVG-TIA) designs with a voltage-controlled variable-gain using Tower Jazz Semiconductor's 0.18- μm SiGe BiCMOS process, while also being compatible with a pure-CMOS process. The designs are unique since they take a single-ended input to become a differential output while maintaining the low input impedance of a RGC configuration, as well as having a small additional automatic negative feedback to lower input impedance even further to compensate the large photodetector capacitive load, which is proven for DVG-TIA design 1 in the reliability analysis. The gain stage is also able to provide a good gain while maintaining the bandwidth throughout due to its interleaving feedbacks and capacitive degeneration techniques.

The measurement results after chip tape-out is presented, with gain ranges of 24.5–60.6 dB Ω and 27.8–62.8 dB Ω and bandwidths of 6.42 GHz and 5.22 GHz for DVG-TIA designs 1 and 2 respectively while having an on-chip capacitive load of 250 fF modelling a real photodetector. If buffer gain drop of 2.7 dB Ω is de-embedded, the maximum gains would be 63.3 dB Ω and 65.5 dB Ω respectively. By varying the biasing voltage, very wide gain ranges of 36.1 dB Ω and 35 dB Ω with no drop in the bandwidths achieved. This translates into giving wide input current dynamic ranges of 40.4 μA to 3 mA and 76.8 μA to 2.7 mA which fits the real photodetector's current output.

Both DVG-TIA designs also have an input referred noise current of 10.3 pA/ $\sqrt{\text{Hz}}$ and 21.7 pA/ $\sqrt{\text{Hz}}$ (simulation), core DC power consumption of 30.7 mW and 27.5 mW and compact core area of 100 μm $\times$ 85 μm . They both have the best figure of merit as defined in this paper with five key TIA parameters for designs above 5 GHz operation.

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