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Single DC Source Multilevel Inverter with Changeable Gains and Levels for Low-Power Loads

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Abstract: Different types of multilevel converters have been used to convert DC voltage to AC voltage for different applications. It is, however, desirable for flexible AC output voltage to be created from a single DC source at lower cost. This paper presents a new type of single DC source multilevel inverter which has the ability to create a different number of levels with low rate components. This device is also able boost the magnitude of the output voltage by means of a variable gain with one DC source. The advantages of the multilevel inverter are rapid stepping among levels, and its ability to produce different ranges of levels (seven, nine and eleven) and gains (two, four and eight). The proposed multilevel inverter includes six semiconductor switches, eight diodes, two capacitors and two inductors, making it suitable for low-power applications. A simulation in MATLAB and experimental tests on a prototype setup showed good performance for different modulations, with THD% down to 2.29%, which are meets the IEEE standard (IEEE 519).

Keywords: boost inverter; multilevel inverter; power electronics; single source; low components

1. Introduction

Multilevel inverters (MLIs) have been used in various applications as voltage source converters (VSC) to connect DC power systems to AC power systems. MLIs include an array of semiconductors and DC sources to generate different output voltage levels with high quality waveforms. Low harmonic contents, high resolution on the output voltage and scalability make this kind of inverter more suitable in comparison with traditional two-level inverters for energy conversion applications such as photovoltaic systems [1], HVDC [2,3], wind turbines [4], active power filters [5], drives systems [6,7], electrical vehicles [8] and power grids [9]. Multilevel inverters are classified into three well-known topologies that have been used in various industries: Neutral Point Clamped (NPC) [10], Flying Capacitor (FC) [11] and Cascade H-bridge (CHB) [12]. CHB topologies are gaining attention due to certain aspects, such as simpler control strategy, scalability, the number of levels, the number of semiconductors, etc. However, classical topologies require a large number of components to increase the number of output voltage levels. Circuit complexity, complicated voltage control strategies and higher manufacturing costs are expected when the number of components increases. Nevertheless, creating more voltage levels with fewer components and DC sources is an important objective for newer multilevel inverter topologies [13–16]. In [17], a structural review and comparative study of all categories of Multilevel Inverters are presented.

In [18], a series connection of modules consisting of one DC source and two switches was introduced. The output voltage is generated by the sum of each module's output voltage. The module can only generate zero and positive voltage levels. An H-bridge was added at the end of the series module in [19] to create both negative and positive levels. Also, the module has a simple circuit and control strategy, and the stress on the switches is low compared with conventional CHBs. On the other hand, a large number of cascade connections to generate higher output voltage levels can increase the complexity and construction cost. A similar structure with an H-bridge at the end of the module was introduced in [20]. It is used a diode instead of a switch by [21], as the number of switches decreased in this way. The number of required electronic switches and DC sources are a key factor in designing MLIs, because the circuit size, cost, installation area and control complexity depend on them. Compared with other modules, the device described in [22] can generate more voltage levels with fewer switches. However, the cost of using several DC sources still remains high. Another type of MLI using crossing switches to oppose the polarity of DC links was introduced in [23,24] to generate more levels. The authors of [25,26] introduced modules with few semiconductors in order to achieve maximum levels from four DC sources. Recently, different storage elements such as capacitors have been mixed with DC sources to provide a sinusoidal voltage source in various multilevel inverter structures and increase the output voltage levels with the same number of DC sources. The authors of [27,28] redesigned the configuration of [11,23], replacing some DC sources with capacitors and increasing the number of voltage levels. Some configurations with mixed DC sources and capacitors were proposed in [29,30]. A new topology with only one DC source is presented in [31]. The authors of [32] redesigned the configuration of [31], removing some switches and replacing them with diodes. In some modules that use a single source to generate output levels, the number of semiconductors increased, and the charging/discharging of capacitors and switch driving become complicated [31,33]. Also, the authors of [34] replaced half of the DC sources used in [25,26] with capacitors, and rearranged the semiconductor configuration to present a new multilevel inverter with fewer DC sources.

In this paper, a flexible multilevel inverter for one DC source is proposed which can create a different number of levels and voltages at the output for low-power applications. The main core of the proposed module is a new type of DC–DC converter to change the levels very quickly by a variable duty cycle, in order to create a staircase waveform. The main converter should be rapid with a tiny transient time, and have the ability to create all voltage levels; otherwise, it can produce high harmonics and destroy the staircase waveform. The other part of the proposed inverter is a full-bridge converter (H-bridge) to evenly produce the positive and negative half-cycles of a sinusoidal waveform. The proposed multilevel inverter has the ability to create up to 11 levels and boost the output voltage up to 8 times compared to the DC source. The proposed multilevel inverter is illustrated in Section 2. The modular configuration, switching patterns, equations, and a comparative study with conventional inverters are included in this section. In Section 3, the calculations for the switching pattern and duty cycle for a different number of levels and different gains are presented. Finally, the simulation and experimental results are presented for nine different cases (number of levels = 7, 9 and 11 versus gain = 2, 4 and 8) in Sections 4 and 5.

2. The Proposed Multilevel Inverter

Figure 1 shows the proposed multilevel inverter, which is divided into two parts: the main converter and the full-bridge converter. The main converter provides the levels, and the full-bridge converter changes the polarity of output. The main converter is very fast and comprises a high gain DC–DC converter with good dynamic reactivity to changes in the duty cycle. Each level of output can be achieved in the specified amount of the duty cycle. On the other hand, the duty cycle must be set to a certain number, which is calculated in lookup tables (Tables 1–9). Nevertheless, the duty cycle was changed in one cycle continuously to create different levels in the multilevel inverter. Then, the full-bridge converter changes the polarity for each half-cycle from the positive or negative half-cycles. Figure 2 illustrates this issue with an example for eleven levels on the output.

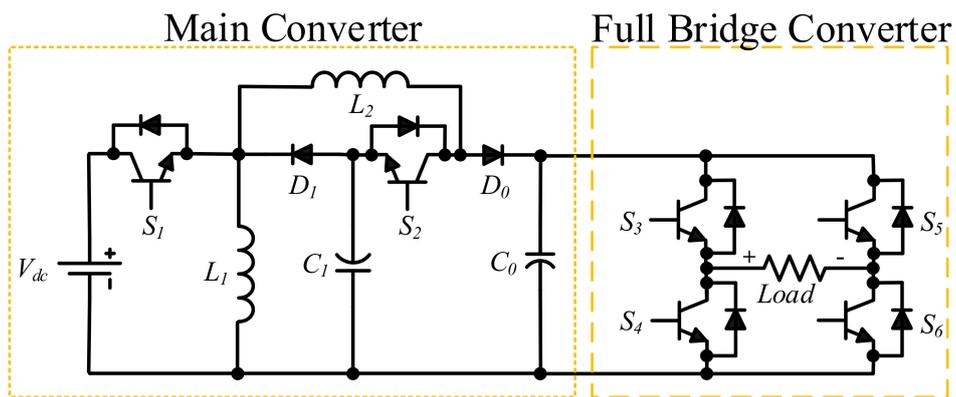


Figure 1. The proposed single source multilevel inverter.

Table 1. Switching table level = 11, gain = 8.

Voltage Level	Duty Cycle S_1 (%)	Duty Cycle S_2 (%)	S_3	S_4	S_5	S_6	
Positive Level	$8 V_{DC}$	74	74	1	0	0	1
	$6.66 V_{DC}$	72	72	1	0	0	1
	$5.66 V_{DC}$	69	69	1	0	0	1
	$4 V_{DC}$	66	66	1	0	0	1
	$1.66 V_{DC}$	56	56	1	0	0	1
Zero Level	0	0	0	1	0	1	0
	0	0	0	0	1	0	1
Negative Level	$-1.66 V_{DC}$	56	56	0	1	1	0
	$-4 V_{DC}$	66	66	0	1	1	0
	$-5.66 V_{DC}$	69	69	0	1	1	0
	$-6.66 V_{DC}$	72	72	0	1	1	0
	$-8 V_{DC}$	74	74	0	1	1	0
Num. of turning on per 1-cycle	20,000	20,000	1	1	2	2	

Table 2. Switching table level = 11, gain = 4.

Voltage Level	Duty Cycle S_1 (%)	Duty Cycle S_2 (%)	S_3	S_4	S_5	S_6	
Positive Level	$4 V_{DC}$	66	66	1	0	0	1
	$3.33 V_{DC}$	64	64	1	0	0	1
	$2.83 V_{DC}$	62	62	1	0	0	1
	$2 V_{DC}$	58	58	1	0	0	1
	$0.84 V_{DC}$	47	47	1	0	0	1
Zero Level	0	0	0	1	0	1	0
	0	0	0	0	1	0	1
Negative Level	$-0.84 V_{DC}$	47	47	0	1	1	0
	$-2 V_{DC}$	58	58	0	1	1	0
	$-2.83 V_{DC}$	63	63	0	1	1	0
	$-3.33 V_{DC}$	72	72	0	1	1	0
	$-4 V_{DC}$	66	66	0	1	1	0
Num. of turning on per 1-cycle	20,000	20,000	1	1	2	2	

Table 3. Switching table level = 11, gain = 2.

Voltage Level	Duty Cycle S ₁ (%)	Duty Cycle S ₂ (%)	S ₃	S ₄	S ₅	S ₆	
Positive Level	2 V _{DC}	58	58	1	0	0	1
	1.66 V _{DC}	56	56	1	0	0	1
	1.41 V _{DC}	54	54	1	0	0	1
	1 V _{DC}	50	50	1	0	0	1
	0.42 V _{DC}	39	39	1	0	0	1
Zero Level	0	0	0	1	0	1	0
	0	0	0	0	1	0	1
Negative Level	-0.42 V _{DC}	39	39	0	1	1	0
	-1 V _{DC}	50	50	0	1	1	0
	-1.41 V _{DC}	54	54	0	1	1	0
	-1.66 V _{DC}	56	56	0	1	1	0
	-2 V _{DC}	58	58	0	1	1	0
Num. of turning on per 1-cycle		20,000	20,000	1	1	2	2

Table 4. Switching table level = 9, gain = 8.

Voltage Level	Duty Cycle S ₁ (%)	Duty Cycle S ₂ (%)	S ₃	S ₄	S ₅	S ₆	
Positive Level	8 V _{DC}	74	74	1	0	0	1
	5.83 V _{DC}	70	70	1	0	0	1
	3.33 V _{DC}	64	64	1	0	0	1
	1.66 V _{DC}	56	56	1	0	0	1
Zero Level	0	0	0	1	0	1	0
	0	0	0	0	1	0	1
Negative Level	-1.66 V _{DC}	56	56	0	1	1	0
	-3.33 V _{DC}	64	64	0	1	1	0
	-5.83 V _{DC}	70	70	0	1	1	0
	-8 V _{DC}	74	74	0	1	1	0
Num. of turning on per 1-cycle		20,000	20,000	1	1	2	2

Table 5. Switching table level = 9, gain = 4.

Voltage Level	Duty Cycle S ₁ (%)	Duty Cycle S ₂ (%)	S ₃	S ₄	S ₅	S ₆	
Positive Level	4 V _{DC}	66	66	1	0	0	1
	2.91 V _{DC}	63	63	1	0	0	1
	1.66 V _{DC}	56	56	1	0	0	1
	0.84 V _{DC}	47	47	1	0	0	1
Zero Level	0	0	0	1	0	1	0
	0	0	0	0	1	0	1
Negative Level	-0.84 V _{DC}	47	47	0	1	1	0
	-1.66 V _{DC}	56	56	0	1	1	0
	-2.91 V _{DC}	63	63	0	1	1	0
	-4 V _{DC}	66	66	0	1	1	0
Num. of turning on per 1-cycle		20,000	20,000	1	1	2	2

Table 6. Switching table level = 9, gain = 2.

Voltage Level	Duty Cycle S_1 (%)	Duty Cycle S_2 (%)	S_3	S_4	S_5	S_6	
Positive Level	$2 V_{DC}$	58	58	1	0	0	1
	$1.45 V_{DC}$	55	55	1	0	0	1
	$0.84 V_{DC}$	47	47	1	0	0	1
	$0.42 V_{DC}$	39	39	1	0	0	1
Zero Level	0	0	0	1	0	1	0
	0	0	0	0	1	0	1
Negative Level	$-0.42 V_{DC}$	39	39	0	1	1	0
	$-0.84 V_{DC}$	47	47	0	1	1	0
	$-1.45 V_{DC}$	55	55	0	1	1	0
	$-2 V_{DC}$	58	58	0	1	1	0
Num. of turning on per 1-cycle		20,000	20,000	1	1	2	2

Table 7. Switching table level = 7, gain = 8.

Voltage Level	Duty Cycle S_1 (%)	Duty Cycle S_2 (%)	S_3	S_4	S_5	S_6	
Positive Level	$8 V_{DC}$	74	74	1	0	0	1
	$5.41 V_{DC}$	69	69	1	0	0	1
	$2.5 V_{DC}$	61	61	1	0	0	1
Zero Level	0	0	0	1	0	1	0
	0	0	0	0	1	0	1
Negative Level	$-2.5 V_{DC}$	61	61	0	1	1	0
	$-5.41 V_{DC}$	69	69	0	1	1	0
	$-8 V_{DC}$	74	74	0	1	1	0
Num. of turning on per 1-cycle		20,000	20,000	1	1	2	2

Table 8. Switching table level = 7, gain = 4.

Voltage Level	Duty Cycle S_1 (%)	Duty Cycle S_2 (%)	S_3	S_4	S_5	S_6	
Positive Level	$4 V_{DC}$	66	66	1	0	0	1
	$2.70 V_{DC}$	62	62	1	0	0	1
	$1.25 V_{DC}$	52	52	1	0	0	1
Zero Level	0	0	0	1	0	1	0
	0	0	0	0	1	0	1
Negative Level	$-1.25 V_{DC}$	52	52	0	1	1	0
	$-2.70 V_{DC}$	62	62	0	1	1	0
	$-4 V_{DC}$	66	66	0	1	1	0
Num. of turning on per 1-cycle		20,000	20,000	1	1	2	2

Table 9. Switching table level = 7, gain = 2.

Voltage Level	Duty Cycle S_1 (%)	Duty Cycle S_2 (%)	S_3	S_4	S_5	S_6	
Positive Level	$2 V_{DC}$	58	58	1	0	0	1
	$1.35 V_{DC}$	53	53	1	0	0	1
	$0.62 V_{DC}$	44	44	1	0	0	1
Zero Level	0	0	0	1	0	1	0
	0	0	0	0	1	0	1
Negative Level	$-0.62 V_{DC}$	44	44	0	1	1	0
	$-1.35 V_{DC}$	53	53	0	1	1	0
	$-2 V_{DC}$	58	58	0	1	1	0
Num. of turning on per 1-cycle		20,000	20,000	1	1	2	2

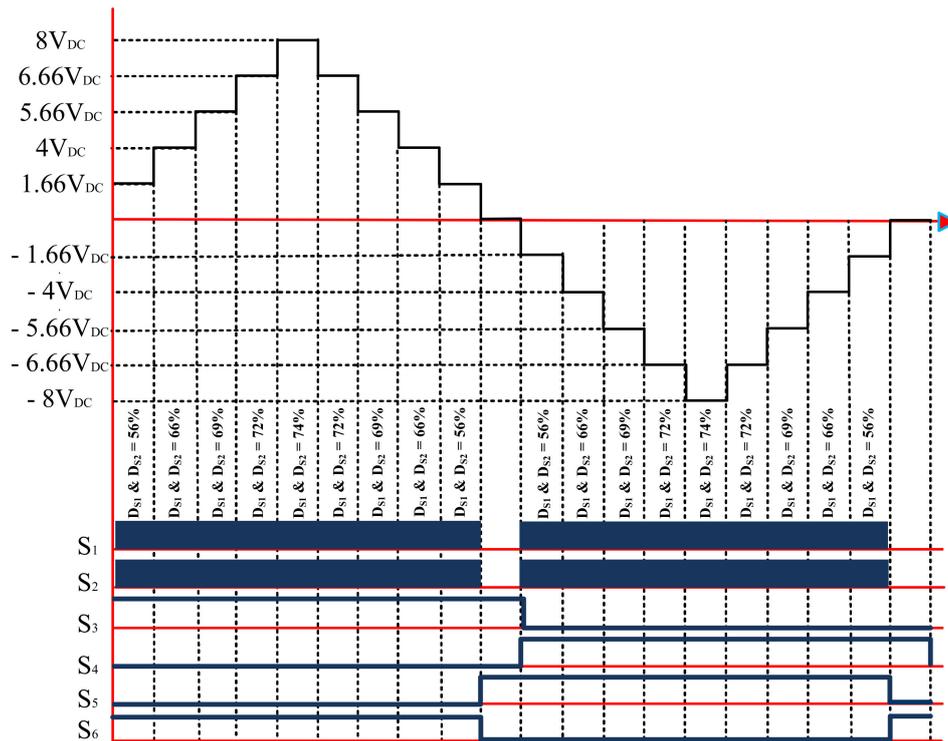


Figure 2. Switching pattern and duty cycle of switches in one-cycle for the proposed multilevel inverter (ex: the number of levels = 11 and gain = 8).

The duty cycle of each level for S1 and S2 are calculated (according to Section 3) and shown in Figure 2. The states for S3, S4, S5, and S6 to create the polarity of the output are also shown.

In order to demonstrate the detail and performance, Figure 3 depicts the two modes (on/off) for the main converter part. It is noticeable that S1 and S2 switch on and off, simultaneously.

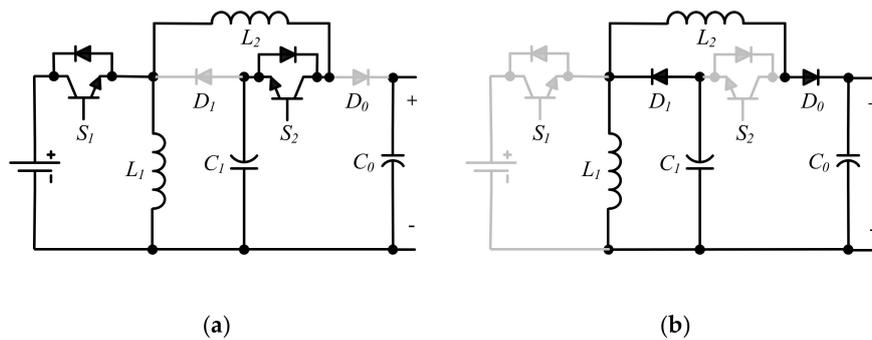


Figure 3. The mode of the main converter: (a) on mode; (b) off mode.

On mode: S1 and S2 are in an on state, and D0 and D1 are in reverse bias (Figure 3a). On the other hand, switches S1 and S2 conduct the current to magnetize L1 and L2, respectively. And C0 and C1 are discharged to the output. Then:

$$V_{L1} = V_{in} \tag{1}$$

$$V_{L2} = V_{in} + V_{C1} \tag{2}$$

Off mode: S1 and S2 are turned off, and D0 and D1 are conducting in forward bias (Figure 3b). L1 and L2 demagnetize to charge C0 and C1, respectively, and supply output. Thus:

$$V_{L1} = -V_{C1} \tag{3}$$

$$V_{L2} = -(V_{C1} + V_0) \tag{4}$$

Figure 4 demonstrates the behavior of the components in the two modes.

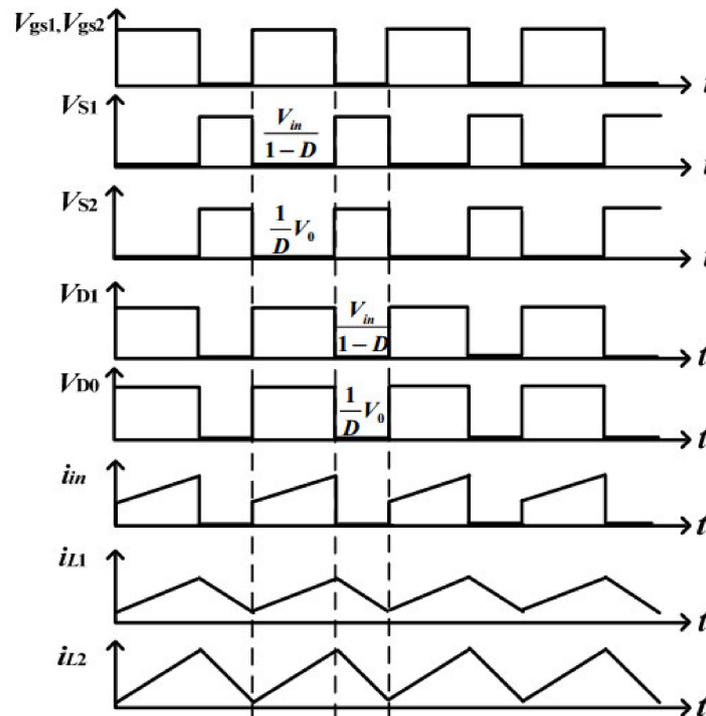


Figure 4. The behaviors of the components for two modes.

From (1) and (3) and balancing in L1:

$$DV_{in} + (1 - D)(-DV_{C1}) = V_{L1} = 0 \tag{5}$$

Then

$$V_{C1} = \frac{D}{1 - D} V_{in} \tag{6}$$

Also, from (2) and (4),

$$D(V_{in} + V_{C1}) + (1 - D)(-(V_{C1} + V_0)) = V_{L2} = 0 \tag{7}$$

Consequently,

$$\frac{V_0}{V_{in}} = \left(\frac{D}{1 - D} \right)^2 \tag{8}$$

Equation (8) provides the formula to calculate the duty cycle which creates the levels. The duty cycles for each level and each gain according to (8) will be presented in Section 3.

A comparative study between the proposed multilevel inverter and some other configurations in cases of producing 11 levels of output voltage is shown in Figure 5. In order to make a suitable comparison, various aspects, such as the number of switches, the number of diodes, the number of DC sources and TSV, were considered.

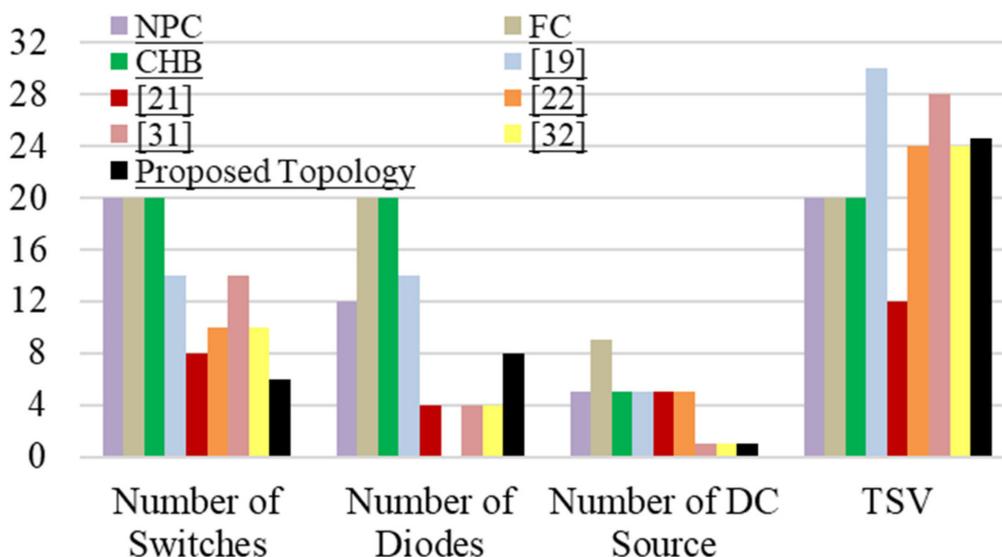


Figure 5. Comparative studies: The number of switches, number of diodes, number of sources and TSV, in terms of the number of levels.

According to Figure 5, the proposed module can get maximum levels with fewer DC sources. As a comparison only in the case of the number of DC sources, [31,32] require the same number of DC sources, but the number of switches should be considered. One of the major advantages of the proposed module is that it uses fewer switches. On the other hand, the module can be considered as being in the group with a low number of diodes. The complexity of the module is reduced by using diodes instead of switches. Since the module is intended for use in low-power applications, the range of TSV is reasonable, as can be seen in Figure 5.

3. Calculation of the Switching Pattern and Duty Cycle

The proposed multilevel inverter is divided into two parts, as mentioned above: the DC–DC converter and the full-bridge. In the DC–DC converter, the number of levels can be achieved by controlling the duty cycles. Thus, the duty cycle should be changed continuously to create each level and a staircase waveform in one cycle of a sinusoidal waveform. In the full-bridge, the switching modes should be set to alternatively change the polarity of the half-cycle. The duty cycle and switching pattern are calculated for levels 7, 9 and 11 and gains 2, 4 and 8. Tables 1–9 illustrate the calculation of the switching pattern and duty cycle according to Equation (8). S3 and S6 are for positive levels and S4 and S5 are for negative levels, which have a low frequency (up to 100 Hz); S1 and S2 are used to set a duty cycle with 20 kHz.

The nearest level control method (NLC) was also considered as a switching technique for level timing, as presented in [35]. This technique is a very simple means by which to reduce the number of calculations in the processor. The modulation scheme and the control diagram are shown in Figure 6. According to Figure 6a, the controller gets a sample from the reference voltage (V_{ref}) and then rounds it to the nearest voltage level (V_{aN}). Each voltage level has a switching table according to the information in Tables 1–9 to change switch modes and duty cycles (Figure 6b). The sampling is repetitive for each sample time (T_s).

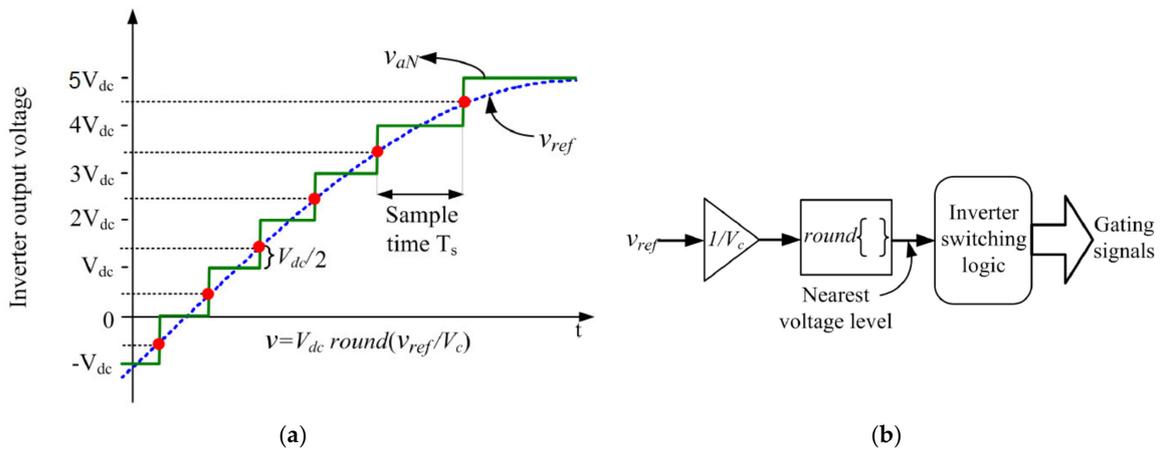


Figure 6. Nearest level control: (a) Waveform synthesis; (b) Control diagram.

4. Simulation Results

A simulation was carried out to evaluate the proposed multilevel inverter at different outputs. The specifications of the simulation are shown in Table 10. The aim of the simulation test was to produce a sinusoidal waveform of 50 Hz from one DC source at 36 volts.

Table 10. Simulation configuration.

Switches		IGBT	
Diodes		Diode	
Inductors	$L_1 = 50 \mu\text{H}$		$L_2 = 250 \mu\text{H}$
Capacitors	$C_0 = 2 \mu\text{F}$		$C_1 = 1 \mu\text{F}$
DC Source		36 V	
Load		500 Ω	

Nine output conditions were considered for the waveforms. The output levels were set for seven, nine and eleven, along with three different gains (output voltage amount/input voltage amount), i.e., two, four and eight. Figure 7 summarizes the nine simulation setups. The simulation results showed the ability of the proposed circuit to create different waveforms with sinusoidal output voltages.

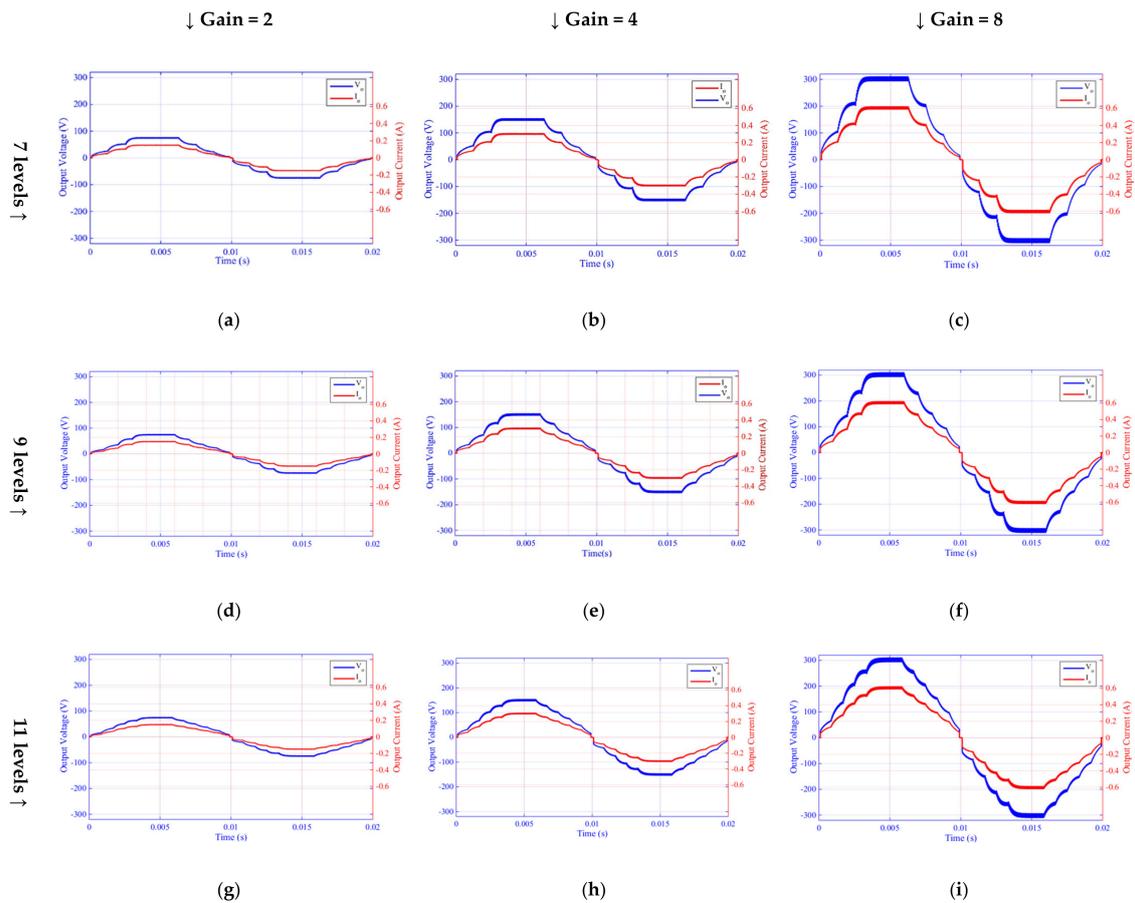


Figure 7. Simulation waveform of output voltages and currents for the proposed multilevel inverter: (a) levels = 7, gain = 2; (b) levels = 7, gain = 4; (c) levels = 7, gain = 8; (d) levels = 9, gain = 2; (e) levels = 9, gain = 4; (f) levels = 9, gain = 8; (g) levels = 11, gain = 2; (h) levels = 11, gain = 4; (i) levels = 11, gain = 8.

5. Experimental Results

A prototype setup was implemented in the laboratory to verify the performance of the proposed single source multilevel inverter with flexible levels and gains. Figure 8 provides a picture of the experimental setup in the laboratory. The specifications of the prototype setup are given in Table 11. An experimental test was also carried out on nine cases (the number of levels for 7, 9 and 11 versus gains for 2, 4 and 8) to generate a sinusoidal waveform of 50 Hz from one DC source at 12 volts.

Table 11. Specifications of the prototype setup configuration.

Switches	IGBT FGH60N60SFD (S_1, S_2) (S_3, S_4, S_5, S_6) IGBT IKW40N120H3	
Diodes	RHRP15120	
Inductors	$L_1 = 50 \mu\text{H}$	$L_2 = 250 \mu\text{H}$
Capacitors	$C_0 = 2 \mu\text{F}$	$C_1 = 1 \mu\text{F}$
DC Source	12 V	
Optocoupler	HCPL3120	
Microcontroller	ATmega32A	
Buffer	7404	
Load	500 Ω	

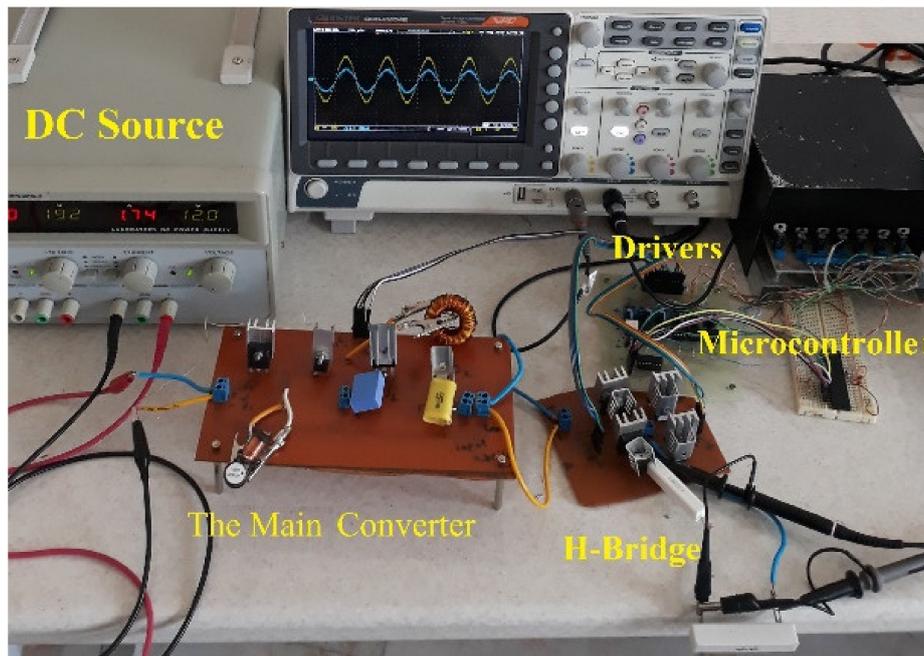


Figure 8. Experimental setup in the laboratory.

Figure 9 shows the voltages and currents of the proposed inverter with nine different outputs. It should be mentioned that the THD% of all the waveforms meets the IEEE standard (IEEE 519), in that they are under 8%. The THD% is shown in Table 12. The worst THD% was 6.82% and the best was 2.08%.

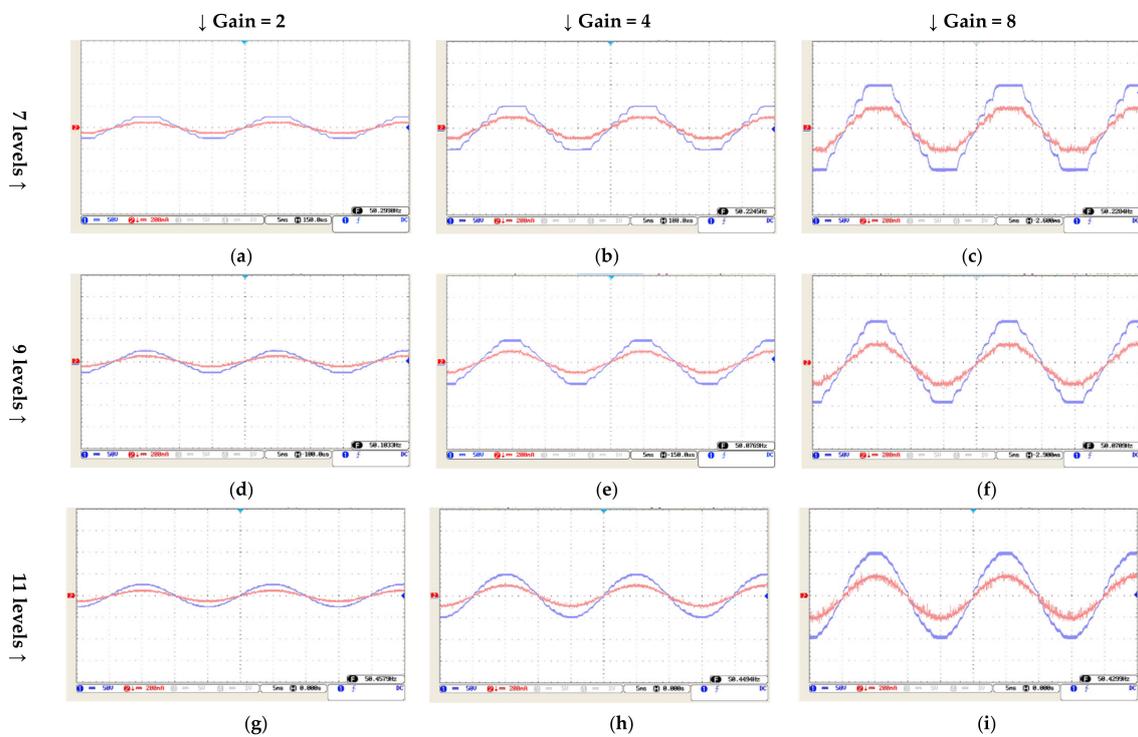


Figure 9. The experimental test waveform of output voltages and currents for the proposed multilevel inverter: (a) levels = 7, gain = 2; (b) levels = 7, gain = 4; (c) levels = 7, gain = 8; (d) levels = 9, gain = 2; (e) levels = 9, gain = 4; (f) levels = 9, gain = 8; (g) levels = 11, gain = 2; (h) levels = 11, gain = 4; (i) levels = 11, gain = 8.

Table 12. THD% of voltages for nine outputs.

7Levels, Gain 2	6.61
7Levels, Gain 4	6.70
7Levels, Gain 8	6.82
9Levels, Gain 2	4.88
9Levels, Gain 4	4.77
9Levels, Gain 8	5.27
11Levels, Gain 2	2.08
11Levels, Gain 4	2.28
11Levels, Gain 8	2.29

The proposed multilevel inverter (with few components and one DC source) is economical, with good output voltage for low-power applications. It can create different voltage levels for different voltages with just one DC source. Also, a low number of harmonics make it especially promising.

Figure 10 illustrates the voltages and currents of the switches and diodes in the proposed inverter.

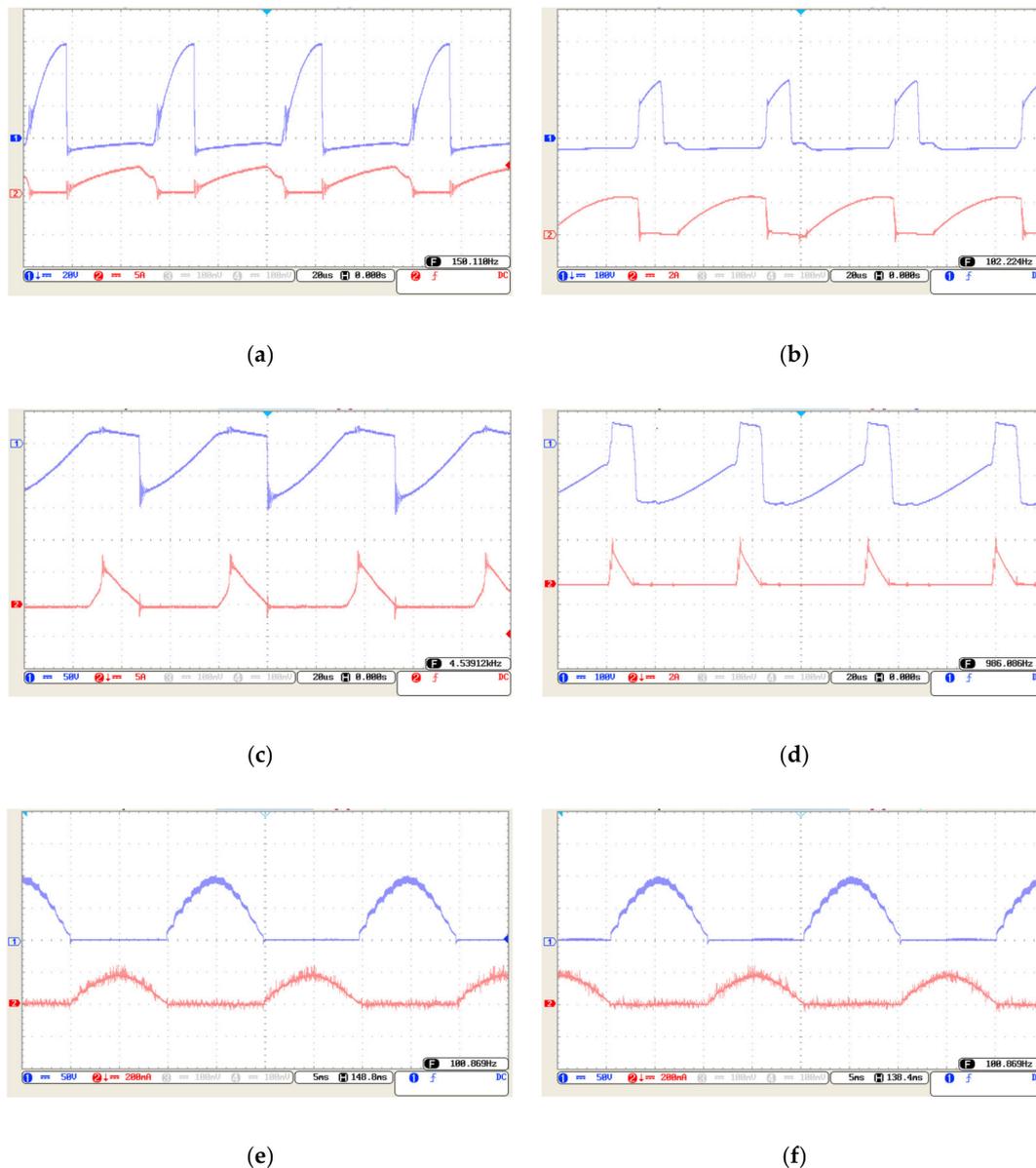
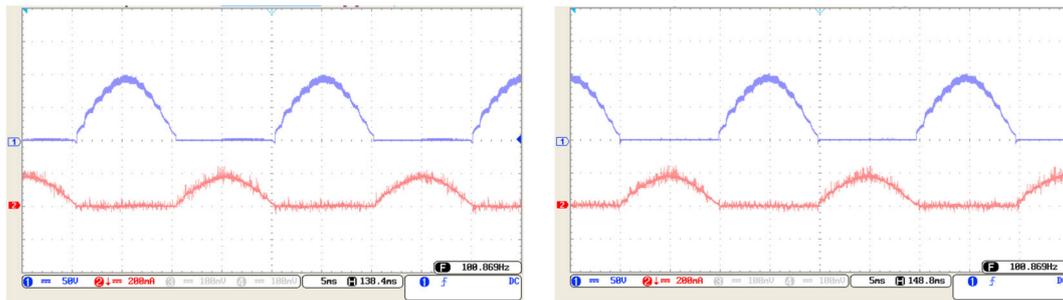


Figure 10. Cont.

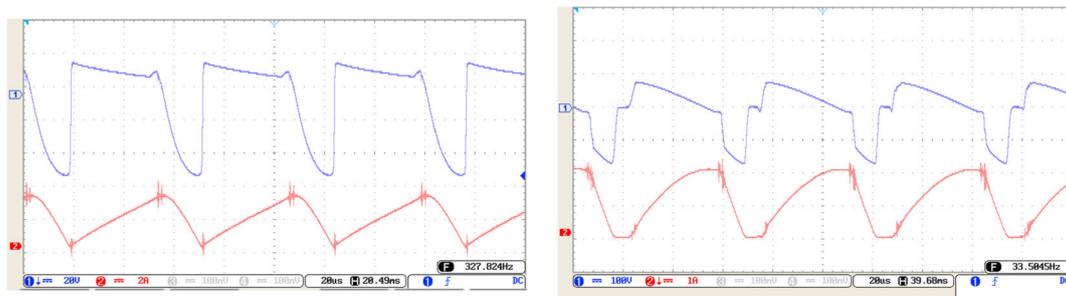


(g)

(h)

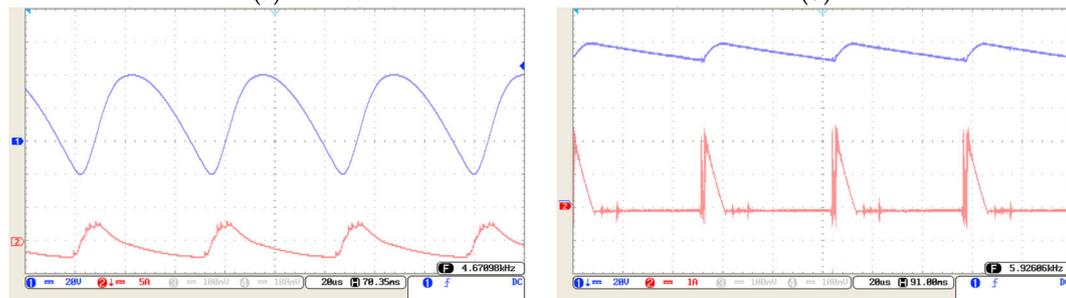
Figure 10. Experimental test waveform of output voltages and currents for the proposed multilevel inverter: (a) the voltage and current of S1; (b) the voltage and current of S2; (c) the voltage and current of D1; (d) the voltage and current of D0; (e) the voltage and current of S3; (f) the voltage and current of S4; (g) the voltage and current of S5; (h) the voltage and current of S6.

Finally, the voltage and current of the capacitors and inductors are depicted in Figure 11.



(a)

(b)



(c)

(d)

Figure 11. Experimental test waveform of output voltages and currents for the proposed multilevel inverter: (a) the voltage and current of L1; (b) the voltage and current of L2; (c) the voltage and current of C1; (d) the voltage and current of C0.

6. Conclusions

A new kind of multilevel inverter for low-power applications, operating from one DC source, was introduced in this paper. The proposed inverter has the ability to produce different levels of output, i.e., up to 11 levels, and to increase the output voltage by up to eight times compared to the input voltage. It also has flexible levels and gains. The circuit of the proposed inverter comprises six semiconductor switches, eight diodes, two capacitors and two inductors, i.e., a low number of components for a multilevel inverter. These components are organized into two parts: the main converter and the full-bridge converter. The main converter is involved in fast DC–DC conversion, with a tiny transient time to create levels and gains by changing the duty cycle according to different

strategies. Meanwhile, the full-bridge changes the polarities for the positive and negative half-cycles. Verification of the proposed inverter was carried out in a simulation and in experimental tests using nine different modulations. The device was shown to produce three level modes for 7, 9 and 11, and three gain modes for 2, 4 and 8. The simulation and experimental results showed a high level of performance for all the test cases; the THD% was shown to be between 2.08% and 6.82% (in the permitted range of the IEEE 519 standard). The illustrated features of the proposed inverter make it suitable for single DC sources in low-power applications.

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References

- Essakiappan, S.; Krishnamoorthy, H.S.; Enjeti, P.; Balog, R.; Ahmed, S. Multilevel Medium-Frequency Link Inverter for Utility Scale Photovoltaic Integration. *IEEE Trans. Power Electron.* **2015**, *30*, 3674–3684. [[CrossRef](#)]
- Nami, A.; Liang, J.; Dijkhuizen, F.; Demetriades, G.D. Modular Multilevel Converters for HVDC Applications: Review on Converter Cells and Functionalities. *IEEE Trans. Power Electron.* **2014**, *30*, 18–36. [[CrossRef](#)]
- Gowaid, I.A.; Adam, G.; Massoud, A.; Ahmed, S.; Williams, B.W. Hybrid and Modular Multilevel Converter Designs for Isolated HVDC–DC Converters. *IEEE J. Emerg. Sel. Top. Power Electron.* **2017**, *6*, 188–202. [[CrossRef](#)]
- Yuan, X. A Set of Multilevel Modular Medium-Voltage High Power Converters for 10-MW Wind Turbines. *IEEE Trans. Sustain. Energy* **2014**, *5*, 524–534. [[CrossRef](#)]
- Ahmadi, D.; Wang, J. Online Selective Harmonic Compensation and Power Generation with Distributed Energy Resources. *IEEE Trans. Power Electron.* **2013**, *29*, 3738–3747. [[CrossRef](#)]
- Mathew, J.; Rajeevan, P.P.; Mathew, K.; Azeez, N.A.; Gopakumar, K. A Multilevel Inverter Scheme with Dodecagonal Voltage Space Vectors Based on Flying Capacitor Topology for Induction Motor Drives. *IEEE Trans. Power Electron.* **2012**, *28*, 516–525. [[CrossRef](#)]
- Nair, V.; Pramanick, S.; Gopakumar, K.; Franquelo, L.G. Novel Symmetric Six-Phase Induction Motor Drive Using Stacked Multilevel Inverters with a Single DC Link and Neutral Point Voltage Balancing. *IEEE Trans. Ind. Electron.* **2017**, *64*, 2663–2670. [[CrossRef](#)]
- Zheng, Z.; Wang, K.; Xu, L.; Li, Y. A Hybrid Cascaded Multilevel Converter for Battery Energy Management Applied in Electric Vehicles. *IEEE Trans. Power Electron.* **2013**, *29*, 3537–3546. [[CrossRef](#)]
- Haw, L.K.; Dahidah, M.S.A.; Almurib, H. A New Reactive Current Reference Algorithm for the STATCOM System Based on Cascaded Multilevel Inverters. *IEEE Trans. Power Electron.* **2015**, *30*, 3577–3588. [[CrossRef](#)]
- Nabae, A.; Takahashi, I.; Akagi, H. A New Neutral-Point-Clamped PWM Inverter. *IEEE Trans. Ind. Appl.* **1981**, *17*, 518–523. [[CrossRef](#)]
- Meynard, T.A.; Foch, H. Multi-Level Choppers for High Voltage Applications. *EPE J.* **1992**, *2*, 45–50. [[CrossRef](#)]
- Peng, F.Z.; Lai, J.-S.; McKeever, J.; VanCoeveering, J. A multilevel voltage-source inverter with separate DC sources for static VAR generation. *IEEE Trans. Ind. Appl.* **1996**, *32*, 1130–1138. [[CrossRef](#)]
- Zare, F. *Power Electronics Education Electronic-Book*; School of Engineering Systems, Queensland University of Technology: Brisbane, SEQ, Australia, 2008.
- Gupta, K.K.; Ranjan, A.; Bhatnagar, P.; Sahu, L.K.; Jain, S.; Ranjan, A. Multilevel Inverter Topologies with Reduced Device Count: A Review. *IEEE Trans. Power Electron.* **2015**, *31*, 1. [[CrossRef](#)]
- Debnath, S.; Qin, J.; Bahrani, B.; Saeedifard, M.; Barbosa, P. Operation, Control, and Applications of the Modular Multilevel Converter: A Review. *IEEE Trans. Power Electron.* **2015**, *30*, 37–53. [[CrossRef](#)]
- Venkataramanaiah, J.; Suresh, Y.; Panda, A.K. A review on symmetric, asymmetric, hybrid and single DC sources based multilevel inverter topologies. *Renew. Sustain. Energy Rev.* **2017**, *76*, 788–812. [[CrossRef](#)]
- Vijeh, M.; Rezanejad, M.; Samadaei, E.; Bertilsson, K. A General Review of Multilevel Inverters Based on Main Submodules: Structural Point of View. *IEEE Trans. Power Electron.* **2019**, *34*, 9479–9502. [[CrossRef](#)]

18. Babaei, E.; Hosseini, S.H. New cascaded multilevel inverter topology with minimum number of switches. *Energy Convers. Manag.* **2009**, *50*, 2761–2767. [[CrossRef](#)]
19. Babaei, E.; Farhadi-Kangarlu, M.; Sabahi, M. Extended multilevel converters: An attempt to reduce the number of independent DC voltage sources in cascaded multilevel converters. *IET Power Electron.* **2014**, *7*, 157–166. [[CrossRef](#)]
20. Najafi, E.; Yatim, A.H. Design and Implementation of a New Multilevel Inverter Topology. *IEEE Trans. Ind. Electron.* **2011**, *59*, 4148–4154. [[CrossRef](#)]
21. Alishah, R.S.; Nazarpour, D.; Sabahi, M.; Hosseini, S.H. New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels. *IET Power Electron.* **2014**, *7*, 96–104. [[CrossRef](#)]
22. Malathy, S.; Ramaprabha, R. A new single phase multilevel inverter topology with reduced number of switches. In Proceedings of the 2016 3rd International Conference on Electrical Energy Systems (ICEES), Chennai, India, 17–19 March 2016; pp. 139–144.
23. Gupta, K.; Jain, S. Topology for multilevel inverters to attain maximum number of levels from given DC sources. *IET Power Electron.* **2012**, *5*, 435–446. [[CrossRef](#)]
24. Farhadi-Kangarlu, M.; Babaei, E. Cross-switched multilevel inverter: An innovative topology. *IET Power Electron.* **2013**, *6*, 642–651. [[CrossRef](#)]
25. Samadaei, E.; Gholamian, S.A.; Sheikholeslami, A.; Adabi, J. An Envelope Type (E-Type) Module: Asymmetric Multilevel Inverters with Reduced Components. *IEEE Trans. Ind. Electron.* **2016**, *63*, 7148–7156. [[CrossRef](#)]
26. Samadaei, E.; Sheikholeslami, A.; Gholamian, S.A.; Adabi, J. A Square T-Type (ST-Type) Module for Asymmetrical Multilevel Inverters. *IEEE Trans. Power Electron.* **2018**, *33*, 987–996. [[CrossRef](#)]
27. Metri, J.I.; Vahedi, H.; Kanaan, H.Y.; Al-Haddad, K. Real-Time Implementation of Model-Predictive Control on Seven-Level Packed U-Cell Inverter. *IEEE Trans. Ind. Electron.* **2016**, *63*, 4180–4186. [[CrossRef](#)]
28. Vahedi, H.; Al-Haddad, K. Real-Time Implementation of a Seven-Level Packed U-Cell Inverter with a Low-Switching-Frequency Voltage Regulator. *IEEE Trans. Power Electron.* **2015**, *31*, 5967–5973. [[CrossRef](#)]
29. Zamiri, E.; Vosoughi, N.; Hosseini, S.H.; Barzegarkhoo, R.; Sabahi, M. A New Cascaded Switched-Capacitor Multilevel Inverter Based on Improved Series-Parallel Conversion with Less Number of Components. *IEEE Trans. Ind. Electron.* **2016**, *63*, 3582–3594. [[CrossRef](#)]
30. Liu, J.; Wu, J.; Zeng, J.; Guo, H. A Novel Nine-Level Inverter Employing One Voltage Source and Reduced Components as High-Frequency AC Power Source. *IEEE Trans. Power Electron.* **2017**, *32*, 2939–2947. [[CrossRef](#)]
31. Taghvaie, A.; Adabi, J.; Rezanejad, M. Circuit Topology and Operation of a Step-Up Multilevel Inverter with a Single DC Source. *IEEE Trans. Ind. Electron.* **2016**, *63*, 6643–6652. [[CrossRef](#)]
32. Tang, Y.; Ran, L.; Alatise, O.; Mawby, P. Capacitor Selection for Modular Multilevel Converter. *IEEE Trans. Ind. Appl.* **2016**, *52*, 3279–3293. [[CrossRef](#)]
33. Sun, X.; Wang, B.; Zhou, Y.; Wang, W.; Du, H.; Lu, Z. A Single DC Source Cascaded Seven-Level Inverter Integrating Switched-Capacitor Techniques. *IEEE Trans. Ind. Electron.* **2016**, *63*, 7184–7194. [[CrossRef](#)]
34. Samadaei, E.; Kaviani, M.; Bertilsson, K. A 13-Levels Module (K-Type) with Two DC Sources for Multilevel Inverters. *IEEE Trans. Ind. Electron.* **2018**, *66*, 5186–5196. [[CrossRef](#)]
35. Meshram, P.; Borghate, V.B. A Simplified Nearest Level Control (NLC) Voltage Balancing Method for Modular Multilevel Converter (MMC). *IEEE Trans. Power Electron.* **2014**, *30*, 450–462. [[CrossRef](#)]

