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# A 12-Bit 2.4 GS/s Four-Channel Pipelined ADC with a Novel On-Chip Timing Mismatch Calibration

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Received: 11 April 2020; Accepted: 26 May 2020; Published: 29 May 2020



**Abstract:** This paper presents a 12-bit 2.4 GS/s analog-to-digital converter (ADC) employing four time-interleaved (TI) pipelined channels with a novel on-chip timing mismatch calibration in 40 nm CMOS process. TI architecture can increase the effective sampling rate of ADC but the dynamic performance of TI-ADC system is seriously degraded by offset, gain, and timing mismatches among the channels. Timing mismatch is the most challenging barrier among these mismatches due to the difficulty and complexity of its detection and correction. An automatic wideband timing mismatch detection without complex calculations. By adopting the proposed mismatch-free variable delay line (VDL), the full-scale traversal timing mismatch correction accomplishes an accurate result without missing codes. Measurement results show that the spurious free dynamic range (SFDR) of the prototype ADC is improved from 55.2 dB to 72.8 dB after calibration at 2.4 GS/s with a 141 MHz input signal. It can achieve an SFDR above 60 dB across the entire first Nyquist band based on the timing mismatch calibration and retiming technology. The prototype ADC chip occupies an area of 3 mm × 3 mm and it consumes 420 mW from a 1.8 V supply.

**Keywords:** analog-to-digital converter; time-interleaved; timing mismatch calibration; automatic wideband detection; variable delay line

# 1. Introduction

Driven by the rapid development of the information society, the need for systems such as high-speed digital oscilloscopes, optical communications, future mobile communication systems, and direct sampling receivers is growing fast. As the core device, analog to digital converter (ADC) plays an important role in such modern signal processing systems [1–5]. Moreover, the throughput rate of such signal processing systems is often limited by the speed of ADC. This can be understood by noticing that the operation rate of the digital signal processing circuits has been continuously increased with the development of the deep submicrometer technology, while the sampling rate of the ADC is not well scaling with the feature size of the transistors. Therefore, the design of high speed ADC has become the bottleneck of the systems [6,7]. In order to overcome the speed limitation of the single-channel ADC while taking both accuracy and power into account, time-interleaved (TI) architecture was proposed and becomes popular and attractive [8,9]. The TI-ADC increases the effective conversion rate by performing parallel data conversion using M sub-ADCs. Each sub-ADC operates at the same frequency  $f_c$  with a different phase, and the effective conversion rate of the TI-ADC can be



improved to  $f_c \times M$  [10]. Meanwhile, each sub-ADC is granted a longer conversion cycle that can keep the ADC in the linear power-speed region, which makes the ADC power consumption acceptable [11].

Ideally, the performance of TI-ADC is the same as one of sub-ADC in each channel. However, there are some mismatches such as offset mismatch, gain mismatch, and timing mismatch among channels due to the practical implementation constraints during fabrication. All of these mismatches not only degrade the signal-to-noise-and-distortion ratio (SNDR), but also affect the spurious free dynamic range (SFDR) seriously [12–20]. The amplitude of spurs from offset mismatch is independent of the input signal in both amplitude and frequency. The amplitude of spurs introduced by gain mismatch only varies with input amplitude. But the timing mismatch makes the amplitude of spurs vary largely with both amplitude and frequency of input signal [4]. Thus, the timing mismatch is the more significant error source for high-speed TI-ADCs with high frequency input signal. In order to correct these errors, digital calibration is necessary to be implemented. Compared to offset mismatch and gain mismatch that can be detected by simple mean result, timing mismatch is more difficult to be calibrated and is the focus of this work [6,21].

Typically, the timing mismatch calibration is composed of detection and correction [11,22]. The main techniques for detection are classified as two categories, namely, foreground and background [7]. For the foreground calibration, the timing mismatch can be detected from the ADC output, where a specific input signal is required, which means this method needs to interrupt the ADC's normal operation during calibration [18]. Compared to foreground calibration, background calibration is preferred as it doesn't need the specified input signal and can operate in real time without interrupting the ADC conversion process [7,17]. Additionally, it can also track possible drifts in timing mismatch due to temperature or voltage variations. A difference-based digital background timing mismatch detection algorithm for different types of input signals is proposed in [11], but the detection frequency of the input signal is limited to a half of the sampling frequency which greatly limits its application range. An algorithm of estimating the timing mismatch through extra reference channels that do not participate in conversion is proposed in [23–25], but it cannot avoid to increase the complexity and consume more area and power. Meanwhile, additional distortions will be introduced by the extra reference channel clock especially in high-speed designs.

There are two main options in timing mismatch correction. One is performed in the digital domain, i.e., inserting long high-speed finite impulse response (FIR) filter in the output data path to remove the timing mismatch [20,26–28], but such a filter brings a heavy burden of power consumption and complexity. The other is adjusting the sampling clock delay path in analog domain. Typically, variable delay line (VDL) is employed in order to narrow the timing mismatch, but it might worsen random jitter due to additional buffers and capacitors of VDL as the noise source in the clock path [24,29]. The jitter of the clock increases the fluctuation of the final calibration value and affects the final calibration result. At the same time, the clock jitter also degrades the overall performance of ADC. Compared with using high-speed FIR filters, ADC that is calibrated under this method does not suffer from the high power and large area consumption, and the additional jitter is acceptable relative to the original clock jitter and the overall performance requirements of the system. Therefore, the VDL is employed to narrow the timing mismatch in the proposed timing mismatch calibration.

The paper presents a 12-bit 2.4 GS/s four-channel TI pipelined ADC with a wideband and accurate timing mismatch calibration on chip. As a key step in realizing calibration of TI-ADC timing mismatch, the traditional timing mismatch detection typically only works in a specific frequency range. The proposed timing mismatch calibration achieves an automatic wideband timing mismatch detection (AWD) that can operate in any Nyquist bands (NBs) through adaptively adjusting the calibration polarity, which greatly expands its application range. Compared with using high-speed FIR filters that have large cost of power and area to correct timing mismatch, the proposed full-scale traversal timing mismatch correction (FSTC) avoids the problem of missing codes due to process mismatch and it achieves an accurate correction without large capacitors. With the proposed timing mismatch

calibration, the SFDR of the prototype ADC is improved from 55.2 dB to 72.8 dB at 2.4 GS/s with a 141 MHz input signal.

This paper is organized, as follows. Section 2 describes the proposed timing mismatch calibration algorithm in detail. Section 3 introduces the concrete implement of the 2.4 GS/s 12-bit pipelined ADC, with the experimental results in Sections 4 and 5 concludes this work.

## 2. Proposed Timing Mismatch Calibration Method

Figure 1 illustrates the overall timing mismatch calibration block diagram in a M-channel TI-ADC. Assume that the sub-ADC sampling frequency is  $f_s$ , and the sampling interval of the sub-ADC is  $t_s = 1/f_s$ . Then the total sampling frequency is  $F_s = f_s \times M$  and the overall sampling time is  $T_s = t_s/M$ . The ideal sampling time of sub-ADC<sub>1</sub>~sub-ADC<sub>M</sub> is  $t_1 + kM \sim t_M + kM$ . Here, channel 1 is taken as the timing adjustment reference channel and its corresponding timing mismatch  $\tau_1$  does not need to be adjusted. Digital outputs from sub-ADCs are imported into AWD in channel m ( $2 \le m \le M$ ) to extract timing mismatch information and feedback a digital control word  $d_m(n)$  to FSTC. The FSTC, which is composed of redundancy traversal module (RTM) and mismatch-free variable delay line (MF-VDL), realizes the accurate adjustment of sampling clock CLK<sub>m</sub> according to  $d_m(n)$ .



**Figure 1.** Architecture proposed to compensate the timing mismatch in M-channel analog to digital converters (ADCs).

The analog input signal x(t) is assumed to have the following characteristics:

(1) x(t) is a wide-sense stationary signal, so it satisfies

$$\mathbf{E}\{\mathbf{x}(\mathbf{t})\} = \mathbf{A},\tag{1}$$

$$R_{x}(|t_{1} - t_{2}|) = E\{x(t_{1})x(t_{2})\},$$
(2)

where  $E\{\bullet\}$  represents the mean value and A is a constant. The autocorrelation function  $R_x(|t_1 - t_2|)$  in Equation (2) only depends on  $t_1 - t_2$ .

(2) x(t) is a band-limited signal whose upper and lower frequencies  $f_H$ ,  $f_L$  satisfy:

$$(k-1) * F_s/2 < f_L \le f_H < k * F_s/2,$$
(3)

where k is a positive whole number.

#### 2.1. Automatic Wideband Timing Mismatch Detection

Figure 2 shows the overall block diagram of AWD. It mainly consists of two modules: estimation that is based on difference and correlation (EBDC), and the automatic determination of convergence direction (ADCD). First, digital output data of each sub-ADC enters the EBDC module to extract related information of timing mismatch among channels. Compared with the difference-based timing detection algorithm proposed in [11], the EBDC extract related information of timing mismatch among channels. So the timing mismatch detection of all channels can be performed at the same time without waiting for the completion of intermediate channel calibration before calibrating other channels, which compresses the calibration time. At the same time, the averaging operations on large amounts of points in the proposed EBDC can greatly reduce the calibration requirement for clock jitter. The specific implementation of EBDC is also shown in Figure 2.



Figure 2. Overall block diagram of automatic wideband timing-mismatch detection.

If assuming  $O_m = 0$  and  $G_m = G$ , the digital sequences from channel m - 1, m, m + 1 ( $2 \le m \le M - 1$ ) are

$$y_{m-1}(k) = x[(M * k + m - 1) * T_s + \tau_{m-1}] * G,$$
(4)

$$\mathbf{y}_{\mathbf{m}}(\mathbf{k}) = \mathbf{x}[(\mathbf{M} \ast \mathbf{k} + \mathbf{m}) \ast \mathbf{T}_{\mathbf{s}} + \tau_{\mathbf{m}}] \ast \mathbf{G},\tag{5}$$

$$y_{m+1}(k) = x[(M * k + m + 1) * T_s + \tau_{m+1}] * G,$$
(6)

where  $\tau$  is the additional sampling phase of each channel. The timing mismatch error function of channel m (2 ≤ m ≤ M – 1) can be written, as following:

$$\mathbf{e}_{m} = \mathbf{E}[|\mathbf{y}_{m+1}(\mathbf{k}) - \mathbf{y}_{m}(\mathbf{k})| - |\mathbf{y}_{m}(\mathbf{k}) - \mathbf{y}_{m-1}(\mathbf{k})|]. \tag{7}$$

The relationship between  $e_m$  and  $\tau_m$  is difficult to be proved directly. But if the absolute value operation  $|y_{m+1}(k) - y_m(k)|$  and  $|y_m(k)-y_{m-1}(k)|$  are approximated by the squaring function  $[y_{m+1}(k) - y_m(k)]^2$  and  $[y_m (k) - y_{m-1}(k)]^2$ , some conclusions can be derived [11]. Therefore, this approximation is carried out for the convenience and intuitiveness of derivation and  $e_m$  can be simplified to:

$$e_m \approx E[2 * y_{m+1}(k)y_m(k)] - E[2 * y_m(k)y_{m-1}(k)]. \tag{8}$$

Substituting the Equations (4)–(6) into the Equation (8), we have

$$e_m \approx 2G^2 * [R_x(T_s + \tau_m - \tau_{m-1}) - R_x(T_s + \tau_{m+1} - \tau_m)].$$
(9)

Because the timing mismatch is a pretty small amount relative to  $T_s$ , Equation (9) can be simplified to:

$$\mathbf{e}_{m} \approx 2\mathbf{G}^{2} * [\mathbf{R}'_{x}(\mathbf{T}_{s}) * (2\tau_{m} - \tau_{m+1} - \tau_{m-1})], \tag{10}$$

where  $R_{x}'(\bullet)$  is the derivative function of  $R_{x}(\bullet)$ .

For channel M, its timing mismatch error e<sub>M</sub> is

$$\begin{array}{rl} e_M & = E[|y_1(k+1) - y_M(k)| \ - \ |y_M(k) - y_{M-1}(k)|] \\ & \approx 2G^2 * \left[ R_x'(T_s) * (2\tau_M - \tau_1 - \tau_{M-1}) \right] \end{array} \prime$$

so e<sub>m</sub> can be expressed as:

$$\mathbf{e}_{m} = 2\mathbf{G}^{2} * [\mathbf{R}'_{x}(\mathrm{Ts}) * (2\tau_{m} - \tau_{(m+1)modM} - \tau_{m-1})], \tag{11}$$

where  $2 \le i \le M$  [7]. This indicates the  $e_m$  is approximately equal to 0 when there is no timing mismatch. The derivative of autocorrelation  $R_x(t)$  can be expressed as

$$\begin{aligned} R'_{x}(t) &= \int_{-\infty}^{+\infty} j2\pi f * S_{x}(f) e^{j2\pi f t} df \\ &= 2\pi * \int_{-\infty}^{+\infty} f[j\cos(2\pi f t) - \sin(2\pi f t)] * S_{x}(f) df \\ &= 2\pi * \int_{-\infty}^{-\infty} [f * j * \cos(2\pi f t) * S_{x}(f) - f * \sin(2\pi f t) * S_{x}(f)] df \end{aligned}$$
(12)

where  $S_x(f)$  denotes the signal spectrum [11] and it is an even function concerning f. So we have

$$R'_{x}(t) = -4\pi * \int_{0}^{+\infty} f \sin(2\pi f t) * S_{x}(f) df.$$
(13)

According to the mean value theorem of integrals,  $R_{x}'(t)$  can be expressed as

$$R'_{x}(t) = -4\pi\xi\sin(2\pi\xi t)\int_{0}^{+\infty} S_{x}(f)df, \xi \in (0, +\infty).$$
(14)

The following discussion is based on the frequency range classification of the input signal x(t):

(a) The frequency of x(t) is in the odd NBs.

The upper and lower frequencies  $f_H$ ,  $f_L$  of x(t) satisfy:

$$(k-1) * F_s/2 < f_L \le f_H < k * F_s/2,$$
(15)

where k is odd. The derivative function of  $R_x(t)$  at  $t = T_s$  can be written as

$$R'_{x}(T_{s}) = -4\pi\xi \sin(2\pi\xi T_{s}) \int_{f_{L}}^{f_{H}} S_{x}(f) df, \xi \in (f_{L}, f_{H})$$

$$(16)$$

where the item  $-4\pi\xi \sin(2\pi\xi T_s)$  is a negative value according to Equation (15). Meanwhile, the integral of  $S_x(f)$  is positive because the power spectral density  $S_x(f)$  is a real valued function. Therefore,  $R_x'(T_s)$ 

< 0. It indicates that the sign of  $2\tau_m - \tau_{(m+1)modM} - \tau_{m-1}$  is opposite to the sign of  $e_m$  if there is a timing mismatch among them, which can be described as

$$(2\tau_{\rm m} - \tau_{({\rm m}+1){\rm mod}{\rm M}} - \tau_{{\rm m}-1}) \propto -e_{\rm m}.$$
 (17)

(b) The frequency of x(t) is in the even NBs.

Now, the upper and lower frequencies  $f_H$ ,  $f_L$  of x(t) satisfy:

$$(k-1) * F_s/2 < f_L \le f_H < k * F_s/2,$$
(18)

where k is even. The analysis process is similar to the case (a). In this case,  $R_x'(Ts) > 0$ . Now,  $2\tau_m - \tau_{(m+1)modM} - \tau_{m-1}$  has the same sign as  $e_m$  if there is a timing mismatch among them:

$$(2\tau_{\rm m} - \tau_{\rm (m+1)modM} - \tau_{\rm m-1}) \propto e_{\rm m}.$$
 (19)

Combining the above two cases, the sign of  $2\tau_m - \tau_{(m+1)modM} - \tau_{m-1}$  can be detected from  $e_m$  as Equation (20)

$$(2\tau_{\rm m} - \tau_{\rm (m+1)modM} - \tau_{\rm m-1}) \propto (-1)^{\kappa} e_{\rm m}.$$
(20)

When  $2\tau_m - \tau_{(m+1)modM} - \tau_{m-1}$  is 0, average of  $e_m$  is also 0.

As the conclusion mentioned above, timing mismatch error function  $e_m$  has the monotonic property of timing mismatch  $\tau_m$  in one NB, but the polarity of the monotonicity is different from different NBs. If this timing mismatch calibration loop converges in odd (even) NBs, it needs to adjust the convergence direction to achieve right calibration in even (odd) NBs. Hence, keeping  $e_m$  the same monotonicity with timing mismatch  $\tau_m$  in different NBs is the key to expand the frequency range of calibration. Based on the EBDC conclusions, the algorithm for automatic determination of convergence direction (ADCD) is proposed. If the input signal bandwidth is limited to one NB, but in which NB is uncertain, this algorithm can determine the timing mismatch convergence direction automatically. The basic idea of ADCD scheme is as follows.

The timing mismatch detection is divided into coarse phase and fine phase by ADCD operation mode. First, timing mismatch detection begins with the coarse phase to determine the calibration updating direction. In coarse phase, the direction judgment is achieved by performing timing mismatch calibration through only one selected channel, and the sampling time of the other channels remain unchanged. This contributes to avoid the temporary drift of adjacent channels' sampling time, otherwise it may cause an error of direction judgment. First, converge direction code CD is preset to -1 as the initial state. In the first calibration cycle (each calibration cycle contains 4096 samples),  $d_m[1]$  is calculated by Equation (21)

$$d_{m}[1] = -C_{D} * e_{m}[1] * \mu, \qquad (21)$$

where  $\mu$  is the convergence step factor. Then MF-VDL of channel m is changed to adjust the sampling time according the RTM output. In the second calibration cycle,  $e_m[2]$  can be calculated through EBDC. The converge direction code  $C_D$  can be determined through following discussion of  $e_m[1]$  and  $e_m[2]$ .

A.  $e_m[1] > e_m[2] > 0 \& e_m[1] < e_m[2] < 0$ 

It indicates that relative to  $e_m[1]$ ,  $e_m[2]$  is approaching 0, which proves the time mismatch of channel m is getting smaller. So  $C_D = -1$  is correct.

B.  $e_m[2] > e_m[1] > 0 \& e_m[2] < e_m[1] < 0$ 

This situation shows that  $e_m[2]$  is far from 0 relative to  $e_m[1]$ , which proves that convergence direction is wrong. Therefore, value of  $C_D$  must be toggled to 1 to correct the direction of convergence.

C.  $e_m[1] > 0 > e_m[2] \& e_m[2] > 0 > e_m[1]$ 

This situation is similar to case A, but the convergence step is too big that  $d_m[1]$  exceeds the suitable value. So keep  $C_D$  as -1.

Combining the above discussion, the following summary Table 1 can be obtained:

case	e <sub>m</sub> [1]* e	$e_m[1]^* e_m[2] < 0$		
	$ e_m[2]  <  e_m[1] $	$ e_m[2]  >  e_m[1] $	/	
CD	-1	+1	-1	

**Table 1.** Value of  $C_D$  in different conditions of  $e_m[1]$  and  $e_m[2]$ .

After determining the value of  $C_D$  in coarse phase, ADCD enters the fine phase. If the preset for  $C_D$  is correct in coarse phase, then  $e_m$  is multiplied by a positive constant  $\mu$  and the products are added with an accumulator to generate the digital control word  $d_m(n)$ , as in Equation (22),

$$d_{m}[n+1] = d_{m}[n] - C_{D} * e_{m} * \mu.$$
(22)

Figure 3a shows the simulation of calibration convergence when the preset for  $C_D$  is correct in coarse phase. If the preset for  $C_D$  is incorrect in coarse phase, the detection will be reset and  $C_D$  is adjusted to 1. The following calibration cycles are similar to the above correct situation, as shown in Figure 3b.  $\tau_m$  is adjusted towards ( $\tau_{(m+1)modM} + \tau_{m-1}$ )/2 and the timing mismatch is minimized when  $e_m$  converges to zero. When all the  $e_m$  converge to 0, they are corrected to the reference skew  $\tau_1$  as well. As one factor that contributes to convergence step,  $e_m$  is directly proportional to timing mismatch, so this algorithm guarantees fast convergence. The accuracy of detection can be also guaranteed by the dynamic adjustment of factor  $\mu$ .



**Figure 3.** Simulation of calibration convergence (**a**) when the preset for  $C_D$  is correct in coarse phase and (**b**) when the preset for  $C_D$  is incorrect in coarse phase.

Thus, the proposed timing mismatch detection scheme is able to adjust the convergence direction adaptively and detect the timing mismatch fast and accurately in not only first NB, but also other NBs.

### 2.2. Full-Scale Traversal Timing Mismatch Correction

Compared with using high-speed FIR filters, ADC using VDL to narrow the timing mismatches among channels do not suffer from the high power and large area consumption. The capacitor DAC is typically employed to realize the adjustment of delay in the traditional VDL, but it will suffer from mismatch due to process inconsistencies. This matter makes the bit-weight of the DAC deviate from their nominal values, which particularly reveals in the appearance of the non-monotony and missing codes in DAC conversion characteristic, as shown in Figure 4 (normalize the minimum transition value of DAC output to 1 LSB).



Figure 4. The conversion characteristic of non-ideal 9bit DAC.

Compared with the non-monotonicity of the DAC, problem of missing codes are more serious in the adjustment of delay in VDL. For example, ideal capacitor bit-weights of a 9-bit binary weighted capacitor DAC is 1, 2, 4, 8, 16, 32, 64, 128 and 256 (bit-weight of unit capacitor is 1). If 128 weighted capacitor deviates to 134 due to process inconsistencies, it will cause missing codes between 128 LSB and 133 LSB in DAC output. Hence, DAC output will eventually jump back and forth between 127 LSB and 134 LSB once the end point of timing mismatch calibration convergence is between 128 and 133, as shown in Figure 5, which affects the accuracy of the calibration. In order to avoid this problem, the traditional approach is to limit the capacitor mismatch to a small range by simply using large capacitors. However, the large area, power consumption, and larger driving load brought by this approach are not what we want to see.



Figure 5. Simulated the calibration convergence with non-ideal 9 bit DAC.

In order to achieve an accurate timing mismatch correction without large capacitors, we propose the FSTC that is composed of MF-VDL in analog domain and RTM in digital domain. We still take the 9-bit precision correction as the example. First, the original 9-bit DAC is extended to a 10-bit DAC with a redundant bit in the analog domain to realize MF-VDL. Combining the previous step requirements with process matching, we set the redundant bit weight to 16. Now, the ideal bit-weights of the 10-bit DAC are 1, 2, 4, 8, 16, 16, 32, 64, 128, and 256. This MF-VDL is insensitive to miss code within 16. At the same time, we integrate the RTM in digital domain to expands the 9-bit digital control code of VDL  $d_m(n)$  into 10-bit digital control code  $d_{R,m}(n)$ . This module proceeds in three steps: (1) Divide the full-scale of the 9-bit digital control code into 32 intervals of length 16 as the input range of an ideal 9-bit DAC is 0 to 511 and the weight of the redundant bit is 16.

(2) Judge the current slope of the interval code by comparing the interval code of  $d_m(n)$  with the interval code of  $d_m(n - 1)$ .

(3) 10-bit  $d_{R,m}(n)$  can be obtained from 9-bit  $d_m(n)$  according to the result of whether to use the two 16 weighted capacitors (one is the binary 16 weighted capacitor and the other is the redundant 16 weighted capacitor) to realize the 32 weighted capacitor based on the slope of the interval code.

If the 128 weighted capacitor deviates to 134 in 10-bit DAC of proposed MF-VDL, the transmission curve of this DAC is shown in the Figure 6 combined with this algorithm. The algorithm can adjust the DAC output according to the direction of input code change. We can observe that the output of this DAC can coverage from 0 LSB to 511 LSB in Figure 6.



Figure 6. The conversion characteristic of non-ideal 10-bit DAC based on proposed algorithm.

Figure 7 show the simulation of the calibration convergence with non-ideal 10-bit DAC based on proposed algorithm. Compared to calibration convergence of non-ideal 9-bit DAC, the convergence will eventually reach 130 LSB if the end point of the timing mismatch calibration convergence is 130 LSB.



Figure 7. Simulated the calibration convergence with non-ideal 10 bit DAC based on proposed algorithm.

Depending on the combination of the MF-VDL in analog domain and RTM in digital domain, full coverage from 0 LSB to 511 LSB of the DAC output can be achieved as long as the smallest 5 capacitors are proportional and the mismatch of other capacitors does not exceed 16. This method can

guarantee an accurate correction result without missing codes, which greatly reduces the requirement for capacitor mismatch.

#### 3. ADC Implementation

The top-level architecture of the proposed 2.4 GS/s 12-bit ADC is shown in Figure 8. Considering the trade-off among speed, area, accuracy, and power dissipation, a four-channel TI structure is selected. The overall structure of the 600 MSps pipelined sub-ADC is also shown in Figure 8. In order to reduce power consumption and noise, the SHA-less technology is adopted. Each sub-ADC contains 5 levels of 2.5-bit multiplying digital-to-analog converter (MDAC) and a level of 2-bit flash. For the sake of further cutting down the power consumption, capacitances and operational amplifiers in the first three stages of MDAC have been scaled down proportionally. The inter-stage gain errors and the capacitor mismatches in the pipeline stages are main linearity error that limit the dynamic performance of the pipelined ADC [30,31]. Hence, these errors in the first three stages of MDAC are calibrated in digital domain before TI mismatch calibration.



Figure 8. Top-level architecture of the proposed 2.4GS/s 12bit ADC.

The clock circuit is a very important part of TI-ADC with high resolution or ultra-high sampling rate, so it needs to be designed carefully. Figure 9 is the specific clock scheme of the proposed ADC. The external master clock CLK\_IN is input to the CML buffer, and then transferred to a CMOS level clock through the CML to CMOS module. The clock divider module uses the CMOS level clock to generates four 50% duty cycle clocks p<n> with 90° phase difference, respectively. Then two adjacent clocks are input to the clock logic block of each sub-ADCs to generate a 25% non-overlapping sampling clock, which can reduce the crosstalk among the four sub-ADCs. At last, this non-overlapping sampling clock is aligned with 2.4 GHz master clock CLK<sub>m</sub> that has already been corrected by proposed timing mismatch calibration to generate the sampling clock of each channel.



Figure 9. Specific clock scheme of the proposed 2.4 GS/s 12-bit ADC.

Due to the different signal path and variation in the delay gates, the sub-ADC sampling clock cannot avoid shifting in different phases. Although the timing mismatch calibration module is designed on chip, we use the retiming technology to reduce the required calibration range. Figure 10a illustrates the block diagram of the retiming scheme. After retiming, the falling edges of the sampling clocks of four sub-ADCs  $\Phi'$  are aligned with the rising edges of master clock CLK<sub>m</sub> that has a sufficiently low clock jitter, as shown in Figure 10b. This greatly reduces the burden of timing mismatch calibration and sampling clock route.



**Figure 10.** (**a**) Block diagram of the retiming scheme; (**b**) Timing diagram of sub-ADC sampling clock before and after retiming.

However, the sampling time mismatch among channels that limited to hundreds of fs (RMS) is still remained after retiming in TI-ADC due to factors, such as layout, parasites, and device mismatches. It calls for timing mismatch calibration to minimize sampling time mismatch. In order to accomplish an accurate timing mismatch correction, a VDL without missing code is necessary. The MF-VDL designed in this paper can achieve a 20fs adjustment step and an adjustment range exceeding 10.24 ps. Figure 11 shows the schematic and layout of the MF-VDL used in this paper. The MF-VDL consisting of a 10 bit

capacitor DAC and 1X and 2X buffers. The entire MF-VDL is divided into two segments driven by 1X and 2X buffers to reduce power consumption and area. Meanwhile, the capacitors with different weights are all composed of LSB capacitor to ensure consistency. With the cooperation of module RTM implemented in digital domain, MF-VDL with redundant bit can eliminate the missing codes problem caused by mismatch. In terms of layout, the matching of the device is improved through adding a lot of dummy and optimizing the consistency of the routing and parasites. With the help of retiming and timing mismatch calibration, the timing mismatch of each channel can be compressed to the minimum.



Figure 11. (a) Schematic and (b) layout of the MF-VDL.

# 4. Measurement Results

The ADC prototype is manufactured in a 40nm CMOS process. The die micrograph is shown in Figure 12, including four sub-ADCs, clock input block, digital process module, efuse, and serdes output. The chip occupies an area of 3 mm  $\times$  3 mm. The TI mismatch calibration is implemented in digital process module. A large number of decoupling capacitors are filled in the spaces between different blocks to keep the power supply voltage clean and stable.



Figure 12. Prototype ADC micrograph.

Effect of calibration can be verified by variation of output spectrums before and after calibration. Figure 13 illustrates the output spectrums before and after calibration at 141 MHz input frequency. After calibration, the spurs resulting from timing mismatches fall to about 75 dB. The SFDR improves from 55.2 dB to 72.8 dB, and the SNDR rises from 52.3 dB to 55.7 dB. The convergence process of VDL control DAC output in timing mismatch calibration is presented in Figure 14a. It can be observed that the loop settles in about 15 cycles (each cycle collects 4096 points). The output spectrums before and after calibration at 1.3 GHz input frequency is presented in Figure 15. When the input frequency is raised to 1.3 GHz, the SFDR and SNDR can maintain 57.9 dB and 48.2 dB, respectively, which is similar to sub-ADCs' performance with the help of calibration. It can be seen that the spurs that are caused by timing mismatch have disappeared through the spectrum. The decrease in performance is mainly due to the performance degradation of the balun block on PCB, input buffer, and sub-ADCs in high frequency. As shown in Figure 15, the 2nd harmonic (HD2) is the main limitation for SFDR after timing mismatch calibration. The convergence process of VDL control DAC output in timing mismatch calibration is presented in Figure 14b. It shows that the module of automatic determination of convergence direction works properly in the second NB. For very low frequency or small amplitude input signals, the calibration cannot achieve a good calibration and eliminate the timing mismatch because the information about the timing mismatch carried by the digital output of the ADC is too little. But the effect of timing mismatch on the output of TI-ADC is also reduced accordingly, and the requirement for calibration is also much loose under these conditions.



**Figure 13.** Measured output spectrum when fin = 141 MHz (**a**) before timing mismatch calibration and (**b**) after timing mismatch calibration.



**Figure 14.** Convergence process of VDL control DAC output (**a**) when fin = 141 MHz and (**b**) when fin = 1.3 GHz.



**Figure 15.** Measured output spectrum when fin = 1.3 GHz (**a**) before timing mismatch calibration and (**b**) after timing mismatch calibration.

Figure 16 shows the ADC performance with and without timing mismatch calibration versus the input frequency at 2.4 GS/s. Under the condition of low input frequency, the SFDR can be improved more than 15 dB through the implementation of timing mismatch calibration. The SNDR is also slightly improved by the calibration. When the input frequency is above 1.2 GHz, the order harmonic grows rapidly and becomes the main limitation for SFDR. To a certain extent, the optimization of sub-ADCs and input buffer considering the trade-off between performance, power, and area can improve the high-frequency performance of the ADC. The SFDR of the ADC is above 60 dB across the entire first NB. The total ADC consumes 420 mW powered at 1.8 V and the Walden figure of merit (FOM) of 0.70 pJ/step is achieved.



**Figure 16.** SNDR/SFDR of the ADC versus frequency of the input signal before and after calibration at 2.4 GS/s.

Table 2 summarizes the comparison of our results with previous published papers for ADCs with higher than 10-bit resolution and faster than 1 GSps. Our work achieves a relatively good SFDR under the acceptable FOM with the help of the proposed calibration.

	[32]	[33]	[34]	[35]	[36]	This Work
Technology	40 nm	65 nm	65 nm	40 nm	65 nm	40 nm
Sampling rate (GS/s)	3	3.6	2.6	1	1	2.4
Supply (V)	2.5	1.2/2.5	1.2/1.3/1.6	1.8/1.3/0.9	2/1.2	1.8
ENOB@Nyquist (bits)	8.2	6.7	7.7	8.7	9.5	8.0
SNDR@Nyquist (dB)	51	42	48.5	54.2	56	49.7
SFDR@Nyquist (dB)	59	50	53.8	62	60.1	60.2
ERBW (GHz)	0.9	0.7	0.8	0.51	0.5	0.78
Area (mm <sup>2</sup> )	0.4	7.4	5.1	1.125	2.5	9
Power (mW)	500	795	480	250	230	420
FOM (pJ/step)	0.58	2.15	0.85	0.61	0.45	0.70

Table 2. Performance comparison with state-of-art ADCs.

# 5. Conclusions

This paper proposes a novel and low-cost timing mismatch calibration algorithm in TI-ADC. The automatic wideband timing-mismatch detection expands the frequency range of detection and increases the calibration speed. Based on the proposed MF-VDL, the full-scale traversal timing-mismatch correction accomplishes an accurate result without missing codes, which reduces the requirement for capacitance mismatch in the VDL and avoids the use of large capacitors. A 12-bit 2.4 GS/s four-channel TI pipelined ADC employing the proposed calibration on chip is presented. It exhibits a SNDR of 55.7 dB and SFDR of 72.8 dB for a 141 MHz input signal at 2.4 GS/s. With the help of calibration, the SFDR can be improved over 15 dB in low frequency input. The convergence time is approximately at  $6 \times 10^5$  samples, which is at the same level as that of other timing mismatch calibration for the TI-ADCs to remove the timing mismatch among channels with low cost.

**Author Contributions:** H.J. designed the circuits, analyzed the measurement data, and wrote the manuscript. X.G., D.W., L.Z. and J.L. assisted the circuit simulation and implementation. N.W. wrote the test program for this chip. Y.H. assisted the chip package implementation and the PCB designing. X.Z. and J.W. reviewed the manuscript. X.L. gave some valuable guidance and confirmed the final version of manuscript. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was funded by the National Key Research and Development Program of China (Grant No. 2017YFF0106602).

Conflicts of Interest: The authors declare no conflict of interest.

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