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# **Open-Loop Switched-Capacitor Integrator for Low Voltage Applications**

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**Abstract:** An architecture of a switched-capacitor integrator that includes a charge buffer operating in an open-loop is hereby proposed. As for the switched-capacitor filters, the gain of the proposed integrator, which is given by the input/output capacitor ratio, ensures desensitization to process, voltage, and temperature variations. The proposed circuit is suitable for low voltage supplies. It enables a significant power saving compared to a traditional switched-capacitor integrator. This was demonstrated through an analytical comparison between the proposed integrator and a traditional switched-capacitor integrator. The mathematical results were supported and verified by simulations performed on a circuit prototype designed in 16 nm finFET technology with 0.95 V supply. The proposed switched-capacitor integrator consumes 76  $\mu$ W, resulting in more than twice the efficiency for the traditional closed-loop switched-capacitor filter as an input voltage equal to 31.25 mV at 7 ns clock period is considered. The comparison of architectures was led among the proposed integrator and the state-of-the-art technology in terms of the figure of merit.

Keywords: switched-capacitor filters; low-voltage; finFET

# 1. Introduction

Switched-capacitor filters are used in a variety of applications like sensors interfaces [1], audio applications [2], RF front-ends [3], analog-to-digital converters [4], etc. The high accuracy, comparable to the capacitors mismatch and the ease of reprogramming, makes this topology preferable. Such filters require high-performance operational transconductance amplifiers (OTAs). Using modern IC technologies helps to reach high-frequency operation. However, obtaining high DC-gain becomes more challenging for two main reasons: the low supply voltage of the modern IC technologies that limit the number of stackable devices, generally used to obtain high DC-gain OTAs; the reduced length of the transistors that reduces the output resistances and limits the transistor intrinsic gain. On the other hand, the required high-DC gain is obtainable, increasing the number of gain stages of the OTA at the cost of higher power consumption.

In this paper, an open-loop switched-capacitor filter as a building block for the design of a higher-order switched-capacitor filter is presented. Despite its open-loop architecture, the integrator gain depends on the capacitor ratio whose accuracy is related to the capacitor mismatch as it is usually done in closed-loop switched-capacitor integrators. Furthermore, the proposed switched-capacitor integrator enables low voltage operation and relaxes the power requirement compared to the closed-loop counterpart. The paper is organized as follows: Section 2 starts with the analysis from the conventional switched-capacitor integrator used as a benchmark. Section 3 extends the analysis to the proposed open-loop integrator. Section 4 reports the simulation results and Section 5 concludes the paper.

# 2. The Closed Loop Switched-Capacitor Integrator

Figure 1 shows the conventional architecture of a switched capacitor integrator.



Figure 1. Conventional architecture of a closed-loop switched-capacitor integrator.

The switching scheme of this architecture is defined by two complementary clock phases,  $\phi_1$  and  $\phi_2$ . During  $\phi_1$  phase, the input signal,  $v_s$ , is sampled with the input capacitor,  $C_1$ . During  $\phi_2$  phase the charge collected by  $C_1$  is transferred to the feedback capacitor  $C_2$ , assuming an ideal virtual ground at the input of the OTA. The overall transfer function in Z-domain is the following

$$\frac{v_o}{v_s}(z) = -\frac{C_1}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}} \tag{1}$$

As in many other electronic systems, the feedback in this circuit serves two main functions:

- mitigate the impact of nonlinearities in the OTA;
- desensitize the overall transfer function to process, voltage, and temperature (PVT) variations.

The cost of these desirable features is an excessive OTA requirement.

# 2.1. Analysis of the Requirements of the Single Stage OTA

To evaluate the OTA requirements, a single-stage architecture was considered. The linear model of the OTA includes a transconductance  $g_m$  and an output resistance  $r_o$ . Figure 2 reports the linear model of the integrator including the model of the OTA.



**Figure 2.** Equivalent small-signal circuit of the closed-loop switched-capacitor integrator with a single-stage operational transconductance amplifier (OTA).

In a switched-capacitor integrator, the input signal,  $v_s$ , changes suddenly at each clock hit. Therefore,  $v_s$  can be assimilated to a step signal whose a maximum amplitude is equal to  $V_i$ :

$$v_s(t) = V_i \cdot u(t) \tag{2}$$

where u(t) is the unitary step signal.

The approach followed for this analysis is the following:

- 1 firstly, the transfer function  $\frac{v_0}{v_s}$  is calculated;
- 2 the output voltage  $v_o(s)$  is calculated in *s* domain multiplying the transfer function  $\frac{v_o}{v_s}$  and the Laplace transform of  $v_s(t)$ ;
- 3  $v_0(s)$  is then inverse transformed to get the output voltage,  $v_0(t)$ , in time domain.

The transfer function,  $\frac{v_o}{v_s}$ , is calculated as follows:

$$\frac{v_o}{v_s} = -\frac{C_1}{C_2 \cdot \left(1 + \frac{1 + \frac{C_1}{C_2}}{g_m \cdot r_o}\right)} \cdot \frac{1 - \frac{s \cdot C_2}{g_m}}{1 + \frac{s \cdot C_1}{g_m \left(1 + \frac{1 + \frac{C_1}{C_2}}{g_m \cdot r_o}\right)}} = -\frac{C_1}{C_2 \cdot \left(1 + \frac{1 + \frac{C_1}{C_2}}{A_o}\right)} \cdot \frac{1 - \frac{s \cdot C_2}{g_m}}{1 + \frac{s \cdot C_1}{g_m \left(1 + \frac{1 + \frac{C_1}{C_2}}{A_o}\right)}}$$
(3)

where  $A_0$  (= $g_m \cdot r_o$ ) is the OTA DC-gain. Assuming that both  $r_o$  and  $g_m$  tend to infinite,  $\frac{v_o}{v_s}$  can be approximate to the ideal value  $\frac{v_o}{v_s}\Big|_{ideal}$ :

$$\frac{v_o}{v_s}\Big|_{ideal} = \frac{v_o}{v_s}\Big|_{\substack{r_o \to \infty \\ g_m \to \infty}} = -\frac{C_1}{C_2}$$
(4)

The function  $v_s(t)$  reported in Equation (2) is transformed in s domain and combined with Equation (3), and then the inverse Laplace Transform is evaluated as follows:

$$v_{o}(t) = -\frac{C_{1}}{C_{2}\left(1 + \frac{1 + \frac{C_{1}}{C_{2}}}{A_{o}}\right)} \cdot V_{i} \cdot \left(1 - \frac{\tau_{z} + \tau_{p}}{\tau_{p}} \cdot e^{-\frac{t}{\tau_{p}}}\right)$$
(5)

where  $\tau_p$  and  $\tau_z$  are time constants calculated as reciprocal of pole and zero of the transfer function, i.e.,

$$\tau_p = \frac{C_1}{g_m \cdot \left(1 + \frac{1 + \frac{C_1}{C_2}}{A_o}\right)} \text{ and } \tau_z = \frac{C_2}{g_m}$$
(6)

Assuming  $A_0 \gg 1 + \frac{C_1}{C_2}$ ,  $\tau_p$  can be approximated as follows:

$$\tau_p \cong \frac{C_1}{g_m} \tag{7}$$

The output voltage  $v_o(0)$  at t = 0, is defined as:

$$v_{o}(0) = -\frac{C_{1}}{C_{2} \cdot \left(1 + \frac{1 + \frac{C_{1}}{C_{2}}}{A_{o}}\right)} \cdot V_{i} \cdot \left(1 - \frac{\tau_{z} + \tau_{p}}{\tau_{p}}\right) \cong V_{i}$$
(8)

The discontinuity is due to the zero in the transfer function.

# 2.2. Requirements of the Single Stage OTA

A finite gain of the OTA,  $A_0$ , and the non-null time is required for settling introduced errors on the output voltage. The OTA finite gain determines an error in a steady state. This error is called static error,  $\varepsilon_{stat}$ :

$$\varepsilon_{stat} = \left| \frac{v_o}{v_s} \right|_{ideal} V_i - v_o(t \to \infty) \right| \tag{9}$$

On the base of Equations (4) and (5), the static error,  $\varepsilon_{stat}$ , is calculated as follows:

$$\varepsilon_{stat} = \left(\frac{C_1}{C_2} - \frac{C_1}{C_2 \left(1 + \frac{1 + \frac{C_1}{C_2}}{A_o}\right)}\right) \cdot V_i = \frac{\frac{C_1}{C_2} \cdot \frac{1 + \frac{C_1}{C_2}}{A_o}}{1 + \frac{1 + \frac{C_1}{C_2}}{A_o}} \cdot V_i \cong \frac{C_1}{C_2} \cdot \frac{1 + \frac{C_1}{C_2}}{A_o} \cdot V_i$$
(10)

where the last approximation is valid as  $A_0 \gg 1 + \frac{C_1}{C_2}$ .

The charging process of the feedback capacitance,  $C_1$ , has a finite duration. In the following calculations, it is assumed that the duration of the charging phase is half of the clock period,  $T_{CLK}$ . Furthermore, an incomplete settling of the output voltage produces an error, which is called dynamic error,  $\varepsilon_{dyn}$ , which is defined as follows:

$$\varepsilon_{dyn} = \left| v_o(t \to \infty) - v_o\left(\frac{T_{CLK}}{2}\right) \right| \tag{11}$$

By using the expression of  $v_0(t)$ , reported in Equation (5), the dynamic error,  $\varepsilon_{dyn}$ , is calculated as follows:

$$\varepsilon_{dyn} = \frac{C_1}{C_2} \cdot V_i \cdot \frac{1}{1 + \frac{1 + \frac{C_1}{C_2}}{A_p}} \cdot \frac{\tau_z + \tau_p}{\tau_p} \cdot e^{-\frac{I_{CLK}}{2\tau_p}}$$
(12)

which can be simplified combining Equation (12) with Equations (6) and (7) that:

$$\varepsilon_{dyn} = \left(1 + \frac{C_1}{C_2}\right) \cdot V_i \cdot \frac{1}{1 + \frac{1 + \frac{C_1}{C_2}}{A_0}} e^{-\frac{T_{CLK}}{2 \cdot \tau_p}}$$
(13)

Figure 3 shows the qualitative behavior of the output voltage. Both static and dynamic errors are highlighted.



Figure 3. Output voltage behavior of the closed-loop switched-capacitor integrator in the linear regime.

The overall error,  $\varepsilon_{tot}$ , evalueated on the output voltage, is defined as the difference between the ideal output voltage,  $C_2/C_1 \cdot V_i$ , and the output voltage measured at  $T_{CLK}/2$ :

$$\varepsilon_{tot} = \left| \frac{C_2}{C_1} \cdot V_i - v_o \left( \frac{T_{CLK}}{2} \right) \right| = \varepsilon_{stat} + \varepsilon_{dyn} \tag{14}$$

As Equation (14) shows,  $\varepsilon_{tot}$  is calculated as the sum of  $\varepsilon_{stat}$  and  $\varepsilon_{dyn}$ .

# 2.2.1. DC-Gain Requirement of the Single-Stage OTA

The overall error must be less than the required accuracy,  $\xi$ , which is a parameter related to the application. According to the definition, both  $\varepsilon_{stat}$  and  $\varepsilon_{dyn}$  must be positive and smaller than the required accuracy,  $\xi$ .

To fulfill the DC-gain requirement, the accuracy of the static error,  $\varepsilon_{stat}$ , needs to be addressed as follows:

$$\varepsilon_{stat} < \xi$$
 (15)

Combining Equations (10) and (15), the following is obtained:

$$\frac{C_1}{C_2} \cdot \frac{1 + \frac{C_1}{C_2}}{A_o} \cdot V_i < \xi \tag{16}$$

Then, the following constraint on the DC-gain,  $A_0$ , is derived:

$$A_{o} > \frac{C_{1}^{2}}{C_{2}^{2}} \cdot \frac{V_{i}}{\xi} - 1 \cong \frac{C_{1}^{2}}{C_{2}^{2}} \cdot \frac{V_{i}}{\xi}$$
(17)

Since the DC-gain,  $A_o$ , undergoes process, voltage and temperature variations, the sensitivity of  $A_o, S_{A_0}^{v_o(\frac{T_{CLK}}{2})}$ , of the output voltage at  $t = \frac{T_{CLK}}{2}$ ,  $v_o(\frac{T_{CLK}}{2})$ , is evaluated from Equation (5) as follows:

$$S_{A_{0}}^{v_{o}(\frac{T_{CLK}}{2})} = \frac{A_{0}}{v_{o}(\frac{T_{CLK}}{2})} \cdot \frac{\partial v_{o}(\frac{T_{CLK}}{2})}{\partial A_{0}} = A_{0} \cdot \frac{1 + \frac{C_{1}}{C_{2}}}{\left(A_{0} + \frac{C_{1}}{C_{2}} + 1\right)^{2}} \cong \frac{1 + \frac{C_{1}}{C_{2}}}{A_{0}}$$
(18)

where last approximation is valid as  $A_0 \gg 1 + \frac{C_1}{C_2}$ .

### 2.2.2. Transconductance Requirement of the Single Stage OTA

A transconductance constrain is determined through the relation between the accuracy specification and the dynamic error,  $\varepsilon_{dyn}$ , i.e.:

$$\varepsilon_{dyn} < \xi \tag{19}$$

Combining Equations (13) and (19), it is obtained:

$$\left(1+\frac{C_1}{C_2}\right)\cdot V_i \frac{1}{1+\frac{1+\frac{C_1}{C_2}}{A_o}} \cdot e^{-\frac{T_{CLK}}{2\tau_p}} \cong \left(1+\frac{C_1}{C_2}\right) \cdot V_i \cdot e^{-\frac{T_{CLK}}{2\tau_p}} < \xi$$

$$(20)$$

The approximation contained in Equation (20) is justified as it is assumed that  $A_0 \gg 1 + \frac{C_1}{C_2}$ . Combining Equations (7) and (20) the following constraint on  $g_m$  is set:

$$g_m > \frac{2 \cdot C_1}{T_{CLK}} \cdot ln\left(\frac{V_i}{\xi} \cdot \left(1 + \frac{C_1}{C_2}\right)\right)$$
(21)

As for the DC-gain,  $A_o$ , the sensitivity of the output voltage,  $S_{g_m}^{v_o(\frac{T_{CLK}}{2})}$ , at  $\frac{T_{CLK}}{2}$ ,  $v_o(\frac{T_{CLK}}{2})$ , with respect to  $g_m$  is derived from Equation (5) as follows:

$$S_{g_{m}}^{v_{o}\left(\frac{T_{CLK}}{2}\right)} = \frac{g_{m}}{v_{o}\left(\frac{T_{CLK}}{2}\right)} \cdot \frac{\partial v_{o}\left(\frac{T_{CLK}}{2}\right)}{\partial g_{m}} = \frac{T_{CLK}}{2 \cdot \tau_{p}} \cdot \frac{\left(1 + \frac{2\tau_{z}}{T_{CLK}} + \frac{C_{2}}{C_{1}}\right)e^{-\frac{T_{CLK}}{2\tau_{p}}}}{1 - \left(1 + \frac{C_{2}}{C_{1}}\right)e^{-\frac{T_{CLK}}{2\tau_{p}}}} \cong \frac{T_{CLK}}{2 \cdot \tau_{p}} \cdot \left(1 + \frac{C_{2}}{C_{1}}\right) \cdot e^{-\frac{T_{CLK}}{2\tau_{p}}}$$
(22)

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where the last approximation is valid as  $(1 + \frac{C_2}{C_1}) e^{\frac{-T_{CLK}}{2\tau_p}} \ll 1$  and  $\tau_z \ll \frac{T_{CLK}}{2}$ .

# 2.3. Circuit Implementation of the Single Stage OTA

A common circuit solution for the OTA is represented by the telescopic Cascode OTA, shown in Figure 4 [5,6]. As the DC-gain requirement is satisfied and the output signal swing is sufficient, the telescopic Cascode OTA reported in Figure 2 remains the most efficient and simplest OTA solution. Therefore, it was used as a benchmark in this paper.



Figure 4. Telescopic Cascode OTA.

The overdrive voltage of  $M_1$ - $M_2$  input transistors is limited by the available supply voltage,  $V_{dd}$ , and the NMOS transistor threshold,  $V_{THN}$ . Assuming a common mode,  $V_{cm}$ , equal to  $V_{dd}/2$ , by applying Kirchoff's voltage law we obtain:

$$V_{cm} = \frac{V_{dd}}{2} = V_{GS1} + V_{DS0}$$
(23)

where  $V_{GS1}$  is the gate-source voltage of  $M_1$ - $M_2$  input transistors, and  $V_{DS0}$  is the drain-source voltage of the  $M_0$  bias transistor.

The common mode,  $V_{cm}$ , must assure that  $M_1$ - $M_2$  and the  $M_0$  transistors work in the saturation region. Therefore, assuming that all the overdrives of  $M_1$ - $M_2$  and  $M_0$  transistors are equal to  $V_{ov}$ , from Equation (23) we derive:

$$\frac{V_{dd}}{2} > V_{THN} + 2 \cdot V_{ov} \tag{24}$$

Thus:

$$V_{ov} < \frac{\frac{V_{dd}}{2} - V_{THN}}{2} \tag{25}$$

As seen in Equation (25), there is a strict limitation to the design of the overdrive of the input transistors at low supply voltage, which is typical of the modern CMOS IC technologies. For example, in finFET 16 nm technology,  $V_{dd}$  is 0.95 V, and  $V_{THN}$  is 0.275 V, therefore  $V_{ov}$  must be less than 100 mV.

# 2.4. Small Signal Analysis of the Single-Stage OTA

The transconductance  $g_m$  of the linear model of Figure 2 corresponds to the transconductance  $g_{m1}$  of  $M_1$ - $M_2$  input transistors. The bias current,  $I_B$ , of the OTA is defined by the settling requirements, which mainly depends on  $M_1$ - $M_2$  input transistors.

The output resistance  $r_0$  of the linear model of Figure 2 is calculated as follows:

$$r_o = g_{m3} \cdot r_{o3} \cdot r_{o1} || g_{m5} \cdot r_{o5} \cdot r_{o7} \cong \frac{1}{2} g_{m3} \cdot r_{o3} \cdot r_{o1}$$
(26)

where  $g_{m3}$  and  $g_{m5}$  are the transconductances of  $M_3$  and  $M_5$  transistors, respectively, and  $r_{o1}$ ,  $r_{o3}$ , and  $r_{o5}$  are the output resistances of  $M_1$ ,  $M_2$ , and  $M_3$  transistors, respectively. The last approximation in Equation (24) is valid assuming  $g_{m3} \cong g_{m5}$ ,  $r_{o3} \cong r_{o5}$ , and  $r_{o1} \cong r_{o7}$ . In practice, the output resistance of  $M_1$ - $M_2$  transistors,  $r_{o1}$ , is boosted by the intrinsic gain of transistor  $M_3$ ,  $g_{m3}$ : $r_{o3}$ .

The voltage gain,  $A_0$ , can be calculated as follows:

$$A_0 = g_{m1} \cdot r_o \cong \frac{1}{2} g_{m1} \cdot g_{m3} \cdot r_{o3} \cdot r_{o1}$$
(27)

Rearranging Equation (27), we obtain:

$$A_0 \cong 2 \cdot \frac{V_{A3} \cdot V_{A1}}{V_{ov3} \cdot V_{ov1}} \tag{28}$$

where  $V_{A3}$ ,  $V_{A1}$ ,  $V_{ov3}$ , and  $V_{ov1}$  are the early and the overdrive voltages of  $M_3$  and  $M_1$  transistors, respectively. As derived in Equation (28), the margins to increase the voltage gain  $A_o$  are limited. A possibility to increment the voltage gain consists of reducing  $V_{ov3}$  and  $V_{ov1}$ .  $M_3$  and  $M_1$  transistors are then pushed to work in the subthreshold region, where the transconductance depends only on the bias current, while the transistor overdrives approach their inferior limit of about 50 mV [7]. Therefore,  $V_{ov1}$  and  $V_{ov3}$  have a strict range of variability between 50 mV and 100 mV.  $V_{A3}$  and  $V_{A1}$  can be increased by augmenting the length of  $M_3$  and  $M_1$ . This solution degrades the frequency performance of the OTA since larger transistors introduce bigger parasitic capacitances. Moreover, every IC fabrication process has an intrinsic limit to the maximum allowable transistor length, which is lower and lower as the technology is scaled. For example, in FinFET 16 nm, the maximum allowable transistor length is 240 nm.

If the DC-gain requirement is not reachable by the telescopic Cascode OTA, it is necessary to modify the OTA architecture. An increment of  $r_0$  and, consequently,  $A_0$  is obtained by using a regulated Cascode OTA [8] or adding an output stage [9]. Both previous solutions imply a significant increase in power consumption. It is also possible to increase the gain by augmenting the number of stacked transistors. At low voltage supply, the last solution is not practicable because of the further reduction of the output signal swing.

# 2.5. Slew-Rate (SR) Analysis of the Single-Stage OTA

Due to the finite bias current,  $I_B$ , the OTA goes into a slew-rate regime at the beginning of the charging process.

According to Equation (5), the maximum rate of variation of the output voltage is obtained at t = 0 s.

$$\left|\frac{dv_o(t)}{dt}\right|_{max} = \frac{C_1}{C_2 \cdot \left(1 + \frac{1 + \frac{C_1}{C_2}}{A_o}\right)} \cdot V_{SRi,max} \cdot \frac{\tau_z + \tau_p}{\tau_p^2} = \frac{V_{SRo,max}}{\tau_p}$$
(29)

where  $V_{SRi,max}$  is the maximum amplitude of the input voltage step that keeps the OTA in the linear region. The corresponding output voltage in steady state is given by  $V_{SRo,max}$ , which is calculated as follows:

$$V_{SRo,max} = \frac{C_1}{C_2 \cdot \left(1 + \frac{1 + \frac{C_1}{C_2}}{A_o}\right)} \cdot \left(1 + \frac{C_2}{C_1}\right) \cdot V_{SRi,max} \cong \left(1 + \frac{C_1}{C_2}\right) \cdot V_{SRi,max}$$
(30)

where the last approximation is valid as  $A_0 >> 1 + C_1/C_2$ . In a single-stage OTA, the slew-rate depends on the bias current  $I_B$  and the feedback capacitance  $C_2$ , i.e.:

$$SR = \frac{I_B}{C_2} = \frac{I_B \cdot g_{m1}}{C_2 \cdot g_{m1}} = \frac{V_{ov1}}{\tau_z}$$
(31)

where  $g_{m1}$  and  $V_{ov1}$  are the transconductance and the overdrive of the  $M_1$ - $M_2$  input transistors, respectively. Matching the *SR* formula in Equation (31) to the maximum rate of variation of the output voltage reported in Equation (29), the  $V_{SRo,max}$  calculation is obtained:

$$V_{SRo,max} = V_{ov1} \cdot \frac{\tau_p}{\tau_z} \cong V_{ov1} \cdot \frac{C_1}{C_2}$$
(32)

Due to its differential structure, the OTA starts slewing as the input differential voltage step,  $V_i$ , overcomes 2· $V_{SRi,max}$ . The value of  $V_{SRi,max}$  is calculated by combining Equations (30) and (32):

$$V_{SRi,max} \cong \frac{1}{\left(1 + \frac{C_1}{C_2}\right)} \cdot V_{SRo,max} = \frac{V_{ov1}}{\left(1 + \frac{C_2}{C_1}\right)}$$
(33)

The OTA slews until the output voltage reaches the value  $\frac{-C_1}{C_2}V_i + 2V_{SRo,max}$ :

$$V_{i} - \frac{2 \cdot V_{SRo,max}}{\tau_{p}} t|_{t=\tau_{s}} = -\frac{C_{1}}{C_{2}} V_{i} + 2 \cdot V_{SRo,max}$$
(34)

where the starting value of  $V_i$  depends on the fact that, at t = 0 s, the capacitances of the integrator behave like short circuits, transferring the input voltage directly to the output.

From the previous equation, it is possible to calculate the slewing time of the OTA,  $\tau_s$ :

$$\tau_s = \tau_p \cdot \left( \left( 1 + \frac{C_1}{C_2} \right) \cdot \frac{V_i}{2 \cdot V_{SRo,max}} - 1 \right) = \tau_p \cdot \left( \frac{V_i}{2 \cdot V_{SRi,max}} - 1 \right)$$
(35)

During  $\tau_s$ , the OTA output voltage evolves according to the linear law. Considering the slew-rate, the equation of the differential output voltage,  $v_{od}(t)$ , is then calculated as follows:

$$\begin{cases} v_{od}(t) = V_i - \frac{2 \cdot V_{SRo,max}}{\tau_p} \cdot t & \text{for } 0 < t < \tau_s \\ v_{od}(t) = -\frac{C_1}{C_2 \cdot \left(1 + \frac{1 + \frac{C_1}{C_2}}{A_o}\right)} \cdot V_i + 2 \cdot V_{SRo,max} \cdot e^{-\frac{t - \tau_s}{\tau_p}} \cong -\frac{C_1}{C_2} \cdot V_i + 2 \cdot V_{SRo,max} e^{-\frac{t - \tau_s}{\tau_p}} \text{for } t > \tau_s \end{cases}$$
(36)

Figure 5 shows the step response of the closed loop switched capacitor integrator including the slewing period.



**Figure 5.** Output voltage behavior of the closed-loop switched-capacitor integrator including the slewing period.

# 2.6. Signal to Noise (SNR) Calculations of the Closed-Loop Switched-Capacitor Integrator

The telescopic Cascode OTA suffers from a reduced output swing. Indeed, both single-ended output voltages must guarantee that the Cascode transistors ( $M_3$ - $M_4$  and  $M_5$ - $M_6$ ) work in a saturation region even under the signal swing. The main limitation is the negative output swing since three transistors are stacked between the ground and the output nodes, while only two transistors are stacked between  $V_{dd}$  and the output nodes. Focusing the analysis on a single branch,  $V_{o+}$  must satisfy the following inequation to guarantee that  $M_3$  transistors operate in saturation region:

$$V_{o+} > V_{DS,sat3} + V_{S3} = V_{ov} + V_{S3}$$
(37)

where  $V_{S3}$  and  $V_{DS,sat3}$  are the source and the saturation voltages of  $M_3$  transistor, respectively. It is assumed that  $V_{ds,sat3}$  is equal to  $V_{ov}$ . The bias voltage  $V_{b1}$  is chosen to make  $M_1$  transistor operating in saturation, i.e.:

$$V_{DS1} = V_{S3} - V_{S1} > V_{DS,sat1} = V_{ov}$$
(38)

where  $V_{DS1}$ ,  $V_{S1}$ , and  $V_{DS,sat1}$  are the drain-source, the source, and the saturation voltages of  $M_1$  transistor, respectively. In this case, it is assumed that  $V_{ds,sat1}$  is equal to  $V_{ov}$ .  $V_{S1}$  is derived from the input transistor common mode,  $V_{cm}$ , by dropping the gate-drain voltage of the  $M_1$  transistors,  $V_{GS1}$ , i.e.:

$$V_{S1} = V_{cm} - V_{GS1} = V_{cm} - V_{TH} - V_{ov}$$
(39)

Combining Equations (38) and (39) we obtain the minimum source voltage of  $M_3$  transistor,  $V_{S3,min}$ :

$$V_{S3} > V_{S1} + V_{ov} = V_{S3,min} \tag{40}$$

By replacing  $V_{S3}$  in Equation (37) with the value of  $V_{S3,min}$  calculated in Equation (40), the minimum value of  $V_{o+}$ ,  $V_{o+,min}$ , is obtained:

$$V_{o+} > V_{ov} + V_{S3} = V_{cm} - V_{THN} = V_{o+,min}$$
(41)

As the output voltage starts swinging from the common-mode voltage,  $V_{cm}$ , down to  $V_{o+,min}$ , it is possible to calculate the maximum output voltage swing,  $V_{swing}$ :

$$V_{swing} = 2 \cdot (V_{cm} - V_{o+,min}) = 2 \cdot V_{THN}$$

$$\tag{42}$$

where the 2 factor is due to the differential architecture.

The thermal noise due to the switches around  $C_1$  is calculated as  $2 \cdot \frac{K \cdot T}{C_1}$ , where the coefficient 2 takes into account both the sampling ( $\phi_1$ ) and the integration phase ( $\phi_2$ ). Assuming that the thermal noise  $2 \cdot \frac{K \cdot T}{C_1}$  is dominant, from Equation (42), the signal to noise ratio of the overall closed-loop switched-capacitor integrator,  $SNR_{CL}$ , is calculated as follows:

$$SNR_{CL} = \frac{1}{2} \cdot \frac{V_{swing}^2}{\overline{v_{o,n}^2}} = \frac{1}{2} \cdot \frac{4 \cdot V_{THN}^2}{2 \cdot \frac{K \cdot T}{C_1} \cdot \left(\frac{C_1}{C_2}\right)^2} = \frac{V_{THN}^2 \cdot C_2^2}{K \cdot T \cdot C_1}$$
(43)

where  $\overline{v_{n,o}^2}$  is the total output noise, as a result of the thermal noise contribution due to the  $C_1$  switched-capacitor multiplied by the square of the integrator gain  $\left(\frac{C_1}{C_2}\right)^2$ , furthermore, the  $\frac{1}{2}$  factor takes into account that the input signal is a sinusoid.

### 2.7. Power Consumption Requirements

Regarding the telescopic Cascode shown in Figure 4, the power consumption is given by the product of the supply voltage,  $V_{dd}$ , and the bias current  $I_B$ :

$$P_{w,tot} = V_{dd} \cdot I_B \tag{44}$$

Assuming dominant the thermal noise of  $C_1$ , the power consumption of the switched-capacitor integrator is determined by the settling time requirement. In fact, as the input transistor overdrive,  $V_{ov1}$ , is bonded to considerations on the DC-point at low voltage supply, the constraint on the input transistor transconductance,  $g_{m1}$ , expressed by in Equation (21), determines the minimum required bias current  $I_{B,min}$ :

$$I_{B,min} = \frac{2 \cdot C_1}{T_{CLK}} \cdot V_{ov1} \cdot ln\left(\frac{V_i}{\xi} \cdot \left(1 + \frac{C_1}{C_2}\right)\right)$$
(45)

Therefore, the minimum power consumption,  $P_{w,min}$ , is obtained as follows:

$$P_{w,min} = V_{dd} \cdot I_{B,min} = V_{dd} \cdot \frac{2 \cdot C_1}{T_{CLK}} \cdot V_{ov1} \cdot ln\left(\frac{V_i}{\xi} \cdot \left(1 + \frac{C_1}{C_2}\right)\right)$$
(46)

As the OTA starts slewing, the minimum bias current,  $I_{B,min}$ , is determined by taking into account a different calculation for the dynamic error,  $\varepsilon_{dyn}$ . Indeed, considering Equation (36) that assumes the slewing of the OTA, the differential output voltage at  $t = \frac{T_{CLK}}{2}$  is calculated as follows:

$$v_{od}\left(\frac{T_{CLK}}{2}\right) \simeq -\frac{C_1}{C_2} \cdot V_i + 2 \cdot V_{SRo,max} \cdot e^{-\frac{T_{CLK}}{2} - \tau_s}$$
(47)

The dynamic error,  $\varepsilon_{dyn}$ , is, then, calculated as follows:

$$\varepsilon_{dyn} = \left| v_{od}(t \to \infty) - v_o\left(\frac{T_{CLK}}{2}\right) \right| = 2 \cdot V_{SRo,max} e^{-\frac{T_{CLK}}{2} - \tau_s}$$
(48)

Since  $\varepsilon_{dyn}$  must be less than the required accuracy,  $\xi$ , as reported in Equation (19), we obtain:

$$\tau_p < \frac{\frac{T_{CLK}}{2} - \tau_s}{ln\left(\frac{2V_{SRo,max}}{\xi}\right)}$$
(49)

Moreover, the minimum bias current  $I_{B,min}$  is evaluated considering  $\tau_p$  reported in Equation (7), the transconductance of the input transistors,  $g_{m1}$ , determined as  $\frac{I_{B,min}}{V_{op1}}$ , the formula of the slewing

time,  $\tau_s$ , in Equation (35), and the previous equation. As a result the minimum bias current  $I_{B,min}$ , is calculated as follows:

$$I_{B,min} = \frac{2 \cdot V_{ov1} \cdot C_1}{T_{CLK}} \cdot \left( ln \left( \frac{2 \cdot V_{SRo,max}}{\xi} \right) + \frac{V_i}{2 \cdot V_{SRi,max}} - 1 \right)$$
(50)

The minimum power consumption,  $P_{w,min}$ , is derived from the last equation as follows:

$$P_{w,min} = V_{dd} \cdot I_{B,min} = \frac{2 \cdot V_{ov1} \cdot V_{dd} \cdot C_1}{T_{CLK}} \cdot \left( ln \left( \frac{2 \cdot V_{SRo,max}}{\xi} \right) + \frac{V_i}{2 \cdot V_{SRi,max}} - 1 \right)$$
(51)

# 3. Proposed Open-Loop Integrator

As an alternative solution, an open-loop switched-capacitor integrator is presented (Figure 6).



Figure 6. Schematic of the proposed open-loop switched-capacitor integrator.

The active element is an OTA, with a low input impedance, which is called charge buffer. Once the input capacitance,  $C_1$ , is connected to the charge buffer input, it is discharged and its charge is transferred to the output capacitance  $C_2$ . The proposed open-loop switched-capacitor integrator does not include two input nodes with high and low impedances, unlike the switched-capacitor integrator based on a current conveyor [10,11], but only low impedance input nodes. Therefore, the voltage buffer used at the input in the conveyor integrators is eliminated. These simplifications help to get a more efficient circuit implementation.

According to the operation mode aforementioned,  $C_1$  is connected to the inverting input terminal, it is possible to write:

$$Q_1(n-1) = -Q_2(n) \tag{52}$$

where  $Q_1(n-1)$  and  $Q_2(n)$  are the charges stored in  $C_1$  and  $C_2$  capacitances, at n-1 and n time steps, respectively. From Equation (52), it is obtained:

$$C_1 \cdot v_s(n-1) = -C_2 \cdot v_o(n) \tag{53}$$

where  $v_o$  and  $v_s$  are the output and the input voltages. Therefore, it is possible to calculate the integrator gain in the Z domain,  $\frac{v_o}{v_s}(z)$ :

$$\frac{v_o}{v_s}(z) = -\frac{C_1}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}}$$
(54)

By using the proposed approach, we obtain a gain expression, which is identical to the traditional closed-loop integrator reported in Equation (1). In both cases, the desensitization of the gain concerning the OTA parameters is reached as the gain depends only on the  $C_1$  and  $C_2$  capacitor ratio, in the ideal case.

# 3.1. Small Signal Analysis of the Proposed Charge Buffer

To evaluate the impact of the non-null input resistance and the finite output resistance of the charge buffer, the linear model of the integrator reported in Figure 7 was considered.



Figure 7. The linear model of the open-loop switched-capacitor integrator.

In practice, the  $C_1$  capacitance is discharged on input resistance  $r_i$ , producing the input current  $i_i$ . This current is amplified with a current gain  $A_i$  by the current amplifier that feds the output load made by the output resistance  $r_o$  and the output capacitance  $C_2$ .

First of all, the transfer function,  $\frac{v_0}{v_s}(s)$ , is calculated as previously done for the traditional closed-loop switched-capacitor integrator:

$$\frac{v_o}{v_s}(s) = -A_i \cdot \frac{s \cdot C_1}{1 + s \cdot r_i \cdot C_1} \cdot \frac{r_o}{1 + s \cdot r_o \cdot C_2}$$
(55)

Compared to the transfer function of the closed-loop switched-capacitor integrator shown in Equation (3), the transfer function of the open-loop switched-capacitor integrator already is calculated, has an additional pole due to the finite output resistance  $r_0$ .

#### 3.2. Transient Analysis of the Proposed Charge Buffer

Assuming a step signal at the input as reported in Equation (2), the output voltage becomes:

$$v_{o}(t) = -\frac{C_{1}}{C_{2}} \cdot A_{i} \cdot V_{i} \cdot \frac{1}{1 - \frac{r_{i}}{r_{o}} \cdot \frac{C_{1}}{C_{2}}} \left( e^{-\frac{t}{\tau_{p2}}} - e^{-\frac{t}{\tau_{p1}}} \right)$$
  
$$= -\frac{C_{1}}{C_{2}} \cdot A_{i} \cdot V_{i} \cdot \frac{1}{1 - \frac{C_{1}}{A_{v} \cdot C_{2}}} \left( e^{-\frac{t}{\tau_{p2}}} - e^{-\frac{t}{\tau_{p1}}} \right)$$
(56)

where:

$$\tau_{p1} = r_i \cdot C_1, \ \tau_{p2} = r_o \cdot C_2 \qquad A_v = \frac{r_o}{r_i}$$
(57)

 $A_v$  is the voltage gain. The error on the current gain,  $A_i$ , of the current mirror, directly affects the accuracy of the output voltage. This error mainly depends on the transistor mismatch, which can be minimized thanks to the appropriate design of the overdrive of the transistors forming the current mirror [12].

The output resistance  $r_o$ , partially drags the charge stored in  $C_2$ . Considering a first-order Taylor's expansion for the  $e^{-t/\tau p^2}$  term, and assuming a unitary current gain, the output voltage,  $v_o(t)$ , at  $t = T_{CLK}/2$ , is calculated as follows from Equation (56):

$$v_{o}\left(\frac{T_{CLK}}{2}\right) \cong -\frac{C_{1}}{C_{2}} \cdot \frac{1}{1 - \frac{C_{1}}{A_{v} \cdot C_{2}}} \cdot V_{i} \cdot \left(1 - \frac{T_{CLK}}{2 \cdot \tau_{p2}} - e^{-\frac{T_{CLK}}{2 \cdot \tau_{p1}}}\right)$$
(58)

Three sources of error on the output voltage at  $t = \frac{T_{CLK}}{2}$ ,  $v_o(\frac{T_{CLK}}{2})$ , remain. They are due to:

- finite voltage gain  $A_v$ ;
- non-null  $\tau_{p1}$ ;
- finite  $\tau_{p2}$ .

The impact of each source of error is evaluated considering the remaining ones disabled.

To evaluate the error,  $\varepsilon_r$ , due to the finite voltage gain,  $A_v$ , it is assumed that  $\tau_{p1}$  tends to zero and  $\tau_{p2}$  tends to infinite. In these conditions, the output voltage can be approximated as follows:

$$\left. \begin{array}{c} v_o \left( \frac{T_{CLK}}{2} \right) \right|_{\substack{\tau_{p1} \to 0 \\ \tau_{p2} \to \infty}} \cong -\frac{C_1}{C_2} \cdot \frac{1}{1 - \frac{C_1}{A_v \cdot C_2}} \cdot V_i$$

$$(59)$$

The corresponding error,  $\varepsilon_r$ , is calculated as the difference between the ideal voltage obtained using the ideal gain value shown in Equation (54), and the value of the voltage expressed in Equation (59), i.e.,

$$\varepsilon_r = \begin{vmatrix} -\frac{C_1}{C_2} \cdot V_i - v_o \left( \frac{T_{CLK}}{2} \right) \middle| & \tau_{p1} \to 0 \\ \tau_{p2} \to \infty \end{vmatrix} = \frac{C_1}{C_2} \cdot \frac{\frac{C_1}{A_v \cdot C_2}}{1 - \frac{C_1}{A_v \cdot C_2}} \cdot V_i$$
(60)

To evaluate the error due to  $\tau_{p1}$ , it is assumed that  $\tau_{p2}$  tends to infinite. In these conditions, the output voltage can be approximated as follows:

$$v_o\left(\frac{T_{CLK}}{2}\right)\Big|_{\tau_{p2}\to\infty} = -\frac{C_1}{C_2} \cdot \frac{1}{1 - \frac{C_1}{A_v \cdot C_2}} \cdot V_i \cdot \left(e^{-\frac{T_{CLK}}{2 \cdot \tau_{p1}}} + 1\right)$$
(61)

The error due to  $\tau_{p1}$ ,  $\varepsilon_{\tau p1}$ , is calculated as the difference between the output voltages expressed in Equations (50) and (52), i.e.:

$$\varepsilon_{\tau p1} = \left| v_o \left( \frac{T_{CLK}}{2} \right) \right|_{\substack{\tau_{p1} \to 0 \\ \tau_{p2} \to \infty}} - v_o \left( \frac{T_{CLK}}{2} \right) \right|_{\substack{\tau_{p2} \to \infty}} = \frac{C_1}{C_2} \cdot \frac{1}{1 - \frac{C_1}{A_v \cdot C_2}} \cdot V_i \cdot e^{\frac{-T_{CLK}}{2 \cdot \tau_{p1}}}$$
(62)

The error due to  $\tau_{p2}$ ,  $\varepsilon_{\tau p2}$ , is calculated as the difference between the output voltages expressed in Equations (58) and (61), i.e.:

$$\varepsilon_{\tau p2} = \left| v_o \left( \frac{T_{CLK}}{2} \right) - v_o \left( \frac{T_{CLK}}{2} \right) \right|_{\tau_{p2} \to \infty} \right| = \frac{C_1}{C_2} \cdot \frac{1}{1 - \frac{C_1}{A_v \cdot C_2}} \cdot V_i \cdot \frac{T_{CLK}}{2 \cdot \tau_{p2}}$$
(63)

Figure 8 shows the output voltage behavior.



Figure 8. Output voltage behavior of the open-loop switched-capacitor integrator in the linear regime.

The sum of the three error  $\varepsilon_r$ ,  $\varepsilon_{\tau p1}$ , and  $\varepsilon_{\tau p2}$ , gives the total error  $\varepsilon_{tot}$ , which must be less than the required accuracy,  $\xi$ :

$$\varepsilon_{tot} = \varepsilon_r + \varepsilon_{\tau p1} + \varepsilon_{\tau p2} < \xi \tag{64}$$

Since the error terms  $\varepsilon_r$ ,  $\varepsilon_{\tau p1}$ , and  $\varepsilon_{\tau p2}$  are positive, each of them must be less than  $\xi$ .

# 3.3. Voltage Gain Requirement of the Proposed Charge Buffer

As calculated in Equation (60),  $\varepsilon_r$  is less than the  $\xi$ , therefore, we obtain

$$A_{v} > \frac{C_{1}}{C_{2}} \cdot \left(1 + \frac{V_{i}}{\xi} \cdot \frac{C_{1}}{C_{2}}\right) \cong \frac{V_{i}}{\xi} \cdot \frac{C_{1}^{2}}{C_{2}^{2}}$$

$$\tag{65}$$

In Equation (65) is very similar to Equation (17), which defines the requirement of the OTA for the closed-loop switched-capacitor integrator. It can be concluded that the charge buffer of the proposed open-loop switched-capacitor integrator requires the same gain of the OTA in the traditional closed-loop solution.

From Equation (58), the sensitivity,  $S_{A_v}^{v_o(\frac{T_{CLK}}{2})}$ , of the output voltage at  $\frac{T_{CLK}}{2}$ ,  $v_o(\frac{T_{CLK}}{2})$ , and  $A_v$  is evaluated as follows:

$$S_{A_v}^{v_o(\frac{T_{CLK}}{2})} = \frac{A_v}{v_o(\frac{T_{CLK}}{2})} \cdot \frac{\partial v_o(\frac{T_{CLK}}{2})}{\partial A_v} = \frac{A_v \cdot \frac{C_1}{C_2}}{\left(A_v - \frac{C_1}{C_2}\right)^2} \cong \frac{A_v \cdot \frac{C_1}{C_2}}{\left(A_v - \frac{C_1}{C_2}\right)^2} \tag{66}$$

where the last approximation is valid as  $A_v \gg \frac{C_1}{C_2}$ . The previous result is very similar to the one obtained for the Cascode OTA in the closed-loop switched-capacitor integrator in Equation (18).

3.4. Input and Output Resistances Requirements of the Proposed Charge Buffer

Assuming  $\varepsilon_{\tau p1}$ , calculated in Equation (62), less than  $\xi$  we obtain

$$\pi_{p1} < \frac{T_{CLK}}{2 \cdot ln \left(\frac{V_i}{\xi \cdot \left(1 - \frac{C_1}{A_U \cdot C_2}\right) \cdot \frac{C_2}{C_1}}\right)} \cong \frac{T_{CLK}}{2 \cdot ln \left(\frac{V_i}{\xi} \cdot \frac{C_1}{C_2}\right)}$$
(67)

Last approximation in Equation (67) is valid as  $A_v \gg \frac{C_1}{C_2}$ .

Taking into account the expression of  $\tau_{p1}$  in Equation (57), the following constraint on the input resistance,  $r_i$ , is obtained:

$$r_i < \frac{T_{CLK}}{2 \cdot C_1 \cdot ln\left(\frac{V_i}{\xi} \cdot \frac{C_1}{C_2}\right)}$$
(68)

Assuming  $\varepsilon_{\tau p2}$ , calculated in Equation (63), less than  $\xi$  we obtain

$$\tau_{p2} > \frac{T_{CLK}}{2} \cdot \frac{V_i}{\xi \cdot \left(1 - \frac{C_1}{A_v \cdot C_2}\right)} \cdot \frac{C_1}{C_2} \cong \frac{T_{CLK}}{2} \cdot \frac{V_i}{\xi} \cdot \frac{C_1}{C_2}$$
(69)

In this case, last approximation is valid as  $A_v \gg \frac{C_1}{C_2}$ . Considering  $\tau_{p2}$  in Equation (57), from Equation (69) it is derived the following constraint on the output resistance, r<sub>o</sub>:

$$r_o > \frac{T_{CLK}}{2} \cdot \frac{V_i}{\xi} \cdot \frac{C_1}{C_2^2}$$
(70)

As already done for the voltage gain,  $A_v$ , from Equation (58) the sensitivity,  $S_{r_i}^{v_0(\frac{l_{CLK}}{2})}$ , of the output voltage at  $\frac{T_{CLK}}{2}$ ,  $v_o(\frac{T_{CLK}}{2})$ , and  $r_i$  is evaluated as follows:

$$S_{r_{i}}^{v_{o}\left(\frac{T_{CLK}}{2}\right)} = \frac{r_{i}}{v_{o}\left(\frac{T_{CLK}}{2}\right)} \cdot \frac{\partial v_{o}\left(\frac{T_{CLK}}{2}\right)}{\partial r_{i}} = \frac{T_{CLK}}{2 \cdot \tau_{p1}} \cdot \frac{e^{\frac{-T_{CLK}}{2\tau_{p1}}}}{1 - \frac{T_{CLK}}{2 \cdot \tau_{p2}} - e^{\frac{-T_{CLK}}{2 \cdot \tau_{p1}}}} \cong \frac{T_{CLK}}{2 \cdot \tau_{p1}} e^{\frac{-T_{CLK}}{2 \cdot \tau_{p1}}}$$
(71)

where last approximation is valid as  $\frac{T_{CLK}}{2 \cdot \tau_{p2}} - e^{\frac{-T_{CLK}}{2 \cdot \tau_{p1}}} \ll 1$ . This inequation is verified as the condition imposed by Equations (67) and (69) are satisfied, since, generally,  $V_i \gg \xi$  and  $\frac{C_1}{C_2} \ge 1$ . It can be seen that the result of the calculation of the sensitivity of the output voltage compared to  $r_i$  is very similar to the one obtained for the calculation of the output voltage sensitivity for  $g_m$  of the Cascode OTA in the closed-loop switched-capacitor integrator in Equation (22).

Regarding the sensitivity, it can be concluded that the proposed switched-capacitor integrator, despite working in an open-loop configuration, has a robustness to PVT variations similar to the closed-loop switched-capacitor integrator.

However, since the performance of the proposed open-loop switched-capacitor integrator depends on the output resistance of the charge buffer,  $r_o$ , the sensitivity,  $S_{r_o}^{v_o(\frac{T_{CLK}}{2})}$ , of the output voltage at  $\frac{T_{CLK}}{2}$ ,  $v_o(\frac{T_{CLK}}{2})$ , and  $r_o$  is calculated as:

$$S_{r_o}^{v_o(\frac{T_{CLK}}{2})} = \frac{r_i}{v_o(\frac{T_{CLK}}{2})} \cdot \frac{\partial v_o(\frac{T_{CLK}}{2})}{\partial r_i} = \frac{T_{CLK}}{2 \cdot \tau_{p2}} \cdot \frac{1}{1 - \frac{T_{CLK}}{2 \cdot \tau_{p2}} - e^{\frac{-T_{CLK}}{2 \cdot \tau_{p2}}}} \cong \frac{T_{CLK}}{2 \cdot \tau_{p2}}$$
(72)

According to Equation (69) and considering that  $\frac{V_i}{\xi} \gg 1$  and  $\frac{C_1}{C_2} \ge 1$ , it can be assumed that  $S_{r_o}^{v_o(\frac{l_{CLK}}{2})}$  is quite less than 1. Therefore, the impact of the  $r_o$  variation on the integrator performance is limited.

# 3.5. Circuit Implementation of the Proposed Charge Buffer

Figure 9 shows a possible circuit implementation of the charge buffer. The switched capacitors network at the output nodes is used to set the output common-mode voltage at  $V_{cm}$ . Reference  $V_{b1}$  is designed to set the input common-mode voltage at  $V_{cm}$ . To keep  $M_2$  and  $M_8$  transistors in the saturation region, their source-drain voltage must be more than their saturation voltage, i.e.:

$$V_{SD2} = V_{dd} - V_{cm} > V_{SD2,sat} \tag{73}$$

It is supposed that  $V_{cm}$  is equal to half supply voltage and the saturation voltages correspond to the transistor overdrive,  $V_{ov2}$ , from Equation (73) we derive

$$V_{ov2} < \frac{V_{dd}}{2} \tag{74}$$

To bias the  $M_1$  transistor in the saturation region, it must be guaranteed that its source-drain voltage,  $V_{SD1}$ , overcomes its saturation voltage, corresponding to the transistor overdrive,  $V_{ov1}$ , i.e.:

$$V_{SD1} > V_{ov1} \tag{75}$$

From the last equation, we obtain

$$V_{SD1} = V_{cm} - V_{dd} + |V_{THP}| + V_{ov2} > V_{ov1}$$
(76)

Assuming  $V_{cm} = V_{dd}/2$ , the last equation can be rearranged to obtain a constraint on the difference between the  $M_1$  and  $M_2$  transistors overdrives,  $\Delta V_{ov2-1}$ , i.e.:

$$\Delta V_{ov2-1} = V_{ov2} - V_{ov1} > \frac{V_{dd}}{2} - |V_{THP}|$$
(77)

Using the finFET 16 nm we obtain the result  $V_{dd} = 0.95$  V,  $V_{THP} = 0.4$  V. Consequently,  $\Delta V_{ov2-1}$  must be higher than 75 mV.

According to Equations (74) and (77), using a charge buffer in open-loop configuration gives more flexibility to the design since larger overdrives can be defined for the transistors, to employing an OTA in a closed-loop fashion. This is extremely important at low voltage supply.



Figure 9. Circuit implementation of the charge buffer.

The input and the output resistances,  $r_i$  and  $r_o$ , are calculated as follows:

$$r_i \simeq \frac{1}{g_{m1} \cdot g_{m2} \cdot r_{ds3}} = \frac{V_{ov1} \cdot V_{ov2}}{4 \cdot V_{A3} \cdot I_B}; \qquad r_o \simeq r_{ds6} = \frac{V_{A6}}{I_B}$$
(78)

where  $g_{m1}$  and  $g_{m2}$  are the transconductance of  $M_1$  and  $M_2$  transistors, respectively, while  $r_{ds3}$  and  $r_{ds6}$  are the output resistance of  $M_3$  and  $M_6$  transistors, respectively.

The voltage gain,  $A_v$ , is calculated as follows:

$$A_{v} = \frac{r_{o}}{r_{i}} = \frac{4 \cdot V_{A3} \cdot V_{A6}}{V_{ov1} \cdot V_{ov2}}$$
(79)

The telescopic Cascode OTA reported in Figure 4 implements the boost of the output resistance,  $r_0$ . On the other end, the proposed charge buffer circuit enables the boosting of the transconductance of the input transistors,  $g_{m1}$ , by a  $g_{m2}$ · $r_{ds3}$  factor, lowering the input resistance,  $r_i$ . The impact on the final voltage gain is similar as demonstrated by the similitude of the voltage gain expressions reported in Equations (79) and (27), even if the voltage gain,  $A_v$ , of the proposed charge buffer results the double with respect to the telescopic Cascode OTA.

In both cases, the power consumption is determined by the settling requirements, i.e., both the time constants  $\tau_p$  and  $\tau_{p1}$  for the closed-loop and the proposed open-loop switched-capacitor integrator, respectively. The time constant,  $\tau_p$ , depends on  $1/g_{m1}$ . In this case, the only possibility to increase  $g_{m1}$  is to increase the bias current  $I_B$  of the telescopic Cascode OTA, since the input transistor overdrive is bound to bias constraints. For the proposed integrator, the time constant  $\tau_{p1}$  is proportional to  $r_i$ . However, in the last case, as the boost on the input transistor transconductance lowers the input resistance,  $r_i$ , a significant power saving is obtained.

#### 3.6. Slew-Rate Analysis of the Proposed Charge Buffer

According to Equation (56), the maximum rate of variation of the output voltage, i.e., the slew-rate, is obtained at the initial instant, t = 0 s:

$$SR = \frac{dv_o(t)}{dt} \bigg|_{max} = \frac{C_1}{C_2} \cdot \frac{1}{1 - \frac{C_1}{A_v \cdot C_2}} \cdot V_{SRi,max} \cdot \left(\frac{1}{\tau_{p1}} - \frac{1}{\tau_{p2}}\right) \cong \frac{V_{SRo,max}}{\tau_{p1}}$$
(80)

where:

$$V_{SRo,max} = \frac{C_1}{C_2} \cdot \frac{1}{1 - \frac{C_1}{A_v C_2}} \cdot V_{SRi,max} \cong \frac{C_1}{C_2} \cdot V_{SRi,max}$$
(81)

The last approximation in Equation (81) is valid assuming  $\tau_{p1} \ll \tau_{p2}$ .

The slew-rate depends on the bias current  $I_B$  and the output capacitance  $C_2$ , i.e.:

$$SR = \frac{I_B}{C_2} \tag{82}$$

where  $I_B$  is the bias current of each branches composing the charge buffer drawn in Figure 9.

Combining Equations (80) and (82) and considering the expression of  $\tau_{p1}$  and  $r_i$  reported in Equations (57) and (78), respectively, we derive:

$$V_{SRo,max} = \frac{I_B}{C_2} \cdot \tau_{p1} = \frac{C_1}{C_2} \cdot \frac{V_{ov1} \cdot V_{ov2}}{4 \cdot V_{A3}}$$
(83)

where  $V_{ov1}$  and  $V_{ov2}$  are the overdrive voltage of  $M_1$  and  $M_2$  transistors, respectively, and  $V_{A3}$  is the early voltage of  $M_3$  transistor.

Combining Equations (81) and (84), the value of  $V_{SRi,max}$  is obtained:

$$V_{SRi,max} = \frac{V_{ov1} \cdot V_{ov2}}{4 \cdot V_{A3}} \frac{1}{1 - \frac{C_1}{A_v \cdot C_2}} \cong \frac{V_{ov1} \cdot V_{ov2}}{4 \cdot V_{A3}}$$
(84)

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The output voltage range where the charge buffer operates in the linear regime,  $V_{SRo,max}$ , has been reduced by a factor equal to  $\frac{4 \cdot V_{A3}}{V_{ov2}}$  concerning the traditional closed-loop switched-capacitor integrator with the OTA.

Due to its differential structure, the charge buffer starts slewing as  $V_i > 2 \cdot V_{SRi,max}$ . If a slewing period is considered, the differential output voltage,  $v_{od}(t)$ , can be calculated as follows:

$$\begin{cases} v_{od}(t) = -2 \cdot \frac{V_{SRo,max}}{\tau_{p1}} \cdot t & \text{for } 0 < t < \tau_{s} \\ v_{od}(t) = \left( -\frac{C_{1}}{C_{2}} \cdot \frac{1}{1 - \frac{C_{1}}{A_{v} \cdot C_{2}}} \cdot V_{i} + 2 \cdot V_{SRo,max} \right) \left( 1 - \frac{t - \tau_{s}}{\tau_{p2}} \right) - 2 \cdot V_{SRo,max} \cdot \left( 1 - \frac{t - \tau_{s}}{\tau_{p2}} - e^{-\frac{t - \tau_{s}}{\tau_{p1}}} \right) \text{for } t > \tau_{s} \end{cases}$$
(85)

where  $\tau_s$  is the duration of the slewing period. The charge buffer slews until the output differential voltage,  $v_{od}(t)$ , is less than  $2 \cdot V_{SRo,max}$  concerning the final value in steady-state, neglecting the losses due to the output resistance (i.e.,  $\tau_{p2} \rightarrow \infty$ ):

$$-2 \cdot \frac{V_{SRo,max}}{\tau_{p1}} \cdot \tau_s = -\frac{C_1}{C_2} \cdot \frac{1}{1 - \frac{C_1}{A_v \cdot C_2}} \cdot V_i + 2 \cdot V_{SRo,max} \cong -\frac{C_1}{C_2} \cdot V_i + 2 \cdot V_{SRo,max}$$
(86)

From the combination of the last equation and Equation (83), the expression of  $\tau_s$  is derived:

$$\tau_s = \tau_{p1} \cdot \left( \frac{C_1}{C_2} \cdot \frac{V_i}{2 \cdot V_{SRo,max}} - 1 \right) = \tau_{p1} \cdot \left( \frac{V_i}{2 \cdot V_{SRi,max}} - 1 \right)$$
(87)

#### 3.7. SNR Analysis of the Proposed Open-Loop Switched-Capacitor Integrator

By focusing the analysis on a single branch,  $V_{0+}$  must satisfy the following inequation to guarantee that  $M_4$  transistors operate in saturation region:

$$V_{o+} > V_{DS,sat4} + V_{S4} = V_{ov} + V_{S4}$$
(88)

where  $V_{S4}$  and  $V_{DS,sat4}$  are the source and the saturation voltages of  $M_4$  transistor, respectively. It is assumed that  $V_{ds,sat4}$  is equal to  $V_{ov}$ . The bias voltage  $V_{b5}$  was chosen to make  $M_5$  transistor operating in saturation, i.e.,

$$V_{ds5} = V_{S4} > V_{DS,sat5} = V_{ov}$$
(89)

where  $V_{DS5}$ , and  $V_{DS,sat5}$  are the drain-source, and the saturation voltages of  $M_4$  transistor, respectively. In this case, it is assumed that  $V_{ds,sat1}$  is equal to  $V_{ov}$ .  $V_{S1}$  is derived from the  $V_{b5}$  bias voltage, by dropping the gate-drain voltage of the  $M_4$  transistors,  $V_{GS4}$ , i.e.:

$$V_{S4} = V_{b1} - V_{GS4} = V_{b1} - V_{TH} - V_{ov}$$
<sup>(90)</sup>

 $V_{b1}$  can be designed to make  $V_{S4}$ , and, hence,  $V_{DS5}$  equal to  $V_{DS5,sat}$ , i.e.,  $V_{ov}$ . If so, from Equation (88) we derive the minimum output voltage,  $V_{o+,min}$ :

$$V_{o+} > V_{ov} + V_{DS5,sat} = 2 \cdot V_{ov} = V_{o+,min}$$
(91)

As the output voltage starts swinging from the common-mode voltage,  $V_{cm}$ , down to  $V_{o,min}$ , it is possible to calculate the maximum output voltage swing,  $V_{swing}$ :

$$V_{swing} = 2 \cdot (V_{cm} - V_{o+,min}) = 2 \cdot \left(\frac{V_{dd}}{2} - 2 \cdot V_{ov}\right) = V_{dd} - 4 \cdot V_{ov}$$
(92)

where the 2 factor is due to the differential architecture. It is assumed that  $V_{cm}$  is equal to half  $V_{dd}$ .

Assuming that the thermal noise due to the switches around  $C_1$ ,  $2 \cdot \frac{KT}{C_1}$  is dominant, from Equation (92), the signal to noise ratio of the overall open loop switched capacitor integrator,  $SNR_{OL}$ , is calculated as follows:

$$SNR_{OL} = \frac{1}{2} \cdot \frac{V_{swing}^2}{\overline{v_{n,o}^2}} = \frac{1}{2} \cdot \frac{(V_{dd} - 4 \cdot V_{ov})^2}{2 \cdot \frac{K \cdot T}{C_1} \cdot \left(\frac{C_1}{C_2}\right)^2} = \frac{(V_{dd} - 4 \cdot V_{ov})^2 \cdot C_2^2}{4 \cdot K \cdot T \cdot C_1}$$
(93)

where  $\overline{v_{n,o}^2}$  is the total output noise, which is given by the thermal noise contribution due to the  $C_1$  switched-capacitor multiplied by the square of the integrator gain  $\left(\frac{C_1}{C_2}\right)^2$ , and the  $\frac{1}{2}$  factor takes into account that the input signal is a sinusoid.

The resulting  $SNR_{OL}$  is slightly higher than the  $SNR_{CL}$  calculated by Equation (43). The output noise is about the same since the noise contribution of  $C_1$  is assumed dominant. However, assuming  $V_{TH} = 0.275$  V and  $V_{dd} = 0.95$  V as for the finFET technology and  $V_{ov} = 0.1$  V, due to bias constraint as defined by Equation (43), the output voltage swing for the proposed switched-capacitor integrator is higher.

#### 3.8. Power Consumption Requirement of the Proposed Charge Buffer

The minimum power consumption,  $P_{w,min}$ , is given by the product of the supply voltage  $V_{dd}$ , by the minimum total bias current  $I_{BTOT,min}$ :

$$P_{w,min} = V_{dd} \cdot I_{BTOT,min} \cdot 4 \cdot \left(1 + \frac{H}{2}\right) \cdot V_{dd} \cdot I_{B,min}$$
(94)

where  $I_{B,min}$  is the minimum  $I_B$  bias current. The power requirement is calculated according to the settling time requirement. In practice, the minimum bias current  $I_{B,min}$  is derived assuming that the  $\varepsilon_{\tau p1}$  error must be less than the required accuracy  $\xi$ , i.e.:

$$\varepsilon_{\tau p1} < \xi$$
 (95)

As  $V_i < 2 \cdot V_{SRi,max}$ , the charge buffer is in the linear regime, where the expression of  $I_{B,min}$  is derived from Equation (62):

$$I_{B,min} = \frac{2 \cdot C_1 \cdot V_{SRi,max}}{T_{CLK}} \cdot ln \left(\frac{C_1}{C_2} \cdot \frac{V_i}{\xi}\right)$$
(96)

Combining Equations (94) and (96), the minimum required power consumption,  $P_{w,min}$ , is calculated as follows:

$$P_{w,min} = \frac{8 \cdot V_{dd} \cdot \left(1 + \frac{H}{2}\right) \cdot C_1 \cdot V_{SRi,max}}{T_{CLK}} \cdot ln\left(\frac{C_1}{C_2} \cdot \frac{V_i}{\xi}\right)$$
(97)

As  $V_i > 2 \cdot V_{SRi,max}$ , the charge buffer starts slewing. Considering the expression of the differential output voltage  $v_{od}(t)$ , including the slewing period reported in Equation (85), the calculation of the error due to  $\tau_{p1}$ ,  $\varepsilon_{\tau p1}$ , is updated as follows:

$$\varepsilon_{\tau p1} = \begin{vmatrix} v_o \left( \frac{T_{CLK}}{2} \right) \middle|_{\substack{\tau_{p1} \to 0 \\ \tau_{p2} \to \infty}} - v_o \left( \frac{T_{CLK}}{2} \right) \middle|_{\substack{\tau_{p2} \to \infty}} \end{vmatrix} = 2 \cdot V_{SRo,max} \cdot e^{-\frac{T_{CLK} - \tau_s}{\tau_{p1}}}$$
(98)

Considering  $\varepsilon_{\tau p1}$  as reported in the previous equation, the constraint on  $\tau_{p1}$  is derived from Equation (95):

$$\pi_{p1} < \frac{T_{CLK}}{2\left(ln\left(\frac{2\cdot V_{SRo,max}}{\xi}\right) + \frac{V_i}{2\cdot V_{SRi,max}} - 1\right)}$$
(99)

Looking at  $\tau_{p1}$  and  $r_i$  in Equations (57) and (78), respectively, the minimum bias current that satisfies Equation (99),  $I_{B,min}$  is calculated as follows:

$$I_{B,min} = \frac{2 \cdot C_1 \cdot V_{SRi,max}}{T_{CLK}} \cdot \left( ln \left( \frac{2 \cdot V_{SRo,max}}{\xi} \right) + \frac{V_i}{2 \cdot V_{SRi,max}} - 1 \right)$$
(100)

Combining Equations (97) and (100), the minimum required power consumption is calculated as follows:

$$P_{w,min} = \frac{8 \cdot V_{dd} \cdot C_1 \cdot \left(1 + \frac{H}{2}\right) \cdot V_{SRi,max}}{T_{CLK}} \cdot \left(ln\left(\frac{2 \cdot V_{SRo,max}}{\xi}\right) + \frac{V_i}{2 \cdot V_{SRi,max}} - 1\right)$$
(101)

Figure 10 shows the power consumption of the proposed switched-capacitor integrator and the closed-loop switched-capacitor integrator plotted as a function of  $V_i$ .

The two curves in Figure 10 are obtained plotting the Equations (97) and (101) for the proposed design, and Equations (46) and (51) for the closed-loop switched-capacitor integrator. The common design parameters are reported in Table 1.

**Design Parameter** Value  $V_{ov}$ 0.1 V  $V_{ov2}$ 0.2 V  $V_{dd}$ 0.95 V  $V_i$ 31.25 mV ξ (accuracy)  $1 \,\mathrm{mV}$  $T_{CLK}$ 7 ns 1.25 pF  $C_1$  $C_2$ 312.5 fF  $C_{1}/C_{2}$ 4 27 fF  $C_{par1}$ 1 V  $V_{A3}$ 18 V  $V_{A6}$ ×10<sup>-4</sup> 4 3.5 closed loop integrator with OTA 3 open loop integrator with charge buffer (M) 2.5 nim<sup>°</sup> 2 d 1.5 linear regime slew-rate regime 1 0.5 0 0 0.05 0.1 0.2 0.25 0.15 Vi (V)

Table 1. Design parameters of the switched capacitor integrator.

Figure 10. Minimum power consumption for the closed and the open-loop switched-capacitor integrators.

The transistors overdrives have been defined according to the constraints derived from Equations (25), (74), and (77). The values of  $C_{par1}$ ,  $V_{A3}$ , and  $V_{A6}$  are estimated from the simulation results. The *H* factor was set to 2 for the proposed design.

The minimum power required by the closed-loop switched-capacitor integrator is higher than the proposed open loop integrator for an input signal up to 140 mV large. For  $V_i$  = 31.25 mV, the proposed circuit requires a minimum power of 76  $\mu$ W, while the closed-loop switched-capacitor integrator requires about 173  $\mu$ W, i.e., more than the double.

# 3.9. Small Signal Analysis of the Charge Buffer Considering the Parasitic Capacitance C<sub>par1</sub>

The small-signal equivalent circuit shown in Figure 7 is a first-order approximation of the small-signal behavior of the proposed transistor-level open-loop switched-capacitor integrator. Considering also the  $C_{par1}$  as a parasitic capacitance shown in Figure 9, a more accurate transfer function is obtained:

$$\frac{v_o}{v_s} = -\frac{s \cdot C_1 \cdot \left(1 + \frac{s \cdot C_{par1}}{g_{m2}}\right)}{1 + s \cdot \left(\frac{C_{par1}}{g_{m2}} + \frac{C_1}{g_{m1} \cdot g_{m2} \cdot r_{ds3}}\right) + s^2 \cdot \frac{C_1 \cdot C_{par1}}{g_{m1} \cdot g_{m2}}}{\frac{1}{g_{m1} \cdot g_{m2}}} \cdot \frac{r_o}{1 + s \cdot r_o \cdot C_2}$$
(102)

where  $hr_{ds3}$  is the output resistances of  $M_3$  transistor. The parasitic capacitance,  $C_{par1}$ , mainly depends on the gate capacitances of  $M_2$  and  $M_6$  transistors. Therefore, it can be approximated as follows:

$$C_{par1} \cong \frac{2}{3} \cdot W_2 \cdot L_2 \cdot C_{ox} + \frac{2}{3} \cdot W_6 \cdot L_6 \cdot C_{ox} = \frac{4}{3} \cdot W_2 \cdot L_2 \cdot C_{ox}$$
(103)

where  $W_2$  and  $L_2$ , and  $W_6$  and  $L_6$ , are the width and the length of  $M_2$  and  $M_6$  transistors.

Concerning the transfer function reported in Equation (55), the transfer function in Equation (84) includes a further zero,  $z_1$ :

$$z_1 = -\frac{g_{m2}}{C_{par1}} \tag{104}$$

This zero is considered to be at a very high frequency and it does not produce significant effects on the step response of the proposed circuit.

Moreover, two complex poles appear in the transfer function. Their frequency,  $\omega_o$ , and quality factor, Q, are calculated as follows:

$$Q = \frac{\omega_0 = \sqrt{\frac{g_{m1} \cdot g_{m2}}{C_1 \cdot C_{par1}}} = 2 \cdot I_B \cdot \sqrt{\frac{H+1}{V_{ov1}V_{ov2}C_1C_{par1}}} \text{ and} \\ \frac{1}{\sqrt{\frac{g_{m1} \cdot C_{par1}}{g_{m2} \cdot C_1}} + \sqrt{\frac{C_1}{r_{ds3}^2 \cdot g_{m1} \cdot g_{m2} \cdot C_{par1}}}} = \frac{1}{(\sqrt{H+1}) \cdot \left(\sqrt{\frac{V_{ov2} \cdot C_{par1}}{V_{ov1} \cdot C_1}} + \sqrt{\frac{V_{ov1} \cdot V_{ov2} \cdot C_1}{4 \cdot V_{A3}^2 \cdot C_{par1}}}\right)}$$
(105)

A high *Q* factor determines a large overshoot, *OS*, on the step response of the proposed circuit, and wide oscillations, which can have a severe impact on the accuracy of the output voltage. Otherwise, as the circuit is excessively dumped, the step response slows significantly. The criterion here adopted is to limit the overshoot to the required accuracy,  $\xi$ , i.e.:

$$OS = \frac{C_1}{C_2} \cdot V_i \cdot e^{\frac{-\frac{\pi}{2Q}}{\sqrt{1 - \frac{1}{4Q^2}}}} = \xi$$
(106)

The previous equation is valid in linear regime; otherwise, in case of slewing of the charge buffer, the overshot is calculated as follows:

$$OS = V_{SRo,max} \cdot e^{\frac{-\frac{\pi}{2Q}}{\sqrt{1 - \frac{1}{4Q^2}}}} = \xi$$
(107)

For the proposed design, the last equation is satisfied for a Q value of about to 0.75. The Q factor can be reduced by operating on  $V_{ov2}$  and  $V_{ov1}$ , or, by acting on the H factor, which gives a further degree of freedom to the design.

The desired value of *Q* is reached by designing an *H* factor of 2.

### 4. Simulation Results

A transistor-level design of the proposed switched-capacitor circuit was performed in finFET 16 nm CMOS technology. The design parameter reported in Table 1 were considered. The input signal,  $V_i$ , was assumed equal to 31.25 mV. The bias current,  $I_B$ , set to 10  $\mu$ A, corresponds to the minimum value,  $I_{B,min}$ , as predicted by Equation (100). The *H* factor was set to 2 as derived from Equation (107). The minimum power consumption of the core circuit was 76  $\mu$ A, as predicted by Equation (83).

According to Equation (65), the required voltage gain is 56 dB, while a voltage gain of 71 dB results from simulations. Similarly, the required output resistance obtained from Equation (70) was 1.4 M $\Omega$ , while the value obtained through simulations was 1.85 M $\Omega$ . Therefore, we can conclude that the voltage gain and the output resistance requirements were largely satisfied.

Figure 11 shows the response of the circuit to an input step of 31.25 mV for the theoretical model and simulations. The two curves are very close, proving the validity of the proposed circuit model. Based on the design parameters, the expected error on the output voltage at  $T_{CLK}/2$  was 1 mV. This results from both the model prediction and the simulations.



Figure 11. Simulated and predicted step response of the proposed open-loop switched-capacitor integrator.

The simulation results show a slightly marked overshot due to the complex poles generated by the internal loop including  $M_1$  and  $M_2$  transistors, as predicted in paragraph 3.9. However, the first-order model gives a valid approximation of the circuit behavior especially in the steady-state regime.

Table 2 summarizes the required values of the design parameters and their values obtained through simulations.

Table 2. Required and simulated design parameters for the open-loop switched-capacitor integrator.

Design Parameter	Required Value	Simulated Value
$A_v$	>56 dB	71 dB
r <sub>o</sub>	>1.4 MΩ	1.85 MΩ
I <sub>B,min</sub>	10 µA	10 µA
ξ (accuracy)	1 mV	1 mV

Table 3 reports the performance summary of the proposed switched-capacitor integrator and compares it to the state-of-the-art approach. The following figure of merit (*FoM*) is introduced for a fast comparison

$$FoM = \frac{SNR}{\frac{Pw}{N} \cdot \frac{f_{CLK}}{2 \cdot OSR}}$$
(108)

where *N* is the number of poles of the switched-capacitor filter under consideration,  $P_w$  is its power,  $f_{CLK}$  is the clock frequency and *OSR* is the oversampling ratio, i.e., the ratio between half clock frequency and the maximum signal bandwidth.

Parameter	This work	[13]	[14]
Supply	0.95 V	1.8 V	1.2 V
Power	76 μW	4.3 mW	8.4 mW
Technology	16 nm FinFET	180 nm	65 nm
Number of poles	1	4	12
f <sub>CLK</sub>	143 MHz	300 MHz	430 MHz
OSR	1.57	11.3	9.23
SNR	61.5 dB	74.9 dB	45 dB
FoM	179.3 dB	175.8 dB	150.6 dB

Table 3. Performance summary and state-of-the-art comparison.

As can be seen in Table 3, the proposed work is well compared to the state of the art in terms of FoM.

# 5. Conclusions

An architecture of a switched-capacitor integrator including a charge buffer operating in open-loop have been proposed and designed in finFET 16 nm technology. As for the switched capacitor filters, the gain of the proposed integrator is given by the capacitor ratio, guarantying desensitization concerning the PVT variations. Furthermore, the proposed circuit is more suitable for low voltage supplies. Moreover, the analytical study demonstrated that the proposed integrator is more efficient than the traditional closed-loop switched-capacitor integrator for input signal amplitude less than 140 mV. The proposed switched-capacitor integrator results were more than twice the efficiency when compared to the traditional closed-loop switched-capacitor filter, as it consumes 76  $\mu$ W from the 0.95 V supply, assuming an input voltage of 31.25 mV and a clock period of 7 ns. The proposed work results were satisfactory when compared to the state-of-the-art in terms of the figure of merit.

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