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A Low-Power Column-Parallel Gain-Adaptive Single-Slope ADC for CMOS Image Sensors

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Abstract: A low-power column-parallel gain-adaptive single-slope analog-to-digital converter (ADC) for CMOS image sensors is proposed. The gain-adaptive function is realized with the proposed switched-capacitor based gain control structure in which only minor changes from the traditional single-slope ADC are required. A switched-capacitor controlled dynamic bias comparator and a flip-reduced up/down double-data-rate (DDR) counter are proposed to reduce the power consumption of the column circuits. A 12-bit current steering digital-to-analog converter (DAC) with a two-dimensional gradient error tolerant switching scheme is adopted in the ramp generator to improve the linearity of the ADC. The proposed techniques were experimentally verified in a prototype chip fabricated in the TSMC 180 nm CMOS process. A single-column ADC consumes a total power of 63.2 μ W and occupies an area of 4.48 μ m $\times$ 310 μ m. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC are $-0.43/+0.46$ least significant bit (LSB) and $-0.84/+1.95$ LSB. A 13-bit linear output is acquired in nonlinearity within 0.08% of the full scale after calibration.

Keywords: CMOS image sensor; single-slope ADC; double-data-rate (DDR) counter; low-power comparator; gain-adaptive

1. Introduction

CMOS image sensors (CISs) are widely used in mobile phones, surveillance security, autonomous driving, machine vision, and the Internet of Things. Figure 1 shows a CIS system including pixel array, control signal and clock generator, readout circuits, memory, and other modules. As illustrated in Figure 1, a typical 4T pixel includes a photodiode (PD), a transfer transistor (M_{TX}), a reset transistor (M_R), an amplifier transistor (M_{SF}), and a select transistor (M_S) [1].

Currently, the signal readout architecture with column-parallel analog-to-digital converters (ADCs) is often used in the CIS system. The column-parallel ADCs make it possible to read out image signals from the pixel array with less noise and higher bandwidth and to transfer the image data to outside at very high pixel rate with no degradation of signal quality [2]. The column-parallel ADC is an important part of the CIS readout circuits and a key element to affect the performance of CISs. As the resolution of CIS increases, the pitch of pixel decreases. The column-parallel ADC must be designed under very severe constraints because it must be embedded into the narrow column and arranged as an array of many elements [2].

The column-parallel single-slope ADC (SS-ADC) architecture is widely adopted for CIS because of its simplicity, low power consumption, and high linearity [3]. Figure 2a shows the single-slope ADCs in a CIS system consisting of a global ramp generator, comparators, and up/down counters. The ramp generator is

shared among all the columns. Only a comparator and counter are necessary in each column, so the area of column circuits is quite small. In CISs, the variation of the output from different pixels under the same illumination condition is referred to as fixed-pattern noise (FPN), which is mainly caused by the mismatch of in-pixel or column-level transistors, and the dark current generated inside the pixel [4]. To eliminate the FPN, the correlated double sampling (CDS) operation is adopted. As illustrated in Figure 2b, an entire A/D conversion period of CDS includes a P-phase comparison period during which a reset signal read from the pixel is compared with the ramp signal, and a D-phase comparison period during which a pixel signal read from the pixel is compared with the ramp signal [5]. Subtraction of the conversion results in two phases can eliminate the FPN, which is implemented by the up/down counter in this work.

Figure 1. Block diagram of a CIS system.

Figure 2. (a) block diagram of column-parallel SS-ADCs; (b) timing diagram of the CDS operation.

One of the main drawbacks of the SS-ADC is the long conversion time. The clock cycles per conversion is an exponential function of the ADC bit depth. In SS-ADCs, it is generally thought to be difficult to get both high speed and high A/D resolution because the A/D resolution is restricted by the number of clock cycles [6]. On the one hand, with the increasing demands of high-quality imaging, high-resolution ADCs are required. On the other hand, the analog-to-digital conversion time per row is only a few microseconds

in high resolution CISs. Thousands of SS-ADCs work simultaneously and the counting clock usually goes up to several GHz, which makes the power consumption quite high. In high resolution CISs, the power consumption of the SS-ADCs, which is over 40% of that of the entire CIS [7], has become a major problem. The trade-off between power consumption and conversion time has become a big challenge in the design of SS-ADC.

Recently, some methods to reduce the power consumption of the SS-ADC in CIS have been published. In Reference [8], a hold-and-go counter scheme with a global counter is proposed to realize CDS and reduce power consumption. However, the speed of the global counter is limited because of its large load. In Reference [9], a global 5-bit least significant bit counter is shared among every 248 columns and the power consumption of the counters is reduced. However, the refreshing of the memory cells in columns will lead to a large amount of power waste. In Reference [10], a passing window technique is used to save power in LSB memories and data bus driver, but the complexity and area of the column ADC will increase. A dynamic SS-ADC [11] based on a dynamic bias comparator and a two-step counter can achieve high energy efficiency but the fully dynamic circuits may cause more random noise and power supply variation.

In this paper, a low-power gain-adaptive SS-ADC is proposed to reduce the conversion time and power consumption of SS-ADC. The gain-adaptive function is realized with the proposed switched-capacitor based gain control structure. To reduce the power consumption, a switched-capacitor controlled dynamic bias comparator and a flip-reduced up/down double-data-rate (DDR) counter are proposed. In addition, a 12-bit current steering DAC with two-dimensional gradient error tolerant switching scheme is adopted in the ramp generator to improve the linearity of the ADC. With the 500 MHz counting clock and 2.2 μ s for the signal level in per conversion, a conventional SS-ADC can only achieve 10-bit A/D conversion, while the proposed ADC acquires 13-bit linear digital outputs based on the gain-adaptive function and DDR counter.

This article is organized as follows. Section 2 illustrates the concept of the proposed gain-adaptive SS-ADC. Section 3 presents the circuit configuration of the SS-ADC including the comparator, the counter, and the ramp generator. Section 4 describes the nonlinearity of the gain-adaptive SS-ADC and the calibration method. Section 5 shows the experimental results. Finally, conclusions are presented in Section 6.

2. Overall Architecture

2.1. Concept of Gain-Adaptive SS-ADC

The pixel response to light intensity is plotted in Figure 3 along with main noise sources of CIS. Temporal noise in CISs can be divided into two main categories. Most of the noise sources are basically independent of light intensity, such as thermal noise, $1/f$ noise, etc., which can be regarded as a “noise floor” and limit the dynamic range of the CIS [12]. In order to ensure that the quantization noise of the ADC does not deteriorate the performance of the system noise, the ADC is usually designed to make the quantization noise lower than the noise floor.

Figure 3. Pixel response to light intensity and main noise sources [12].

The other type of noise is photon shot noise, which is dependent on the signal level and can be expressed as follows:

$$n_{shot}(N_{sig}) = \sqrt{N_{sig}} \quad (1)$$

where N_{sig} is the signal level and $n_{shot}(N_{sig})$ is corresponding photon shot noise. N_{sig} and $n_{shot}(N_{sig})$ are both expressed in the number of electrons. With the increase of light intensity, photon shot noise becomes the dominant noise source of the system. In this situation, the quantization noise of the ADC is much lower than the photon shot noise, and the ADC actually has a better noise performance than is required. Therefore, in the situation of high light intensity, even if the quantization noise of the ADC is increased, it will not affect the overall noise performance of the system. The reason why the SS-ADC is slow is because its working principle is continuously integrating with the smallest quantization step in the entire input range. If the quantization step can be increased with the increase of light intensity, the clock cycle required can be greatly reduced, the speed of the SS-ADC can be effectively increased. Within a certain conversion time, the required counting clock frequency is reduced which will reduce the power consumption.

Based on the above analysis, multiple-ramp [12], nonlinear-slope [9,13,14], and gain-adaptive [7,15,16] techniques have been proposed to realize high A/D resolution in a short conversion time, which is shown in Figure 4. The multiple-ramp signal path occupies more area and the calibration of offset errors among different ramps is difficult. The nonlinear-slope functions usually produce significant nonlinearity, especially at the knee point. Conventional gain-adaptive techniques employ a programmable gain amplifier (PGA) in each column to change the analog gain according to the pixel output. However, the power consumption and area occupied of the column-parallel PGAs are large.

Figure 4. Block diagram of column-parallel ADCs. (a) conventional SS-ADC; (b) multiple-ramp ADC; (c) nonlinear-slope ADC; (d) gain adaptive ADC with a PGA.

To solve the problems, we proposed a low-power gain-adaptive SS-ADC with a switched-capacitor based gain control structure. The block diagram of the proposed gain-adaptive SS-ADC is shown in Figure 5. The gain-adaptive function is realized by adjusting the slope of the ramp signal in each column according to the signal level of the pixel. A high-gain (HG) ramp with a small slope is realized in the dark condition and a low-gain (LG) ramp with a large slope is realized in the bright condition. The slope adjustment is realized by the switched-capacitor based gain control structure. This approach only requires minor changes from a conventional single-slope ADC with small overhead of area by adding several switches and registers..

Figure 5. Block diagram of the proposed gain-adaptive SS-ADC.

2.2. Gain Control Structure

Figure 6 illustrates the switched-capacitor based gain control structure. In a conventional SS-ADC, the ramp signal V_{RAMP} and pixel output V_{PXD} are connected to the input of the comparator through two capacitors C_{IP} and C_{IN} of the same value. The capacitors allow the comparator to achieve the auto-zero operation to eliminate the offset voltage and determine the appropriate operating point. In the gain control structure, the capacitor C_{IN} between the pixel output node V_{PXD} and the negative input terminal of the comparator V_{IN} is set to $4C$, where C is the unit capacitance value. The capacitor C_{IP} between the ramp signal V_{RAMP} and the positive input terminal of the comparator V_{IP} is divided into three parts of 1:1:2.

The upper plates of the three capacitors (C_{IP0} , C_{IP1} and C_{IP2}) are connected to the V_{IP} node, and the lower plate of the capacitor C_{IP0} is connected to V_{RAMP} . The lower plates of C_{IP1} and C_{IP2} are connected to V_{RAMP} or ground controlled by the switches. $AG<1:0>$ and $AGB<1:0>$ are two sets of opposite control voltage to control the corresponding switches. The switches ($S0$ and $S1$) connected to the lower plate of the capacitor C_{IP0} are fixed and used for circuit matching. V_{RAMP} is an input ramp signal with a certain slope. By changing the connection of the capacitors between V_{RAMP} and V_{IP} nodes, the voltage relationship between V_{RAMP} and V_{IP} can be changed to adjust the slope of the ramp signal in V_{IP} node. The smaller the slope of the ramp, the higher the analog gain of the pixel.

The voltage relationship between V_{IP} and V_{RAMP} with different control voltages is shown in Figure 7. In Figure 7a, the control voltages are $AG<1:0> = 00$ and $AGB<1:0> = 11$, so the lower plates of the capacitors C_{IP1} and C_{IP2} are connected to V_{RAMP} . V_{IP} is consistent with V_{RAMP} , and the analog gain is 1, which is the low-gain (LG) scheme in this design. In Figure 7c, the control voltages are $AG<1:0> = 10$ and $AGB<1:0> = 01$, so the lower plate of capacitor C_{IP2} is connected to ground, and the lower plate of capacitor C_{IP1} is connected to V_{RAMP} . The relationship between V_{IP} and V_{RAMP} is

$$V_{IP} = V_{RAMP} \times \frac{C_{IP0} + C_{IP1}}{C_{IP}}. \quad (2)$$

Here, $C_{IP} = C_{IP0} + C_{IP1} + C_{IP2} = 4C$, so

$$V_{IP} = V_{RAMP} \times \frac{2C}{4C} = \frac{1}{2} V_{RAMP}, \quad (3)$$

and the analog gain is 2, which is the medium-gain (MG) scheme in this design. Similarly, the voltage relationship in Figure 7d can be obtained as follows:

$$V_{IP} = V_{RAMP} \times \frac{C_{IP0}}{C_{IP}} = V_{RAMP} \times \frac{C}{4C} = \frac{1}{4} V_{RAMP}. \quad (4)$$

The analog gain is 4, which is the high-gain (HG) scheme in this design. The gain schemes and corresponding control voltages are summarized in Table 1.

Figure 6. Switched-capacitor based gain control structure.

Table 1. Gain schemes and the control voltages.

Gain Scheme	Light Intensity	AG<1: 0>	AGB<1: 0>	Analog Gain
Low	High	00	11	$\times 1$
Medium	Medium	10	01	$\times 2$
High	Low	11	00	$\times 4$

Figure 7. The gain control structure with different control voltages. (a) $AG<1: 0> = 00$; (b) $AG<1: 0> = 01$; (c) $AG<1: 0> = 10$; (d) $AG<1: 0> = 11$.

Figure 8 shows the timing diagram of the proposed gain-adaptive SS-ADC in a horizontal scanning period. In (1), the pixel reset level is sampled for analog CDS with the same method in [17]. The comparator is reset and the comparator offset voltage is sampled during (2). The reset level is down-counted in the counter respectively in (3) with the high-gain scheme. After signal readout in (4), the pixel output voltage is compared with two threshold voltages V_{OM1} and V_{OM2} to estimate the voltage level. The control voltages are obtained by the comparison results of the pixel output voltage to the threshold voltages and stored in the flipflops. If V_{PXD} is darker than V_{OM1} , $AG<0>$ is equal to 1. If V_{PXD} is brighter than V_{OM1} , $AG<0>$ is equal to 0. If V_{PXD} is darker than V_{OM2} , $AG<1>$ is equal to 1. If V_{PXD} is brighter than V_{OM2} , $AG<1>$ is equal to 0. According to the control voltages obtained in (5), a gain-adaptive signal readout scheme is implemented in process (6). In dark condition, the high-gain (HG) scheme is employed as the blue line

in Figure 8. The low-gain (LG) scheme is employed in the bright condition as the red line in Figure 8. The black line in Figure 8 represents the medium-gain (MG) scheme.

Figure 8. Timing diagram of the proposed gain-adaptive SS-ADC.

3. Circuit Configuration

3.1. Comparator

In the conventional SS-ADC, as the input ramp signal changes continuously, a static comparator is usually adopted and always kept on, which leads to significant static power waste. If a lower current is supplied to the static comparator, the response of the comparator will slow down, causing a risk of the degradation of the A/D conversion performance [5]. In fact, a high supply current only needs to be maintained during the comparison period to ensure the speed of the comparator, while the current can be lower during the non-comparison period, which only changes the common static operating point of the comparator without affecting the comparison. For the above reasons, a switched capacitor controlled dynamic bias comparator is proposed to reduce the power consumption. As shown in Figure 9, the proposed comparator consists of first amplification stage (Amp1), second amplification stage (Amp2), and output stage. The gate of the tail current transistor of Amp1 is biased by a switched capacitor.

Figure 9. Schematic diagram of the proposed comparator.

Figure 10 shows the timing diagram of the control signal of the comparator during an entire A/D conversion period, which includes an autozero period, comparison periods, and hold periods. For simplicity, the gain-adaptive function is not shown in the diagram. The working process of the comparator is explained as follows:

- During the autozero period, switches S1 and S6 are closed and S5 is open. The lower plate of the capacitor C_{B1} is connected to the ground and the gate voltage of the transistor M6 (V_G) is equal to V_B .
- During the comparison period, switches S1 and S6 are open and S5 is closed. The lower plate of the capacitor C_{B1} is connected to the boost voltage V_{BST} and $V_G = V_B + V_{BST}$.
- During the hold period, the switches S1 and S5 are open and S6 is closed, and V_G is equal to V_B .

During the entire A/D conversion, the average current of Amp1 is

$$I_{ave} = \frac{I_1(T_{AZ} + T_H) + I_2 T_{CMP}}{T_{AD}}, \quad (5)$$

where I_1 is the current of Amp1 during the autozero and hold periods, I_2 is the current of Amp1 during the comparison period, T_{AD} is the time of an A/D conversion period, T_{AZ} is the time of an autozero period, T_H is the total time of hold periods, and T_{CMP} is the total time of comparison periods. While I_1 is lower than I_2 , the average current I_{ave} is lower than the static current in the conventional structure, which is equal to I_2 .

Figure 10. Timing diagram of the control signal of the comparator.

As shown in Figure 10, switch S1 is only closed for a short time during the autozero period, which might prevent noise coupling between different columns during comparison periods. Switch S3 is closed once before each comparison to set the output of Amp1 (V_1) high to ensure the same initial state for comparison. The transistor M8 is used to clamp the output voltage of Amp2 (V_2) to prevent the transistor M10 operating in the triode region.

3.2. Counter

A double-data-rate counter [18], also called double-edge-counting (DEC) counter, is capable of performing counting at both edges of the clock. In a traditional up/down DDR counter, a latch is used so that the lowest bit circuit can operate at the same frequency as the input clock. However, a latch and an inversion selector in the LSB circuit perform high-speed operation in synchronization with a high frequency input clock and consume a large amount of current [19].

To reduce the power consumption, the lowest bit circuit is redesigned in the proposed counter as it consumes the most power. Figure 11 shows the block diagram of the proposed flip-reduced up/down DDR counter [20]. In the proposed structure, the latch in the LSB circuit is replaced by two D flip-flops. The outputs of the two D flip-flops (QX and QN) change only when the output of comparator (CMP) changes. The lowest bit circuit can count at both edges of the input clock, but only records the parity information of the lowest bit. The proposed counter counts with twice the frequency as an input clock, but the LSB circuit (DDR Cell) flips much fewer times than conventional counters in both down and up counting phases.

Figure 11. Block diagram of the flip-reduced up/down DDR counter.

Figure 12 shows the timing diagram of the proposed counter with two examples to explain the counting process of the counter. A 3-bit structure implementation is taken as an example for simplicity. The CDS operation is realized by reversing the P-phase counting code REF, which is controlled by the control signals HLD and XRV. The clock signal for D-phase counting is chosen by a selector in LSB circuit based on the LSB counting result D[0] in P-phase counting to ensure the subtraction between SIG and REF is correct. D[0] records the parity information of DATA and does not need to change with the clock all the time.

Figure 12. Timing diagram of the counter with two examples.

The DDR counter needs to be modified to realize CDS operation with the gain-adaptive function. The counting process of the signal voltage is shown in Figure 13. Since the reference voltage is converted in HG scheme, if the signal voltage is also converted in HG mode, the counter will work directly without adjustment. If the signal voltage is converted in MG scheme in which the quantization step is 2 LSB, the

DDR Cell is directly input to Counter Cell [2], and Counter Cell [1] is bypassed. In order to ensure correct counting, the reference counting result of Counter Cell [1] should be written into the DDR Cell before the conversion of the signal voltage. Similarly, the quantization step in LG scheme is 4 LSB and the DDR Cell is directly input to Counter Cell [3]. Counter Cell [1] and Counter Cell [2] are bypassed. The reference counting result of Counter Cell [2] should be written into the DDR Cell before the conversion of the signal voltage. The modified DDR Cell is shown in Figure 14. A XOR gate is used to decide whether to change the value of D[0] for signal level conversion. A latch is used to hold the value of D[0] of the reference level conversion.

Figure 13. Counting process of the DDR counter in (a) HG; (b) MG; (c) LG scheme.

Figure 14. Modified DDR Cell for gain-adaptive function.

3.3. Ramp Generator

A 12-bit current steering DAC with 6+6 architecture and two-dimensional gradient error tolerant switching scheme [21] is adopted as the ramp generator to improve the linearity of the ADC. The block diagram of the ramp generator is shown in Figure 15. When the most significant bit (MSB) unary source is divided into 16 elements located in 16 separated regions of the array, the linear gradient errors and quadratic errors can be averaged and eliminated effectively. Figure 16 shows the scheme for 6-bit unary

decoding of the MSB current source. The 6-bit unary decoding array is generated from a basic 4-bit decoding array [22]. Each unary source has exactly one element in each 8×8 region.

Figure 15. Block diagram of the ramp generator.

Figure 16. Diagram of the scheme for 6-bit unary decoding.

A common noise canceling section [23] is adopted to reduce the effect of power supply noise on the ramp generator. The differential output of DAC is input to the common noise canceling section. The power supply noise is regarded as common noise which can be canceled through a differential operation between the differential ramp signals. The output of the ramp generator is

$$V_{OUT} = 2 \frac{C_S}{C_F} V_{DAC} \quad (6)$$

where V_{DAC} is the single output of the DAC.

3.4. Group Delay Scheme

The column ADCs are divided into groups as shown in Figure 17. The clock and control signals are delayed for every four column ADCs to prevent gates in different groups, especially the counters, from flipping at the same time, which would cause transient large current from source. The clock signals for adjacent groups are in the opposite phase to further suppress power source variations. Figure 18 shows the diagram of supply current of counters during an A/D conversion period with/without group delay

scheme. The simulation result of the maximum value of the transient current of 1000 counters is also shown in the diagram. Two horizontal bit lines are grouped by parity for every bit so that the frequency of the readout clock can be reduced to half and the power consumption in the readout phase can also be lower.

Figure 17. Diagram of the group delay scheme.

Figure 18. Simulation result of the supply current.

4. Nonlinearity and Calibration

The gain-adaptive function realized by adjusting the slope of the ramp to change the analog gain is relatively simple, but the quantization result usually has nonlinearity and needs calibration. One of the main reasons of the nonlinearity is that the comparator is not an ideal model. When the ramp signal reaches the pixel output voltage, the comparator output does not immediately toggle, and there will be a delay time. Figure 19 is a timing diagram of the comparator comparison process, in which the total counting time of the counter t_c is defined as

$$t_c = t_p + t_d. \quad (7)$$

Here, t_p is the time from the beginning of the ramp to when the ramp voltage is the same as the pixel voltage. For a certain pixel voltage, t_p is inversely proportional to the slope of the ramp. t_d is the time from when the ramp voltage is same as the pixel voltage to when the comparator output toggles, defined as the toggle delay of the comparator.

Figure 19. Timing diagram of the comparator comparison process.

Since t_d is not inversely proportional to the slope of the ramp s_r , for a certain pixel voltage, changing the slope of the ramp by a certain ratio will not completely inversely change the total counting time by the same ratio. Figure 20 shows the simulation result of the total counting time of the SS-ADC with different slopes of the ramp signal under a certain input voltage. The relationship between t_c and s_r is not completely inversely proportional, reflecting a kind of nonlinearity.

Figure 20. Simulation result of counting time with different slopes.

In addition, due to the non-idealities in the circuit, the slope of the ramp will change, resulting in gain errors. In the switched-capacitor structure, gain errors may come from the effects of charge injection and clock feedthrough of the switches, or the influence of the parasitic capacitance of each node on the charge distribution relationship. The gain error brought by the slope error of ramp signals is also an important source of the nonlinearity of the quantization result.

The quantization result with nonlinearities produced by the above two reasons is shown in Figure 21. The nonlinearity between the counting time and the slope of the ramp will produce a jump near the gain switching point, which can be regarded as an offset voltage. The slope mismatch will produce a gain error, which is reflected as the nonuniformity of slope between quantization lines of different gain schemes.

Figure 21. The quantization result with nonlinearities and calibration method.

The calibration method for the nonlinearity is also shown in Figure 21. Two predetermined voltages (V_0 and V_1) are converted in three gain schemes. $D_{0,HG}$ and $D_{1,HG}$ are quantization results in HG scheme. $D_{0,MG}$ and $D_{1,MG}$ are quantization results in the MG scheme. $D_{0,LG}$ and $D_{1,LG}$ are quantization results in LG scheme. The slopes with different gain schemes are:

$$S_{HG} = \frac{D_{1,HG} - D_{0,HG}}{V_1 - V_0} \quad (8)$$

$$S_{MG} = \frac{D_{1,MG} - D_{0,MG}}{V_1 - V_0} \quad (9)$$

$$S_{LG} = \frac{D_{1,LG} - D_{0,LG}}{V_1 - V_0} \quad (10)$$

The gain ratio of α is defined as

$$\alpha = \frac{S_{HG}}{S_{MG}} = \frac{D_{1,HG} - D_{0,HG}}{D_{1,MG} - D_{0,MG}} \quad (11)$$

The gain ratio of β is defined as

$$\beta = \frac{S_{HG}}{S_{LG}} = \frac{D_{1,HG} - D_{0,HG}}{D_{1,LG} - D_{0,LG}} \quad (12)$$

The calibration of gain errors is achieved by multiplying the MG and LG quantization results by the ratio α and β . The offset between the MG and HG lines is

$$\Delta_{MG} = \alpha D_{1,MG} - D_{1,HG} = \alpha D_{0,MG} - D_{0,HG}. \quad (13)$$

The offset between the LG and HG lines is

$$\Delta_{LG} = \beta D_{1,LG} - D_{1,HG} = \beta D_{0,LG} - D_{0,HG}. \quad (14)$$

For a MG quantization result D_{MG} , the calibration result is

$$\hat{D}_{MG} = \alpha D_{MG} - \Delta_{MG}. \quad (15)$$

For a LG quantization result D_{LG} , the calibration result is

$$\hat{D}_{LG} = \beta D_{LG} - \Delta_{LG}. \quad (16)$$

5. Experimental Results

The single-slope ADCs prototype is fabricated in a 180 nm standard CMOS process, and the microphotograph of the chip is shown in Figure 22. In order to focus on the characterization of the ADC design, only 100 columns of single-slope ADCs are implemented in this prototype. The control signals are generated on chip and the counting 500 MHz clock is generated externally and buffered on chip. The SS-ADC is implemented within a column pitch of 4.48 μm and a vertical length of 120 and 190 μm for the comparator and the counter, respectively.

Figure 22. Microphotograph of the ADC chip.

Figure 23a shows the FFT spectrum plot of the measured output for a 185 kHz sinusoidal input in the LG scheme. The signal-to-noise and distortion ratio (SNDR) is 65.85 dB, the spurious-free dynamic range (SFDR) is 82.84 dB, and the effective number of bits (ENOB) is 10.65 bits. As shown in Figure 23b, the measured DNL and INL in LG scheme are $-0.43/+0.46$ LSB and $-0.84/+1.95$ LSB, respectively.

Figure 23. (a) spectrum plot; (b) INL and DNL of the measured output in the LG scheme.

Figure 24 shows the power breakdown of the SS-ADC in one column with a total power of 63.2 μW . The single-column power of the global ramp generator is calculated by dividing its power by the number

of columns. Figure 25 illustrates the relationship between the power consumption of the proposed comparator and the boost voltage V_{BST} . With the proposed dynamic bias technique, 32% of the power consumption of the comparator can be saved when V_{BST} is chosen as 0.6V. As shown in Figure 26, 54% of the power consumption of the counter is saved with the proposed DDR structure compared with the conventional ripple counter and 20% of the power consumption is saved compared with a previous DDR counter [19]. According to the post layout simulation, the ramp generator can drive more columns, and therefore the power consumption of one-column SS-ADC can be lower in a higher resolution design with the counting clock of same frequency.

Figure 27 shows the linearity of the gain-adaptive SS-ADC. With the 500 MHz counting clock and 2.2 μ s for the signal level in per conversion, a conventional SS-ADC can only achieve 10-bit A/D conversion, while the proposed ADC achieves 13-bit linear digital outputs based on the gain-adaptive function and DDR counter. The nonlinearity of the proposed ADC is only 0.08% of the full scale after calibration.

Figure 24. Power breakdown of the SS-ADC in one column.

Figure 25. Power consumption of the proposed comparator with different boost voltages.

Table 2 summarizes the performance of the implemented ADC compared with prior works. This work achieves low power consumption and high A/D resolution. The power efficiencies were compared using figure of merits (FoMs) calculated as follows [3]:

$$FoM_1 = \frac{Power \times T_{conv}}{2^{Nbit}} [fJ/convstep], \quad (17)$$

$$FoM_2 = \frac{Power \times T_{conv} \times Area}{2^{Nbit}} [pJ \cdot \mu m^2/convstep], \quad (18)$$

where T_{conv} is time of an entire A/D conversion period. The proposed SS-ADC achieved the FoM_1 of 20.1 fJ/convstep and the FoM_2 of 27.9 pJ $\cdot\mu$ m²/convstep.

Figure 26. Power consumption of the proposed DDR counter compared with conventional structures.

Figure 27. Linearity of the gain-adaptive SS-ADC (a) without (b) with calibration.

Table 2. Performance comparison of the related works.

	[10]	[24]	[25]	[26]	[27]	This Work
Process [nm]	40	65	90	130	130	180
Architecture	SS	Cyclic/SAR	SAR/SS	SS	$\Delta\Sigma$	SS
Resolution [bit]	12	12	12	12	12	13
Conv. Time [μ s]	2.7	0.92	2.7	6.4	2.3	2.6
Col. Pitch [μ m]	5.4	4.4	2.24	11.2	4.5	4.48
Col. Height [μ m]	610	920	998	590	600	310
Col. Power [μ W]	66.8	120	56	90	55	63.2
DNL[LSB]	-0.28/+0.32	-0.88/+0.82	-0.45/+0.84	-0.49/+1.34	-0.55/+0.63	-0.43/+0.46
INL [LSB]	-0.94/+4.21	-11.75/+1.04	-1.5/+0.74	-2.47/+2.44	-0.8/+3.7	-0.84/+1.95
FoM_1	44.0	27.0	36.9	140.6	30.9	20.1
FoM_2	145.0	109.1	82.5	929.3	83.4	27.9

6. Conclusions

A 63.2 μ W per-column gain-adaptive single-slope ADC for CMOS image sensors was designed and fabricated in a 180 nm CMOS process. With the proposed switched-capacitor controlled dynamic bias comparator and flip-reduced up/down DDR counter, total power consumption is reduced. With the proposed gain-adaptive function, the ADC achieves total 13-bit linear A/D resolution in nonlinearity within 0.08% of the full scale after calibration. The occupied area of one column ADC is 4.48 μ m $\times$ 310 μ m. The prototype ADC has a competitive FoMs performance with the proposed gain-adaptive structure and

low power techniques. The proposed techniques are suitable for low-power and high-resolution CMOS image sensors.

A limitation of this work is that the performance of the proposed ADC was independently tested without pixels. However, the proposed gain-adaptive SS-ADC has already been implemented in a 5-megapixel CIS chip, which has been taped out and is being manufactured in a 90 nm CIS process. The performance of the proposed techniques will be tested and verified in the CIS system.

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