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An Optimized Structure of Split-Gate Resurf Stepped Oxide UMOSFET

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Abstract: In this paper, a split-gate resurf stepped oxide with double floating electrodes (DFSGRSO) U-shape metal oxide semiconductor field-effect transistor (UMOSFET) is proposed. The floating electrodes are symmetrically distributed on both sides of the source electrode in the trench. The performance of the DFSGRSO UMOSFET with different size of floating electrodes is simulated and analyzed. The simulation results reveal that the floating electrodes can modulate the distribution of the electric field in the drift area, improving the performance of the device significantly. The breakdown voltage (BV) and figure of merit (FOM) of the DFSGRSO UMOSFET at optimal parameters are 23.6% and 53.1% higher than that of the conventional structure. In addition, the regulatory mechanism of the floating electrodes is analyzed. The electric field moves from the bottom of the trench to the middle of the drift area, which brings a new electric field peak. Therefore, the distribution of the electric field is more uniform for the DFSGRSO UMOSFET compared with the conventional structure.

Keywords: power UMOSFET; split gate; floating electrode; electric field modulation

1. Introduction

The power metal oxide semiconductor field-effect transistor (MOSFET) has been playing an important role in the electronic power industry with the development of society. In order to improve the performance of devices, some new structures have been proposed, such as the laterally-diffused MOSFET (LDMOSFET) [1–3], the vertical double-diffused MOSFET (VDMOFET) [3–6] and the U-shape MOSFET (UMOSFET) [6–9], and the on-state resistance (R_{SP}) of these devices is getting lower and lower. However, it was difficult to realize a very low R_{SP} due to the limit of one-dimensional silicon, until the super junction MOSFET (SJ-MOSFET) [10–14] was proposed. The R_{SP} is about 140 mΩ·cm^2–100 mΩ·cm^2 [3,5] for the previous structure, while the SJ-MOSFET achieves an R_{SP} of 10 mΩ·cm^2, and the next-generation devices are likely to be around 8 mΩ·cm^2 [11]. The SJ-MOSFET adopts the principle of charge-coupling, which could increase the doping concentration of the drift area, completely breaking the one-dimensional silicon limit and significantly improving the performance of the device. However, there are some problems in the actual process, mainly because of the doping interdiffusion. Therefore, the split-gate resurf stepped oxide (SGRSO) UMOSFET [14–19] has attracted the attention of researchers, as it also adopts the principle of charge-coupling and has a relatively simple preparation process compared with SJ-MOSFET. The conventional structure is shown in Figure 1a, whereby the electrode in the trench is connected to the source, which can enhance the depletion of drift area and increase the doping concentration of the epitaxial layer to reduce the R_{SP} of the device.

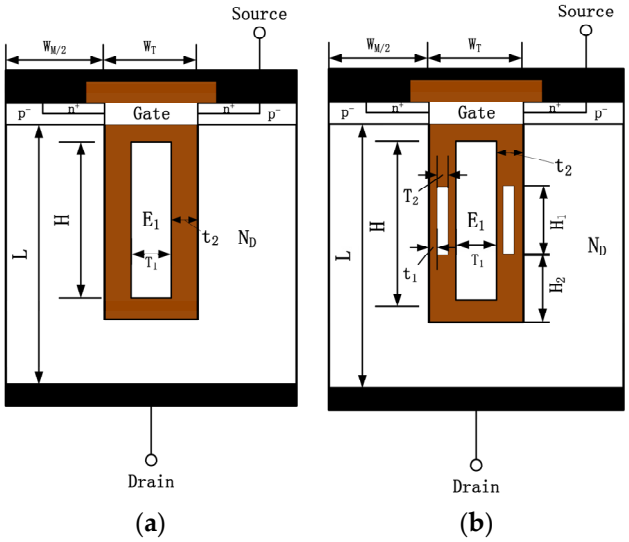

Figure 1. Schematic cross section of (**a**) SGRSO and (**b**) DFSGRSO UMOSFETs.

However, the electric field distribution of this structure is not very ideal compared with the SJ-MOSFET, especially for breakdown above 200 V [20]. In order to improve the distribution of electric field in the drift area, a series of measures has been put forward, for example, a split gate UMOSFET with P-pillar [21], subsection dielectric layer [22] and slope oxide layer [23], but it is unclear if the control of the slope side oxygen or P-pillar is feasible with the appropriate accuracy in the actual process and so on. Hence, an advanced SGRSO UMOSFET with a higher breakdown voltage (BV) and figure of merit (FOM) is needed.

In this paper, a split-gate resurf stepped oxide with double floating electrodes (DFSGRSO) UMOSFET is proposed. The floating electrodes are symmetrically distributed on both sides of the source electrode in the trench. The simulation results reveal that the BV and FOM at optimal parameters are higher than those of the conventional structure. In addition, the performance of the DFSGRSO UMOSFET with different size of floating electrodes and the regulatory mechanism of the floating electrodes is analyzed in this paper.

2. Device Structure and Principles of Operation

The schematic of the DFSGRSO UMOSFET is shown in Figure 1b. The electrode in the trench (E_1) is connected to the source electrode in order to achieve charge-coupling. Two floating electrodes are introduced in the trench and located on both sides of the source electrode (E_1) symmetrically. The floating electrodes and the source electrode (E_1) are separated by the oxide layer. Except for the floating electrodes of the DFSGRSO UMOSFET, the other structural parameters are the same as the conventional structure.

As shown in Figure 2, the distribution of the electric field and potential of the DFSGRSO UMOSFET are compared with that of the device with the conventional structure. As shown in Figure 2a,b, the electric field distribution of the DFSGRSO UMOSFET is more uniform compared to the conventional structure, which reveals that the floating electrodes can modulate the electric field of the drift area. The floating electrodes can be regarded as an equipotential body. Therefore, the electric field originally converged on the bottom of the trench moves to the middle of the drift area, which is near the top of the floating electrodes, and it brings a new electric field peak. Furthermore, it can be seen from Figure 2c,d that the introduction of a floating electrode can increase the density of the potential line, which proves that the DFSGRSO UMOSFET has a higher breakdown voltage at the same structural parameters.

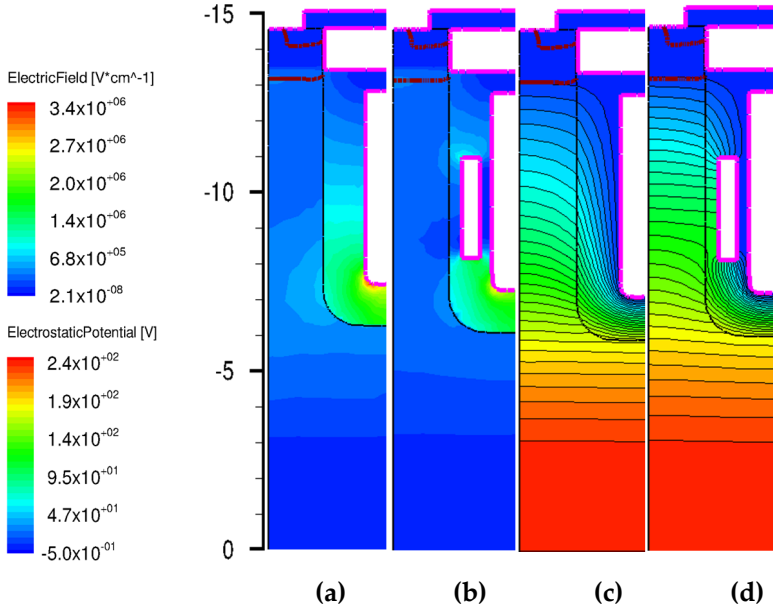

Figure 2. Electric field distribution of (**a**) SGRSO and (**b**) DFSGRSO UMOSFETs and potential distribution of (**c**) SGRSO and (**d**) DFSGRSO UMOSFETs.

As shown in the Figure 3, the electric field intensity on the surface of the trench and in the middle of the drift area for the DFSGRSO UMOSFET are compared with that for the conventional structure, respectively, at the same structure parameters. Figure 3a is a comparison of the electric field on the trench surface of the two structures. It can be clearly seen that a new electric field peak (A) has been brought, which is near the top of the floating electrode, while the intensity of the electric field, which is near the bottom of the floating electrode, has decreased. In addition, the electric field intensity in the middle of the drift area is compared, as shown in Figure 3b. It can be seen that the introduction of the floating electrode improves the intensity of peak 1 significantly, and the distribution of the electric field is more uniform compared with the conventional structure.

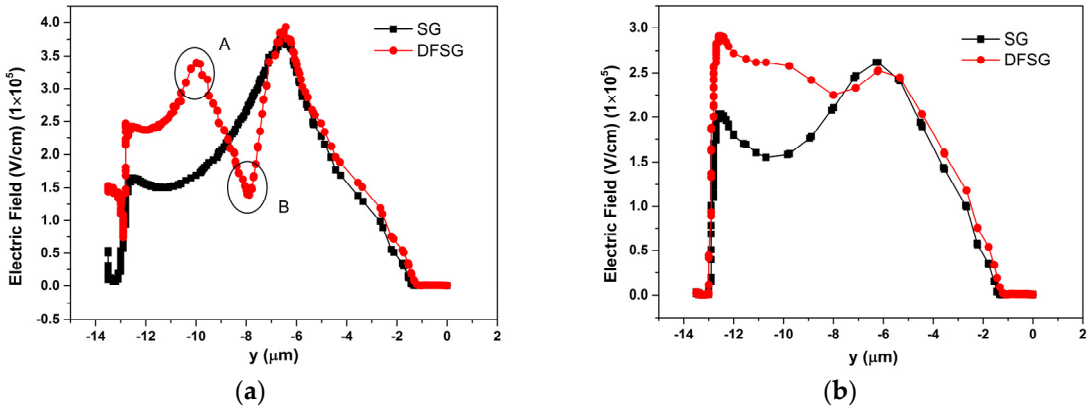

Figure 3. Electric field distributions comparing the (**a**) surface of the trench and (**b**) middle of the drift area for SGRSO and DFSGRSO UMOSFETs with the same n-drift area doping concentration.

A three-dimensional views of the electric field distribution in the drift area of the two structures are shown in Figure 4. Figure 4a–d show the front view and back view of the SGRSO and DFSGRSO UMOSFETs respectively. The electric field distribution in the drift area of the DFSGRSO UMOSFET is more symmetrical compared with the conventional structure where the electric field usually converges at the bottom of the trench. As a result, the volume under the electric field curved surface of the

DFSGRSO UMOSFET is bigger than that of the SGRSO UMOSFET. Hence, the DFSGRSO UMOSFET has a higher BV and FOM.

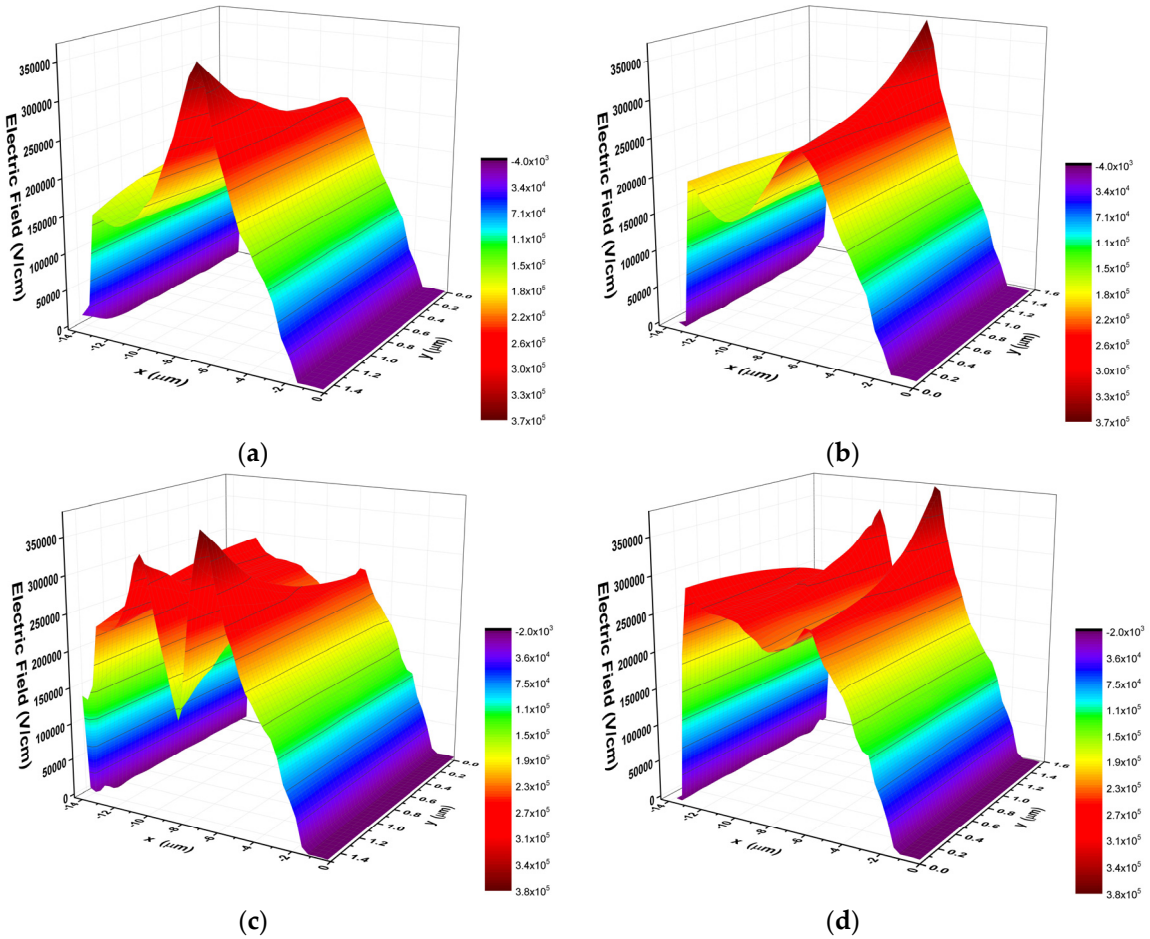

Figure 4. Three-dimension electric field distributions of the (**a**) front view and (**b**) back view of the SGRSO UMOSFET and the (**c**) front view and (**d**) back view of the DFSGRSO UMOSFET with the same n-drift area doping concentration.

3. Fabrication Procedure

First, a N-type epitaxial layer grows on a heavily doped N^+ substrate and a deep trench is formed by dry etching, as shown in Figure 5a. Next, a 1.2 μm oxide is deposited on the trench surface, as shown in Figure 5b. As can be seen in Figure 5c, the trench is filled with highly doped N-type polysilicon and etched back. Then, the trench is filled with oxide and etched back again to obtain the space for the floating electrodes, as shown in Figure 5d. As shown in Figure 5e, a thicker oxide is deposited on the surface of the trench. Afterwards, the trench is refilled with polysilicon and etched back to form the floating electrodes, as shown in the Figure 5f. Subsequently, a 50 nm fresh oxide is grown thermally on the trench sidewalls to form the gate oxide, and the gate is formed by the Chemical Mechanical Polishing (CMP) process, as shown in the Figure 5g. Finally, the n^+ and p^- body is formed by the ion implantation, and the complete structure is shown in Figure 5h.

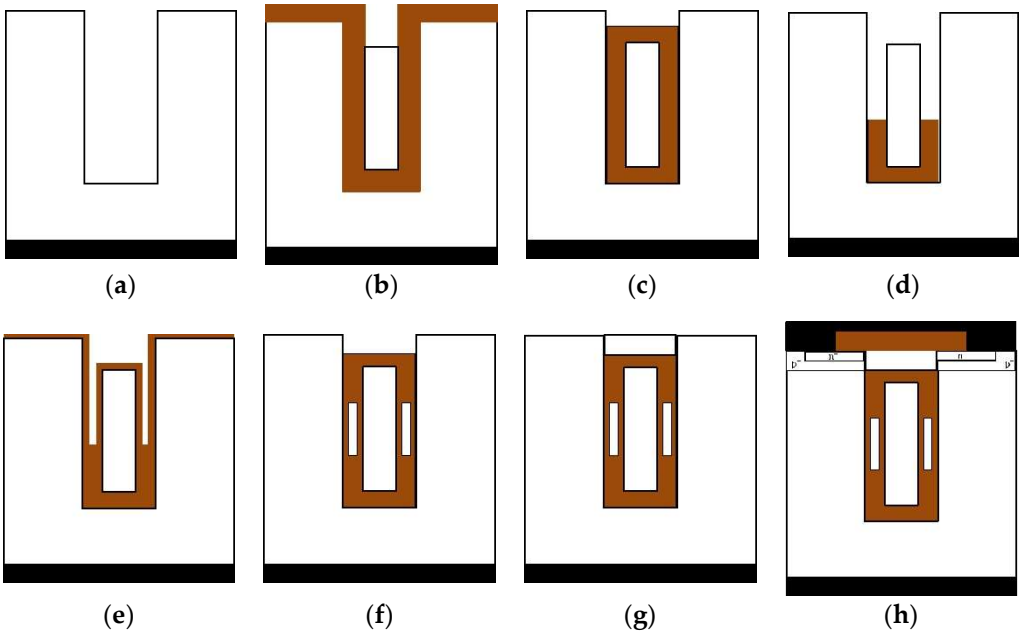

Figure 5. Proposed fabrication process steps for the DFSGRSO UMOSFET.

4. Results and Discussion

To compare the characters of both structures, we adopt the model of bandgap narrowing, the concentration dependent mobility model (CONMOB), the parallel electric field-dependent mobility model (FLDMOB) and the Shockley-Read-Hall model in simulations [24].

Figure 6 shows the dependence of the BV and FOM on the doping concentration of n-drift for the two structures. The parameters of the structures used in the simulations are shown in Table 1. It can be seen that the BV and FOM of the DFSGRSO UMOSFET are always higher than that of the conventional structure in the range of 1×10^{15} cm^3–5×10^{15} cm^3. With the increase of doping concentration, the BV of the two structures decreases gradually, but the FOM value increases and achieves the optimal value when the n-drift doping concentration is 4.5×10^{15} cm^3. As a result, the BV and FOM of the conventional structure are 195.2 V and 236.1 V^2/mΩ·mm^2 respectively, while the BV and FOM of the DFSGRSO UMOSFET are 238.3 V and 352.7 V^2/mΩ·mm^2 respectively, which have been improved by 22.1% and 49.4%.

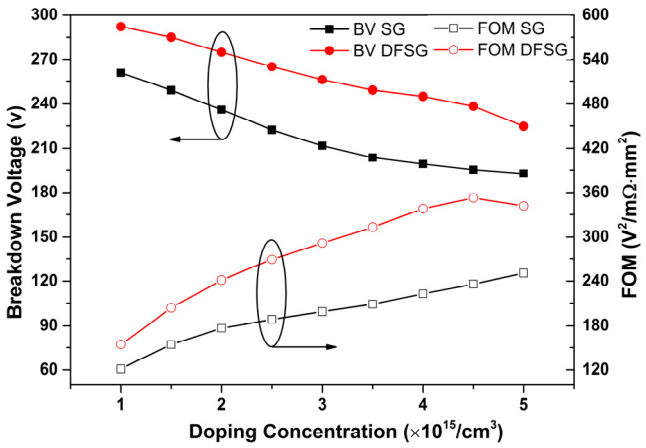

Figure 6. Dependence of the breakdown voltage (BV) and figure of merit (FOM) (BV^2/R_{SP}) on the doping concentration of n-drift for SGRSO and DFSGRSO UMOSFETs.

Table 1. Device parameters for the comparison of simulations.

Parameter	Value
Depth of trench in drift region (H_T)	7.5 μm
Depth of gate (H_G)	1.0 μm
Depth of n^+ source junction	0.2 μm
Depth of p-body junction	0.8 μm
Doping of p-body	1.5×10^{18} cm^{-3}
width of trench (W_T)	3.6 μm
Width of mesa (W_M)	3.2 μm
Width of source electrode E_1 (T_1)	1.6 μm
Thickness of split-gate oxide for SGRSO (t_2)	1.2 μm
Doping of n-drift region (N_D)	4.5×10^{15} cm^{-3}
Width of floating electrodes (T_2)	0.5 μm
Length of floating electrodes (H_1)	2.2 μm
Depth of floating electrodes (H_2)	2.0 μm
Thickness of n-drift region (L)	13.5 μm
Height of source electrode of SGRSO (H)	6.3 μm

The dependence of the BV and FOM on the thickness of the epitaxial layer (L) for the SGRSO and DFSGRSO UMOSFETs is shown in the Figure 7. As can be seen from the figure, with the increase of the thickness of the epitaxial layer for the two structures, the BV reaches saturation state, while FOM increases gradually at first and then decreases after reaching the optimal value, because the on-state resistance gradually increases with the increase of the thickness of the epitaxial layer for both structures. As shown in the results, when the epitaxial layer thickness is 13.5 μm, the FOM of the two structures achieves the optimal value. Furthermore, the BV and FOM of the device with the conventional structure are 198.2 V and 247.3 $V^2/m\Omega{\cdot}mm^2$, while the BV and FOM of the DFSGRSO UMOSFET are 243.1 V and 373.1 $V^2/m\Omega{\cdot}mm^2$, which have been improved by 22.7% and 50.9% respectively.

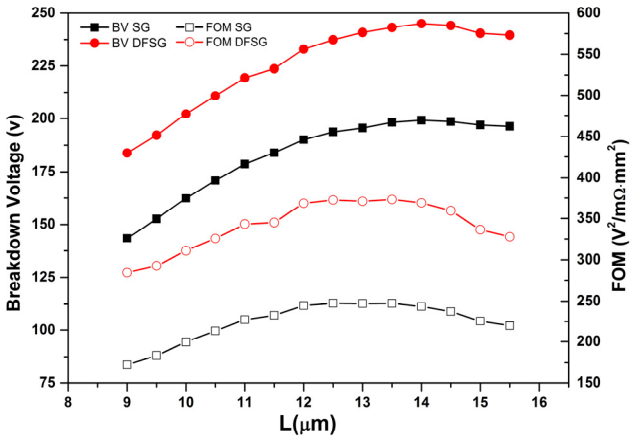

Figure 7. Dependence of the BV and FOM (BV^2/R_{SP}) on the thickness of drift layer (L) for the SGRSO and DFSGRSO UMOSFETs.

The dependence of BV on the length of floating electrodes (H_1) at different depth (H_2) for the DFSGRSO UMOSFET is shown in Figure 8. Each curve in the figure represents the variation of the BV with the length of the floating electrodes at a certain depth for the DFSGRSO UMOSFET. It can be seen from the graph, at different depths, the BV of the DFSGRSO UMOSFET always increases gradually with the length of the floating electrodes at first and then decreases after reaching the optimal value. This is because as the length of the floating electrodes increases, the electric field gradually moves from the bottom of the trench to the middle of the drift area and achieves a uniform state. If the length of the floating electrodes continues to increase, the optimal state is broken, and the electric field around of the PN junction increases sharply. It makes the DFSGRSO UMOSFET break in advance and reduces the

BV of the device. In addition, it can be seen from the graph that the modulation effect of the floating electrodes becomes stronger as its depth increases, and the length of floating electrodes required to achieve optimal station gradually reduces. When the depth and length of the floating electrodes is 2 µm and 2.2 µm respectively, the BV reaches a maximum value of 238.3 V. However, if the depth of the floating electrodes continues to increase, the BV of the DFSGRSO UMOSFET decreases due to the break of the charge-coupling.

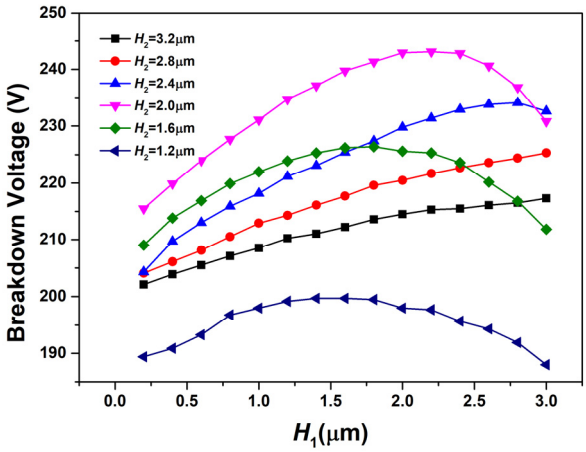

Figure 8. Dependence of the BV on the length of floating electrodes (H_1) at different depth (H_2) for the DFSGRSO UMOSFET.

Figure 9 shows the dependence of the BV on the width of the floating electrodes (T_2) for different lengths (H_1) for the DFSGRSO UMOSFET. Each curve in the figure represents the variation of the BV with the width of the floating electrodes at a certain length. As the width of the floating electrode increases, its BV gradually increases and reaches the optimal value. Furthermore, the trend of the BV with the length is similar to the result of Figure 8. As the length of the floating electrodes increases, the breakdown voltage of the device gradually increases, and the width required to reach the optimal value becomes smaller and smaller. When the length and width of the floating electrode is 2.2 µm and 0.5 µm, the BV and FOM of the DFSGRSO UMOSFET reaches the optimal values of 244.9 V and 378.6 $V^2/m\Omega{\cdot}mm^2$ respectively, which shows an improvement of 23.6% and 53.1% compared with the device with the conventional structure.

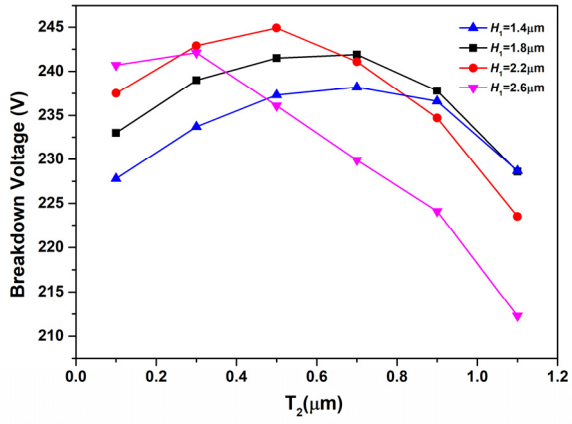

Figure 9. Dependence of the BV on the width of floating electrodes (T_2) at different length (H_1) for the DFSGRSO UMOSFET.

In order to compare the output characteristics of the two structures, the BV of both structures was set at about 200 V by adjusting the doping concentration of the drift area, as shown in the Figure 10a.

The leakage current is limited to 1×10^{-7} A. Figure 10b shows a comparison of the output characteristic for both structures. As can be seen from the graph, when the gate voltage is 4, 8, 12 and 16 V, the output characteristic of the DFSGRSO UMOSFET is higher than that of the device with the conventional structure. Furthermore, the output characteristics of the DFSGRSO UMOSFET at a gate voltage of 8 V are even better than that of the SGRSO UMOSFET at a gate voltage of 16 V.

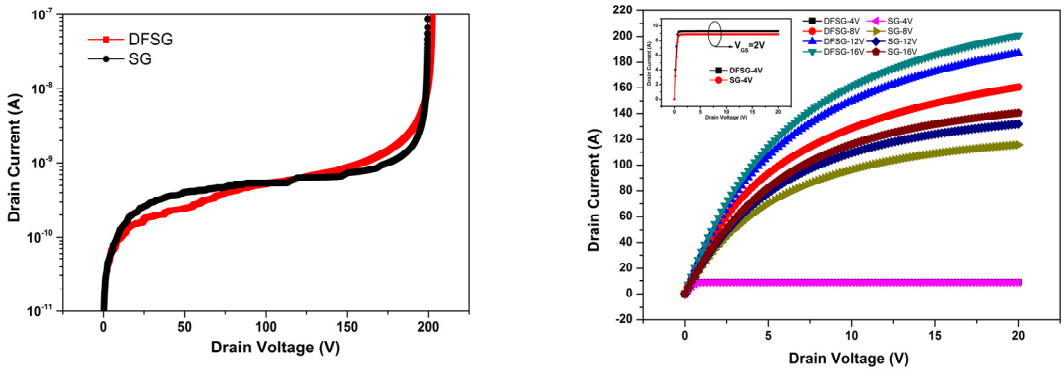

Figure 10. Characteristics comparison of (**a**) breakdown voltage and (**b**) output characteristics for the SGRSO and DFSGRSO UMOSFETs.

As shown in Figure 11, the work of this article is compared with several published works. It can be found that the work of this article has a higher breakdown voltage and a lower on-resistance, which proves that the introduction of floating electrodes helps to improve the overall performance of the device.

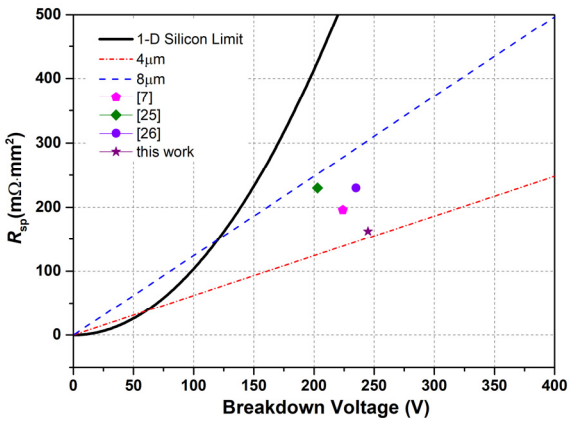

Figure 11. R_{SP} as a function of the BV for one-dimensional silicon limit and two-dimensional charge-coupling limits for the pitches of 4 and 8 μm, some references [7,25,26] and this work.

5. Conclusions

In this paper, a split-gate resurf stepped oxide with double floating electrodes (DFSGRSO) UMOSFET has been proposed. The floating electrodes are symmetrically distributed on both sides of the source electrode in the trench. The regulatory mechanism of floating electrodes has been analyzed. The electric field originally converged on the bottom of the trench moves to the middle of the drift area, which is near the top of the floating electrodes, and it brings a new electric field peak. Therefore, the distribution of the electric field is more uniform for the DFSGRSO UMOSFET compared with the conventional structure. In addition, the performance of the DFSGRSO UMOSFET with different size of floating electrodes has been simulated and analyzed. The simulation results reveal that the floating electrodes introduced in the trench can modulate the distribution of the electric field in the drift area

and improve the performance of the device significantly compared with the conventional structure. The breakdown voltage and FOM at optimal parameters is 23.6% and 53.1% higher than that of the conventional structure.

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