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Selective Epitaxial Growth of In Situ Doped SiGe on Bulk Ge for p⁺/n Junction Formation

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Abstract: Epitaxial in situ doped Si_{0.73}Ge_{0.27} alloys were grown selectively on patterned bulk Ge and bulk Si wafers. Si_{0.73}Ge_{0.27} layers with a surface roughness of less than 3 nm were demonstrated. Selectively grown p⁺Si_{0.73}Ge_{0.27} layers exhibited a resistivity of 3.5 mΩcm at a dopant concentration of 2.5 × 10¹⁹ boron atoms/cm³. P⁺/n diodes were fabricated by selectively growing p⁺-Si_{0.73}Ge_{0.27} on n-doped bulk Ge and n-doped Si wafers, respectively. The geometrical leakage current contribution shifts from the perimeter to the bulk as the diode sizes increase. Extracted near midgap activation energies are similar to p⁺/n Ge junctions formed by ion implantation. This indicates that the reverse leakage current in p⁺/n Ge diodes fabricated with various doping methods, could originate from the same trap-assisted mechanism. Working p⁺/n diodes on Ge bulk substrates displayed a reverse current density as low as 2.2·10⁻² A/cm² which was found to be comparable to other literature data. The layers developed in this work can be used as an alternative method to form p⁺/n junctions on Ge substrates, showing comparable junction leakage results to ion implantation approaches.

Keywords: germanium; SiGe; junction; diode; selective; epitaxy

1. Introduction

Currently Ge based field effect transistor (FET) devices are researched due to their potential for low voltage operation stemming from the superior hole and electron mobility in Ge as compared to Si. A critical aspect in fabricating such devices is junction formation and control of junction leakage current. Junctions on bulk Ge have been traditionally formed with ion implantation and a subsequent anneal. The need for highly doped, shallow and abrupt junctions on Si has been met with the introduction of selective epitaxially grown in situ doped SiGe layers [1–8]. Junctions on bulk Ge have been traditionally formed with ion implantation and a subsequent anneal to activate the implanted dopants [9,10]. However, ion implantation damages the Ge crystal [11,12]. This creates the need for a high temperature treatment to anneal out the defects and recrystallize Ge [13–16]. A high heating rate can induce structural damage while a low annealing time might not fully crystallize the implanted region, resulting in defect formation that will affect the junction leakage current [17]. Reaching high doping concentrations (>10²⁰ cm⁻³) can give rise to defect formations that affect dopant diffusion [18]. Recently a report has shown the potential of sequential 3D integration with Ge devices [19]. Such fabrication methods require a reduced thermal budget, usually determined by an upper limit in the area of 600 °C [20,21]. Selective epitaxy of in situ doped SiGe is an implantation-free and temperature-flexible process. It has therefore, the potential to address the challenges outlined above. In [22] epitaxial in situ n⁺ doped SiGe with concentrations from 20% to 100% Ge are grown on virtual Ge substrates to achieve low source/drain contact resistance (ρ_c). It is shown that 20% Ge content in the in situ doped SiGe alloy exhibits approximately two orders of magnitude lower

ρ_c than the ion implanted SiGe with the same Ge content. In [23] a simulation study of As doped $\text{Si}_{0.75}\text{Ge}_{0.25}$ embedded stressors in a Ge FinFET fabricated on germanium-on-insulator (GOI) substrates is presented. The authors show a three-fold improvement in the device current at the ON state (I_{ON}), achieved with 25% Ge in the SiGe stressor.

This work investigates the feasibility of selectively grown, in situ doped $\text{p}^+-\text{Si}_{0.73}\text{Ge}_{0.27}$ layers as a source/drain junction material. Planar p^+/n diodes were fabricated on SiO_2 patterned, bulk n-Ge substrates using selective epitaxy of $\text{p}^+-\text{Si}_{0.73}\text{Ge}_{0.27}$. A benchmark towards other junctions on Ge bulk is performed. Insights on junction leakage that can be helpful for further device integration are provided by the electrical characterization of the p^+/n diodes. The thermal budget for the process presented here was set by the epitaxial growth temperature of 650 °C. The layers can potentially be integrated in germanium-on-insulator (GOI) substrates and in sequential 3D integration where the process budget for dopant activation is limited.

2. Materials and Methods

Selective epitaxial growth of in situ doped $\text{Si}_{0.73}\text{Ge}_{0.27}$ was performed on n-Si wafers (525 μm , As doped, resistivity = 20–40 Ohm-cm, supplied by Westec) and on n-Ge wafers (460 μm , Sb doped, resistivity = 0.05–0.25 Ohm-cm, supplied by Umicore). A description of the process flow and the resulting diode structures on Si and Ge substrates is shown in Figure 1. The openings towards Ge or Si were patterned on a 200 nm SiO_2 with i-line optical lithography. Dry etch was used to remove all but ~20 nm SiO_2 layer on top of the surface openings. The remaining SiO_2 layer was removed during pre-epitaxy surface cleaning. For Si surfaces, ex situ surface treatment was performed in a 3:1 mixture of H_2SO_4 (CAS 7664-93-9, 95–97%, BASF/Merck) / H_2O_2 (CAS 7722-84-1, >=35–<50%, Sigma-Aldrich Sweden AB) followed by 1% HF (CAS 7664-39-3, 5% wt, BASF/Sigma-Aldrich Sweden AB) diluted in H_2O . Ge surfaces require a different ex situ cleaning approach that does not involve H_2O_2 which is a Ge etchant. In this work a 1% HF surface clean in an automated wet etch spray tool followed by a rinse and dry step was conducted prior to loading in the epitaxial reactor. All epitaxial growth was performed in an ASM Epsilon 2000 reduced pressure chemical vapor deposition (RPCVD) reactor at a constant pressure of 20 Torr in H_2 ambient. In situ surface preparation was common for both Si and Ge substrates and was conducted at 800 °C in H_2 for 10 min inside the RPCVD chamber. This temperature was well below the melting point of Ge and potential Ge surface reflow issues were thus avoided. The selective epitaxial growth of SiGe was performed at 650 °C under 20 Torr with H_2 (20 slm, 10% in N_2 , CAS 1333-74-0, <=100%, AGA Gas AB/Air Liquide) as the carrier gas. The gas precursors for Si and Ge species are H_2SiCl_2 (60 sccm, CAS 4109-96-0, <=100%, AGA Gas AB/Air Liquide) and GeH_4 (10 sccm, CAS 7782-65-2, 10% in H_2 , AGA Gas AB), respectively. The *in situ* doping was achieved B_2H_6 (80 sccm, CAS 019287-45-7, 1% in H_2 , AGA Gas AB) for p^+SiGe . A 10 s 1% HF dip was employed prior to the metal contact definition. A 100 nm TiW and 500 nm Al metal stack was deposited by physical vapor deposition (PVD) for contacting the fabricated diodes.

Figure 1. The p^+/n diode fabrication flow is shown in the left. The resulting device is depicted on the right. Each device is accessed from the top via a TiW/Al metal stack and the bottom of the bulk substrate via the measurement unit's chuck.

3. Results and Discussion

3.1. Layer Characterization

Atomic force microscopy (AFM) was used for surface roughness and step height profile measurements. The AFM image is shown in Figure 2. The p^+ -Si_{0.73}Ge_{0.27} layers show a root mean square (RMS) surface roughness of < 3 nm. Spectroscopic ellipsometry (SE) was used for layer thickness and Ge content measurements. The growth rate of the p^+ -Si_{0.73}Ge_{0.27} on Ge was 45 nm/min. Secondary ion mass spectroscopy (SIMS) was performed to determine the dopant concentration and the Ge content in the Si_{0.73}Ge_{0.27} alloy. The SIMS profiles are shown in Figure 3. Dopant concentration is 2.5×10^{19} B atoms per cm³. Ge content is 27% in agreement with the result from SE. A summary of the layer characterization results is presented in Table 1. X-ray diffraction (XRD) measurements were performed on SiGe layers grown on 1.7 μ m of Ge strain relaxed buffer substrates (SRB). The Ge SRB substrates were grown in house as reported in [24].

Figure 2. Atomic force microscopy (AFM) image ($35 \mu\text{m} \times 35 \mu\text{m}$) of the p^+ -Si_{0.73}Ge_{0.27} film grown on the substrate openings of an SiO₂ masked Ge strain relaxed buffer (SRB) wafer. The root mean square (RMS) surface roughness is 2.4 nm. The growth is selective to SiO₂.

Table 1. p^+ -Si_{0.73}Ge_{0.27} layer properties. For the growth rate, all three methods are in agreement at ~45 nm/min. Similarly, Ge content as deduced from the three methods is ~30%.

Title 1		Value	
Growth rate (nm/min)	SE: 45	AFM: 42	Weight: 50
Ge content (%)	SE: 29	XRD: 30	SIMS: 27
Resistivity (m Ω cm)	-	3.5	-
Surface roughness (nm)	-	2.4	-

In Figure 4 the ω -2 θ XRD profile of 120 nm thick p^+ -Si_{0.73}Ge_{0.27} grown on Ge SRB is shown. The Si peak corresponds to the Si bulk on which the Ge SRB was grown. The XRD peak suggests Ge content of 27%.

Figure 3. Secondary ion mass spectroscopy (SIMS) analysis on 80 nm thick p^+ - $\text{Si}_{0.73}\text{Ge}_{0.27}$ layer grown on Ge SRB. Boron dopant concentration is 2.5×10^{19} atoms/ cm^3 . The peak for the B concentration around 80 nm layer depth is due to dopant segregation at the SiGe/Ge interface. The Ge content of the SiGe layer is 27%.

Figure 4. X-ray diffraction results of the 120 nm thick p^+ - $\text{Si}_{0.73}\text{Ge}_{0.27}$ layer grown on Ge. The peak corresponding to $\text{Si}_{0.73}\text{Ge}_{0.27}$ does not show well defined fringes due to layer relaxation.

3.2. Electrical Characterization and Analysis

Square shaped diodes with varying sizes were measured. The junction quality between the epitaxially grown p^+ - $\text{Si}_{0.73}\text{Ge}_{0.27}$ layer and the substrate was evaluated by examining the reverse leakage current (I_R). The thickness of the p^+ - $\text{Si}_{0.73}\text{Ge}_{0.27}$ films was 40 nm for both Ge and Si substrates. I_R values were extracted at a reverse voltage of 1 V for all diode sizes. In Figure 5 the current (I)–voltage (V) characteristics of diodes on Ge bulk with areas from $4 \mu\text{m}^2$ to $10^4 \mu\text{m}^2$ are shown.

Figure 5. Current (I) versus applied voltage (V), for p^+ - $\text{Si}_{0.7}\text{Ge}_{0.3}$ on n -type Ge diodes with area from $4 \mu\text{m}^2$ to $10^4 \mu\text{m}^2$.

The forward current is in the same order of magnitude for all the diodes and is limited by the series resistance of the back contact to the wafer as well as the bulk resistance of the wafer itself (Figure 1). The ideality factor is ~ 1.3 as extracted from the $4 \mu\text{m}^2$ and $9 \mu\text{m}^2$ diodes. Leakage current density of $2.2 \cdot 10^{-2} \text{ A/cm}^2$ is achieved for the $10^4 \mu\text{m}^2$ diode. Figure 6 shows I_R as a function of the perimeter (P) length for Ge and Si diodes. The reverse leakage current is about two decades higher for Ge devices due to the higher intrinsic carrier concentration in Ge compared to Si. For squared shaped diodes I_R can be expressed as the sum of the leakage current per unit area (I_A) and the leakage current per unit perimeter (I_P) as follows [25–28]:

$$I_R = I_A \times P^2/16 + I_P \times P \quad (1)$$

The solid black lines show the reverse current behavior as a function of only area (P^2) or perimeter (P). The solid red and blue lines in Figure 6 display I_R using Equation (1) with I_A and I_P as fitting parameters. Area and perimeter components of I_R for Ge and Si substrates are found to be:

$$\begin{aligned} I_{A,\text{Si}} &= 2.1 \times 10^{-12} \text{ A}/\mu\text{m}^2, & I_{P,\text{Si}} &= 1.8 \times 10^{-12} \text{ A}/\mu\text{m} \\ I_{A,\text{Ge}} &= 2.4 \times 10^{-10} \text{ A}/\mu\text{m}^2, & I_{P,\text{Ge}} &= 2.2 \times \text{A}/\mu\text{m} \end{aligned}$$

For small area diodes, with a perimeter of $8 \mu\text{m}$ or $12 \mu\text{m}$, the perimeter component of the leakage current dominates I_R . This occurs both on Si and Ge substrates although the effect is slightly more pronounced on Ge, possibly due to higher surface state density for SiO_2/Ge interfaces compared to the SiO_2/Si interfaces. The higher perimeter leakage on Ge substrates has been reported on p^+ / n -diode fabricated by ion implantation [29].

For diodes with a perimeter length of $40 \mu\text{m}$ and above, the area component dominates I_R and for the largest diodes ($10^4 \mu\text{m}^2$), the area component is $>20\times$ the perimeter component. Therefore, the largest diodes were further characterized by evaluating the temperature dependence of I_R . Figure 7 shows an Arrhenius plot of I_R for Ge and Si diodes in the temperature range of -50°C to 100°C . The extracted activation energy was 0.42 eV for Ge and 0.48 eV for Si, respectively.

Figure 6. Area and perimeter dependent diode leakage current for Ge and Si substrates. In the insert the two main leakage mechanisms are graphically depicted. The black lines show the reverse current as a function of only area (P^2) or perimeter (P). Red and blue lines depict I_R for Ge and Si using Equation (1) and fitting parameters I_A and I_P .

Figure 7. Arrhenius plot of the leakage current I_R versus $1/kT$ for $10^4 \mu\text{m}^2$ diodes where the bulk leakage dominates.

The activation energies are consistent with area dependent leakage currents caused by trap assisted generation/recombination mechanisms for both Ge and Si diodes [30,31]. For these activation energies, the trap centers can potentially originate at the interface between the $p^+-\text{Si}_{0.73}\text{Ge}_{0.23}$ layer and the substrates without eliminating the possibility for defects in the bulk wafers.

Reverse current density values extracted at 1 V from similarly sized p^+/n diodes ($\sim 10^4 \mu\text{m}^2$) on Ge reported in the literature are shown in Table 2 for comparison [32–37]. The literature data were chosen in order to cover as broad an area as possible in terms of doping techniques, annealing approaches and substrates. Diodes fabricated with ion implantation (I/I), spin-on-dopant (SOD) techniques as well as various anneals (laser annealing—LA, ELA and rapid thermal annealing—RTA) are included. The sole experimental data reported so far with a non-ion implantation approach can be found in [33]

where a spin-on-dopant (SOD) technique is used. The leakage current of the Ge diodes in this work is on a par with p^+/n SOD junctions reported in [33] that have also been laser annealed. In addition, leakage current densities reported here are within the range of ion implanted p^+/n diodes reported in [32–35]. Our work shows similar levels of leakage current density as in the ion implantation junction studies. The near midgap activation energies for p^+/n diodes (with B ion implantation for the p^+ region) reported by Duffy et al. in [30], are close to the activation energies in this work. This indicates that the reverse leakage current in p^+/n germanium diodes has the same origin for the various doping methods in Table 2.

Table 2. Leakage current density comparison between a $10^4 \mu\text{m}^2$ diode fabricated with selective epitaxy (this work) and other published data of similarly sized diodes (where that information was available). The reverse current values were graphically extracted at 1V.

Reported Data	J_R @ 1 V (A/cm ²)	Doping/Anneal
This work	$\sim 2 \times 10^{-2}$	p^+ -Si _{0.73} Ge _{0.27} RTA (N ₂) 600 °C
[32] Park et al.	$\sim 9 \times 10^{-3}$	B $\times$ I/I + Co capping layer RTA (N ₂) 380 °C
[33] Li et al.	$\sim 5 \times 10^{-2}$	Spin on dopant LA & RTA (N ₂) 495 °C
[34] Eneman et al.	$\sim 3 \times 10^{-2}$	B $\times$ I/I* RTA (N ₂) 500 °C
[35] Bhatt et al.	$\sim 2 \times 10^{-2}$	B $\times$ I/I @ -100 °C RTA (N ₂) 400 °C
[36] Simoen et al.	$\sim 5 \times 10^{-3}$	B $\times$ I/I RTA (N ₂) 500 °C
[37] Matsumura et al.	$\sim 2 \times 10^{-3}$	B $\times$ I/I on GOI substrate RTA (N ₂) 400 °C

Key: B: Boron, I/I: ion implantation, LA: laser anneal; * No halo implant, standard and heavy halo show higher leakage.

4. Conclusions

In situ doped Si_{0.73}Ge_{0.27} layers have been successfully grown on n-Ge bulk wafers at 650 °C. In-situ boron doped p^+ -Si_{0.73}Ge_{0.27} layers exhibit a resistivity of 3.5 mΩcm and a dopant concentration of $2.5 \cdot 10^{19} \text{ cm}^{-3}$. For both Ge and Si diodes the dominant leakage current component shifts from perimeter to area as the diode sizes increase. The extracted near midgap activation energy is similar to p^+/n Ge junctions formed by ion implantation methods. This indicates that the reverse leakage current in p^+/n Ge diodes could originate from the same trap-assisted mechanism for various doping methods. A leakage current density of $2.2 \cdot 10^{-2} \text{ A/cm}^2$ for $10^4 \mu\text{m}^2$ diode area is achieved on Ge wafers with an RTA anneal of 600 °C. This result is on a par with the literature data from ion implantation and spin-on-dopant approaches, showing that selective epitaxy of in situ doped SiGe layers is a promising candidate for low temperature junction formation on Ge substrates.

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