Article

An AMOLED Pixel Circuit Based on LTPS Thin-film Transistors with Mono-Type Scanning Driving

Jianyuan Ke, Lianwen Deng *, Liying Zhen, Qing Wu, Congwei Liao, Heng Luo[‡] and Shengxiang Huang[‡]

School of Physics and Electronics, Central South University, Changsha 410083, China; ke_jianyuan@csu.edu.cn (J.K.); liyingzhen@csu.edu.cn (L.Z.); wuwuqing@csu.edu.cn (Q.W.); liaocw@csu.edu.cn (C.L.); luohengcsu@csu.edu.cn (H.L.); hsx351@csu.edu.cn (S.H.)

* Correspondence: denglw@csu.edu.cn; Tel.: +86-13787206916

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Abstract: Using low-temperature poly-silicon thin-film transistors (LTPS TFTs) as a basis, a pixel circuit for an active matrix organic light-emitting diode (AMOLED) with narrow bezel displays was developed. The pixel circuit features mono-type scanning signals, elimination of static power lines, and pixel-integrated emitting control functions. Therefore, gate driver circuits of the display bezel can be simplified efficiently. In addition, the pixel circuit has a high-resolution design due to an increase of the pulse width of the scan signal to extend the threshold voltage and internal-resistance drop (IR drop) detection period. Further, regarding the influences of process–voltage–temperature (PVT) variation in the pixel circuit, comparison investigations were carried out with the proposed circuit and other pixel circuits with mono-type scanning signals using Monte Carlo analysis. The feasibility of the proposed pixel circuit is well demonstrated, as the current variations can be reduced to 2.1% for the supplied power reduced from 5 V to 3 V due to IR drop, and the current variation is as low as 10.6% with operating temperatures from −40 degrees to 85 degrees.

Keywords: AMOLED; LTPS TFT; pixel circuit; IR drop; Monte Carlo

1. Introduction

Active-matrix organic light-emitting diode (AMOLED) displays have an important presence in mainstream next-generation displays due their extremely high contrast ratio, fast electrical-optical response, and excellent compatibility with flexible electronics [1,2]. Although different AMOLED backplane solutions have been discussed over the past decades [3,4], for state-of-the-art AMOLED displays, low-temperature poly-silicon thin-film transistors (LTPS TFTs) show better performance. Compared with other types of TFTs, LTPS TFTs exhibit higher mobility and better stability in terms of electrical characteristics [5,6]. However, the drawbacks of LTPS TFTs lie in the obvious variations in the threshold voltage (V_{TH}) and mobility [7,8], which hinder the implementation of high-quality AMOLEDs with uniform display for larger dimensions. For OLED pixel circuit design, the method of detecting and compensating the non-uniformities in TFT characteristics is essential. In addition, the internal-resistance drop (IR drop) on the power line brings additional variation to OLED displays in larger-sized AMOLED panels [9,10]. Further, for co-design of pixel circuits with TFT-integrated gate drivers, it is necessary to meet the requirements of ultra-narrow border displays.

AMOLED pixel schematics can be categorized into three types: voltage programming methods [11,12], current programming methods [13,14], and external compensation methods [15,16]. Voltage-programming methods are mainstream for LTPS OLEDs because current programming methods need long settling times for small currents, and external compensation methods are too complicated. However, for voltage programming methods, the pixel circuit is required to correct

variations in V_{TH} , mobility, and V_{DD} . Thus, Lin et al. proposed a feedback pixel circuit to calibrate the gate voltage distortion of driving TFTs during the light emission time [17]. Lee et al. re-used the scan line for supplying power to replace the conventional power line to increase the aperture ratio [18]. Further, to avoid image flicker, Lin et al. employed overlapping compensation waveforms to extend the V_{TH} detection time and to suppress the OLED current during the compensation time [19]. These previous investigations illustrate that, through a proper circuit topology and timing diagram to offset V_{TH} variations and IR drop, a good display uniformity can be obtained. However, for conventional schematics, the pixel circuit array requires multiple scan signals with different types, which complicates both the pixel circuit and the external gate driver circuit.

In this paper, a compensation AMOLED pixel circuit with mono-type scanning lines is proposed. An emit-controlling function is integrated within the pixel circuit, and the conventional V_{DD} line is also eliminated. Table 1 shows the comparison among the proposed and previous pixel circuits. For conventional pixel circuits, complicated gate drivers are required, as multiple types of scan signals are used, while the proposed circuit has fewer control signals for simpler external drivers. Comparison investigations are carried out with the proposed circuit and other AMOLED pixel circuits with mono-type scanning lines.

Table 1. Comparison among the proposed and previous pixel circuits. TFT: thin-film transistor.

Reference	TFT Number	TFT Type	Number of Scan Lines	Scanning Signal Types	Flicker Prevention	Detection Time Extension
[5]	6T1C	p-type, poly-Si	3	3	No	Yes
[7]	5T2C	p-type, poly-Si	3	3	Yes	Yes
[8]	5T2C	p-type, poly-Si	4	4	Yes	Yes
[9]	5T2C	n-type, a-Si:H	3	3	Yes	Yes
[11]	3T2C	p-type, poly-Si	2	2	No	No
[17]	5T2C	p-type, poly-Si	3	3	Yes	Yes
This work	7T2C	p-type, poly-Si	2	1	Yes	Yes

2. Pixel Circuit Description

Figure 1 shows the schematic and timing diagram of proposed pixel circuit, which consists of seven TFTs and the two capacitors (C_{ST} and C_{TH}). The specifications for the proposed pixel circuit are shown in Table 2. Here, P1 is the driving transistor, and P2 to P7 are switching transistors. The voltage across C_{TH} is reset by the switching transistors P2, P4, P5, and P7 during the initialization phase. The V_{TH} of P1 and supplied power information are stored by the right terminal of C_{TH} by the turning on of P2 for the detection phase. The data signal is transferred to the left terminal of C_{TH} through P3, and the OLED starts to emit following the negative pulse of $V_{SCAN}(n+2)$ through the pull-down of P6. Figure 2 shows the layouts of a single subpixel of the proposed pixel circuit and 5T2C bootstrap pixel circuit [20]. Although the proposed pixel circuit uses more TFTs than 5T2C, the layout area has not increased much, so it has little effect on resolution. The working process of the pixel circuit will be described in detail.

Figure 1. The proposed active matrix organic light-emitting diode (AMOLED) pixel circuit. (a) The circuit schematic, and (b) the timing diagram. V_{TH} : threshold voltage; V_{DATA} : data voltage.

Table 2. Parameters of the proposed pixel circuit.

Parameter	Value	Parameter	Value
W/L (P1)	4 $\mu\text{m}/10 \mu\text{m}$	W/L (P7)	4 $\mu\text{m}/4 \mu\text{m}$
W/L (P2)	4 $\mu\text{m}/4 \mu\text{m}$	V_{SCA}	−10–5 V
W/L (P3)	4 $\mu\text{m}/4 \mu\text{m}$	V_{SS}	−4 V
W/L (P4)	4 $\mu\text{m}/4 \mu\text{m}$	V_{REF}	−1 V
W/L (P5)	4 $\mu\text{m}/4 \mu\text{m}$	C_{TH}	0.1 pF
W/L (P6)	4 $\mu\text{m}/4 \mu\text{m}$	C_{ST}	0.3 pF

Figure 2. Layout of the pixel circuit. (a) The 5T2C bootstrap pixel circuit, and (b) the proposed AMOLED pixel circuit.

2.1. Initialization Phase

During the initialization phase, P2, P5, and P7 are turned on as both $V_{SCAN}(n - 1)$ and $V_{SCAN}(n)$ are at a low level. Then the gate voltage of P4 is pulled down, and P4 is turned on for resetting the drain electrode of P1 with a relatively low voltage level, i.e., below the turning-on voltage of OLED (V_{OLED}). In addition, the gate and the drain electrodes of the driving transistor P1 are shorted by P2 and the gate voltage of P1 is also discharged through P4, while the left electrode of C_{TH} is initialized with V_{REF} by P5. The electrical hysteresis phenomenon in P-type LTPS transistors should be considered,

i.e., the drain-to-source current varies with different gate-sweeping directions, which relates with short-term image sticking issues [21,22]. As C_{TH} is properly initialized before the programming phases, the hysteresis effects can be efficiently suppressed.

2.2. Detection Phase

During the detection phase, P4 is turned off as $V_{SCAN}(n-1)$ switches to a high level. Then, the gate and the drain electrodes of P1 are gradually charged until the voltage difference between the gate and the source of P1 is V_{TH} . By the end of the detection phase, the gate voltage of P1 approximates the voltage of the power line minus $|V_{TH}|$. Since P1 operates in the saturation region, the transient response for the gate voltage of P1 can be expressed as:

$$(C_{TH} + C_{P1_GS} + C_{P2_GD}) \frac{dV_G(t)}{dt} = \frac{1}{2} \mu C_{OX} \frac{W}{L} [V_H - V_G(t) - |V_{TH}|]^2, \quad (1)$$

where C_{P1_GS} , C_{P2_GD} , μ , C_{OX} , W/L , and V_H are the gate-to-source capacitance of P1, the gate-to-drain capacitance of P2, field-effective mobility, gate capacitance per unit area, ratio of the channel width to channel length of P1, and the high level of the scan signal, respectively. Assuming the initial value of the P2's gate electrode as V_O , V_G can be solved as:

$$V_G(t) = V_H - |V_{TH}| - \frac{1}{\frac{\mu C_{OX} W(t-t_0)}{2L(C_{TH} + C_{P1_GS} + C_{P2_GD})} + \frac{1}{V_O - V_H + |V_{TH}|}}, \quad (2)$$

where t_0 and t are the start and end times of the charging process, respectively. The compensating efficiency might be reversely affected by the detection accuracy of V_{TH} and V_H . As shown in Equation (2), for accurate detection of V_{TH} and V_H , a relatively long charging time is required. However, due to the increasing of display resolution, it becomes difficult to extend the detection time.

2.3. Data Writing Phase

During the data writing phase, P3 and P6 are turned on as the levels of $V_{scan}(n-1)$ and $V_{scan}(n)$ are low, and P2, P5, and P7 are turned off as the level of $V_{scan}(n+2)$ is high. Then the data voltage, i.e., V_{DATA} , is transferred to the left electrode of C_{TH} through P3. According to the charge conservation law, the voltage at the right electrode of C_{TH} can be expressed as:

$$V_G' = V_G - \frac{C_{P1_GD} V_G}{C_{TH} + C_{P1_GS} + C_{P1_GD} + C_{P2_GD}} + \frac{C_{TH}(V_{DATA} - V_{REF})}{C_{TH} + C_{P1_GS} + C_{P1_GD} + C_{P2_GD}}, \quad (3)$$

Considering that C_{P1_GD} , C_{P1_GD} , and C_{P2_GD} are much smaller than C_{TH} , one can simplify Equation (3) to:

$$V_G' = V_G + V_{DATA} - V_{REF}, \quad (4)$$

2.4. Emitting Phase

Finally, in the emitting phase, the driving TFT provides the current to OLED pixel, which can be expressed by:

$$\begin{aligned} I_{OLED} &= \frac{1}{2} \mu C_{OX} \frac{W}{L} (V_H - V_G' - |V_{TH}|)^2 \\ &= \frac{1}{2} \mu C_{OX} \frac{W}{L} (V_H - V_H + |V_{TH}| + \frac{1}{\frac{\mu C_{OX} W(t-t_0)}{2L(C_{TH} + C_{P1_GS} + C_{P2_GD})} + \frac{1}{V_O - V_H + |V_{TH}|}} + V_{REF} - V_{DATA} - |V_{TH}|)^2 \\ &= \frac{1}{2} \mu C_{OX} \frac{W}{L} (V_{REF} - V_{DATA} + \frac{1}{\frac{\mu C_{OX} W(t-t_0)}{2L(C_{TH} + C_{P1_GS} + C_{P2_GD})} + \frac{1}{V_O - V_H + |V_{TH}|}})^2 \end{aligned} \quad (5)$$

Therefore, I_{OLED} is determined by V_{REF} and V_{DATA} , being almost independent of V_{TH} and V_H . As shown in Equation (5), the third term in the parenthesis is reversely related with the effective mobility, and then the pixel circuit also renders certain compensation function of mobility non-uniformities. In addition, P4 is maintained off for the initialization and detection phases, the leakage current of the OLED can be suppressed efficiently, and improved contrast ratio with reduced flicker can be obtained.

3. Gate Driver Description

For the co-design of pixel circuit and gate driver circuit, the Rensselaer Polytechnic Institute (RPI) model with Level 36 is used to reproduce the electrical performance of the p-type LTPS TFTs. Figure 3 demonstrates the comparison of the measured and simulated transfer characteristics of LTPS TFT in a logarithm scale. Calculated using the classic current-voltage model of MOSFET, the field-effect mobility, the threshold voltage and the sub-threshold swing for the LTPS TFT are approximately $72 \text{ cm}^2 (\text{V}\cdot\text{s})^{-1}$, -1.1 V , and 0.74 V/decade , respectively.

Figure 3. Measured and simulated transfer characteristics of the low-temperature poly-silicon thin-film transistor (LTPS TFT) with an aspect ratio of $4 \mu\text{m}/4 \mu\text{m}$. C_{OX} : gate capacitance per unit area; μ : field-effective mobility; SS : sub-threshold swing.

For the proposed pixel circuit, the high-to-low pulses with line-by-line scanning sequences are needed. Figure 4 shows the gate driver unit, which consists of six TFTs and one capacitor. The parameters of the gate driver unit are shown in Table 3 and the operating mechanism has been detailed elsewhere [23]. In order to generate the required scan signal, four clocks with overlapped waveforms are used. Figure 5 shows the block diagram of the gate driver with detection time half of the scan pulse. The simulation results are illustrated in Figure 6. The devised gate driver circuit is well verified, and a rail-to-rail output range, i.e., from -10 V to 5 V , can be obtained for the gate driver, with the rising and falling times of $1.68 \mu\text{s}$ and $1.76 \mu\text{s}$ for loading resistance of $2 \text{ K}\Omega$ and loading capacitance of 200 pF .

Table 3. Parameters of the gate driver circuit.

Parameter	Value	Parameter	Value
W/L (G1)	$500 \mu\text{m}/4 \mu\text{m}$	W/L (G6)	$10 \mu\text{m}/4 \mu\text{m}$
W/L (G2)	$30 \mu\text{m}/4 \mu\text{m}$	C_1	0.8 pF
W/L (G3)	$20 \mu\text{m}/4 \mu\text{m}$	CK	$-10\text{--}5 \text{ V}$
W/L (G4)	$10 \mu\text{m}/4 \mu\text{m}$	IN	$-10\text{--}5 \text{ V}$
W/L (G5)	$10 \mu\text{m}/4 \mu\text{m}$	V_{GH}	5 V

Figure 4. The integrated gate driver unit, with (a) the schematic, and (b) the timing diagram.

Figure 5. The block diagram of the proposed gate driver circuit.

Figure 6. The transient response of the proposed gate driver circuit with $R_L = 2 \text{ K}\Omega$ and $C_L = 200 \text{ pF}$.

4. Results and Discussion

As mentioned above, a sufficient detection time for V_{TH} and V_H is required to improve the compensation accuracy of pixel circuit. However, with the increase of display resolution and frame rate, the detection time for V_{TH} and V_H is decreasing. To be more specific, for frame rate of 60 Hz, the row times for the resolution of full-high-definition (FHD) (1920 red–green–blue(RGB)×1080), quad-high definition (QHD) (2560 RGB×1440), and ultra-high-definition (UHD) (3840 RGB×2160), are 15.4 μ s, 11.5 μ s, and 7.7 μ s, respectively. In the proposed circuit, the detection time can be increased by adjusting of the scanning signals. In addition to increase the scan pulse width, modifications of the scanning sequence for the pixel circuit include, replacing the original $V_{SCAN}(n-1)$ and $V_{SCAN}(n+2)$ with $V_{SCAN}(n-2)$ and $V_{SCAN}(n+3)$, respectively. Then, the detection time is increased from 2 H to 3 H, where 1 H presents the one horizontal time.

Figure 7 shows the comparison of proposed circuit current error rate for different resolutions in conventional driving method (detection time = 1 H) and detection time adjustable driving method (detection time = 2 H). For the conventional driving method, i.e., scan width = 2 H, and detection time = 1 H, the current error rate increases for higher resolution. For improved driving method, i.e., scan width = 3 H, and detection time = 2 H, the current error rate is almost independent of the display resolution.

Figure 7. Current error rate versus I_{OLED} for different driving schemes with various resolution formats. FHD: full-high-definition; QHD: quad-high definition; UHD: ultra-high-definition.

In addition to the length of the detection period, the actual performance of pixel circuit depends on process–voltage–temperature (PVT) factors [24,25], namely the electrical characteristic variations of poly-silicon TFT due to the fabrication process, fluctuations in the power supply, and the distribution of ambient temperature. Due to PVT effects, current-to-voltage curve will shift from the expected one. In the following, PVT influences on the pixel circuit performance with the resolution of 1920 RGB×1080 is investigated. Then, PVT performances of the proposed 7T2C circuit schematic are compared with that of the conventional 2T1C pixel circuit and a 4T1C pixel circuit, which compensates V_{TH} and mobility of the driving TFT through discharging of a mirrored TFT. Figure 8 shows the circuit and timing diagram. The merit of the 4T1C circuit schematic is that the structure is relatively simple, and the required scan and data drive waveforms are as simple as the 2T1C scheme.

Figure 8. The mirror-discharge based AMOLED pixel circuit, with (a) the pixel schematic, and (b) the timing diagram.

Due to the grain boundary and silicon orientation variations, the current-to-voltage characteristics of the poly-Si TFT tend to vary from pixel to pixel. Here, Gaussian statistical distribution is used to model the threshold-voltage of the driving TFT. Monte Carlo simulations were performed for threshold voltage variations of 20% from the nominal values for TFT of 7T2C, 2T1C, and 4T1C pixel circuits and Figure 9 shows Monte Carlo simulation results of the output current error with the sample number of 1000. The mean value of pixel current is $1\ \mu\text{A}$, and the standard deviations for the pixel current are 4.6 nA, 8.5 nA, and 151.6 nA for the 7T2C, 4T1C, and 4T1C pixel schematics, respectively. These results further confirm that the proposed pixel circuit has higher luminance uniformity and a stronger immunity to process variations than the conventional 2T1C pixel circuit and the 4T1C pixel circuit.

Figure 9. Monte Carlo analysis of the emission current with V_{TH} in a Gaussian statistical distribution when the relative error is 20%. (a) The conventional 2T1C pixel circuit, (b) the 4T1C pixel circuit, and (c) the proposed pixel circuit.

In addition, due to the metal line resistance, voltage drop along the power supply line is inevitable. For larger display panel, the IR drop effect is further deteriorated. Figure 10 shows the current error rate versus IR drop with three pixel circuits. For the conventional 2T1C pixel, abrupt current error rate is caused by IR drop. In the case V_H drops from 5 V to 3 V, the current error is reduced to 16.7% and 2.1% for the 4T1C pixel circuit and the 7T2C schematic, respectively. Thus, the proposed pixel circuit shows stronger immunity to the IR drop issue than other pixel circuits, which benefits the implementation of a large-dimension AMOLED panel. For actual products, the operating temperature for AMOLED panels is in the range of -40 degrees to 85 degrees. Figure 11 shows the OLED current versus different temperature for three pixel circuits. The current magnitude is increased by 32.1% and 25.7% with the temperature increase from -40 degrees to 85 degrees for 2T1C and 4T1C circuit. The proposed pixel circuit has much reduced temperature dependence, as the current error is reduced to 10.6% for the temperature variations.

Figure 10. Evolution of I_{OLED} error rate versus increased IR drop.

Figure 11. Evolution of I_{OLED} versus temperature.

5. Conclusions

This paper proposed a pixel circuit suitable for a narrow border display, which can compensate for threshold voltage non-uniformity and IR drop, and increase the detection time by increasing the signal width at high resolution. The pixel circuit requires mono-type scanning signals, which benefits simplification of the external driving circuit for narrow border displays. The conventional V_{DD} line is replaced by the scanning line to suppress the leakage current for the initial stage. The proposed pixel circuit has a good compensation effect and stability for temperature variations, the simulation results show that the current variation is reduced to 2.1% for the supplied power reduced from 5 V to 3 V, and the current variation is as low as 10.6% for temperatures from -40 degrees to 85 degrees.

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