

## Article

# A 12-Bit 200 MS/s Pipelined-SAR ADC Using Back-Ground Calibration for Inter-Stage Gain

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Received: 18 February 2020; Accepted: 17 March 2020; Published: 19 March 2020



**Abstract:** A 12-bit 200 MS/s pipelined successive-approximation-register (SAR) analogue-to-digital-converter (ADC) implemented in 40 nm CMOS is presented. Such an ADC consists of two asynchronous SAR ADCs and a dynamic amplifier, which consumes a static power of 1.2 mW (the total power is 8 mW) and occupies an area of 0.046 mm<sup>2</sup>. The inter-stage gain is affected by the parasitic capacitance in SAR ADCs as well as the gain of the dynamic amplifier, which is variable with respect to process-voltage-temperature (PVT). A background calibration of the inter-stage gain is proposed to adjust the inter-stage gain and to track the PVT variables. The measurement results show that, with calibration, the spurious-free-dynamic-range (SFDR) and signal-to-noise-and-distortion-ratio (SINAD) can be improved from 68 dB and 61 dB to 78 dB and 63 dB, respectively. The dynamic performance was stable under different VT conditions.

**Keywords:** pipelined-SAR ADC; background calibration; inter-stage Gain; dynamic amplifier

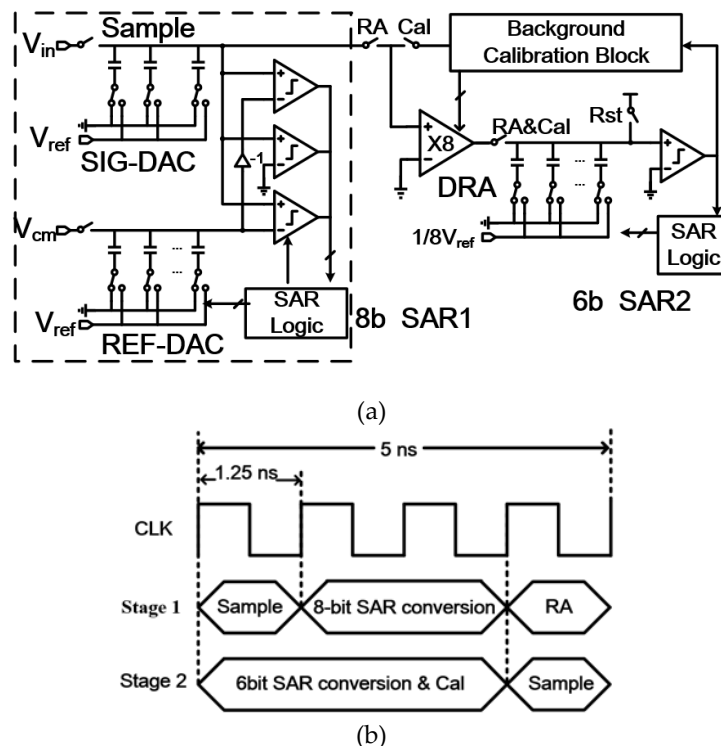
## 1. Introduction

Successive-approximation-register (SAR) ADC is quite powerful and area-efficient due to its mostly digitized structure [1,2], which is scalable with respect to process development. Nonetheless, the bit-by-bit operation sequence limits its sampling rate and the comparator noise confines the overall signal-noise-ratio (SNR) [3,4]. The traditional pipelined structure has a speed merit, but the multiple amplifiers consume much power. Recently, pipelined-SAR structure has obtained much attention because it combines both the merits of pipelines and SAR ADCs [5–17]. As in traditional pipelined ADCs, two SAR ADCs connected by a residue amplifier (RA) can work concurrently. The pipelined-SAR ADC usually employs merely one amplifier, since each SAR ADC can resolve more bits than in a conventional pipelined structure with flash sub-ADC. The RA can reduce the input referred noise of the second SAR ADC, thus greatly relaxing its design burden and decreasing its power. A dynamic residue amplifier (DRA) is usually employed due to its simple structure and zero static power [15–18]. In a dynamic amplifier, the output voltage swing needs to be kept in a small range to obtain relatively high linearity. Fortunately, in a pipelined-SAR ADC, the residue voltage of the first stage (which is also the input of the dynamic amplifier) is usually smaller than the pipelined counterpart. Further, the integration process assists to filter the amplifier noise. The side effect of an open-loop structure of a DRA is also obvious. Its gain is inaccurate and variable due to PVT changes. Calibration schemes have often been employed in pipelined-SAR ADCs to remedy this issue. In [19], a dither signal was injected into the key path to obtain a bit-weights background. Nevertheless, the calibration converged slowly due to large signal-dependent interferences. In [20], the gain was adjusted according to the induced gain-mismatch error, but this was unsuitable for dynamic amplifiers that work under a foreground mode. In [17], the gain of the dynamic amplifier was determined by capacitor ratios, which were stable under various PVT conditions but at the cost of a large analog overhead.

In this work, a simple but efficient background scheme is proposed to adjust inter-stage gain and obtain the proper value. On the other hand, this calibration scheme works in the background, so as to track PVT variations. It adds only a small analog overhead. In Section 2, the ADC architecture and timing relationship are depicted. Section 3 provides the principle and circuit implementation of the background calibration. The measurement results are given in Section 4. Finally, a conclusion is drawn in Section 5.

## 2. Architecture of the Proposed ADC

The block diagram is shown in Figure 1a, in which an 8-bit front-end SAR (SAR1) and 6-bit back-end SAR (SAR2) are connected by the dynamic residue amplifier (DRA). The residue of SAR1 is quite small due to the 8-bit quantization, which confines both the input and output range of the DRA, thereby improving its linearity. Unlike traditional SAR ADC, the signal sampling and residue amplifying phases are included in SAR1, thus decreasing its conversion time interval. Herein, we employ a 2-bit/cycle structure as the first stage to double the conversion speed [3]. The SAR1 includes signal digital-to-analogue converter (SIG-DAC) and reference digital-to-analogue converter (REF-DAC). The timing diagram is illustrated in Figure 1b. The input clock frequency is 800 MHz, which is employed to generate several 200 MHz clock phases for sampling, conversion and residue amplification. As illustrated in Figure 1b, the input clock period is 1.25 ns and it takes four cycles to complete one conversion, in which one cycle is allocated to signal sampling, two cycles are allocated to 8-bit asynchronous SAR1 and one cycle is allocated to the DRA. Since SAR2 takes three cycles (3.75 ns) to finish one conversion, a traditional asynchronous 1-bit/cycle structure can meet the speed demand. The background calibration of the inter-stage gain is started right after the 6-bit SAR conversion.



**Figure 1.** (a) Block diagram of the proposed ADC; (b) timing diagram of the proposed ADC.

The reference voltage of SAR1 ( $V_{ref1}$ ) is the power supply (1.1 V). Hence, SAR1 generates a residue that is confined to  $\pm 4.3$  mV. A 2-bit redundancy (12.9 mV) is included to tolerate various dynamic errors, and finally 12-bit data are acquired. Originally, 2-bit redundancy and 8-bit SAR1 requires that the DRA provide 64x gain. To confine the output range of the DRA and achieve high linearity, only 8x

gain is allocated to the DRA. Accordingly, the reference voltage of SAR2 ( $V_{ref2}$ ) is  $1/8 V_{ref1}$ . The offsets of the three comparators of SAR1 ADC occupy some inter-stage redundancy. The offset mismatch of the DRA and comparators is amplified by the inter-stage  $8\times$  gain, which can easily cause the residue output to exceed the redundancy range. To remedy this issue, the offsets of comparators and the DRA are all foreground calibrated [10]. The offset of the comparator in SAR1 is calibrated by resetting the inputs to a common mode voltage. The comparator output is feedback to a DAC. The offset voltages of the residue amplifier and the comparator in SAR2 are calibrated together in a similar way. Finally, 2-bit redundancy is employed to tolerate the dynamic errors such as reference settling and kick-back effects. The capacitor mismatches between the reference DAC and signal DAC are also corrected by the 2-bit redundancy.

### 3. Background Calibration of the Inter-Stage Gain

$V_{FS1}$  and  $V_{FS2}$  are the signal ranges of the two SAR ADCs, respectively.  $M$ ,  $R$  and  $G$  are on behalf of the SAR1 bit, the redundancy bit and the inter-stage gain. Ideally, these variables should meet the below relationship:

$$G \times \frac{V_{FS1}}{2^{M-R}} = V_{FS2} \quad (1)$$

If  $G$  is larger than the ideal value, missing analog information occurs. If  $G$  is smaller, missing codes occur [20]. In both cases, obvious nonlinearity is induced. On the other side,  $G$  of the DRA is changeable due to PVT variations. As a result, calibration for accurate  $G$  should be in real-time. The key idea herein is to compare the left side to the right side in Equation (1). The comparison result is fed to the DRA so as to adjust the gain until they are almost equal.

As illustrated in Figure 2, only the DRA and part of SAR2 related to the proposed calibration are shown. The corresponding timing diagram is depicted in Figure 3. Compared to the traditional pipelined-SAR ADC, some switches and phases are added. The DRA is disconnected to SAR1 after its residue voltage is amplified and sampled by the DAC of SAR2 ( $C_{DAC2}$ ). Then, SAR2 conversion begins. Afterward, its DAC is reset to the power supply. The DRA starts again to amplify the calibration voltage ( $V_{calp} - V_{caln}$ ) to obtain  $G \times (V_{calp} - V_{caln})$ , which is also sampled by the  $C_{DAC2}$ . The bottom plate of  $C_{5a}$  is switched from  $V_{ref2}$  to ground. Finally, the comparator works, and the result is fed to a bi-directional shift register (BDSR) to adjust  $G$ . Since the switching method of SAR2 is a split structure [21],  $C_{5a}$  is a quarter of the total capacitor of  $C_{DAC2}$ . Herein,  $V_{calp} - V_{caln}$  is set at  $V_{FS1}/2^9$  and  $(M - R)$  equals 6. The calibration voltage ( $V_{calp} - V_{caln}$ ) is generated by the reference voltage  $V_{ref1}$  and a resistor array. The resistor ratio makes the calibration voltage stable. The mismatch of the resistors affects the calibration accuracy slightly. A Monte Carlo simulation is performed using 1000 runs, as shown in Figure 4. The mismatch of the resistor is 1%, and the induced three-sigma value of the deviation of  $V_{calp} - V_{caln}$  is 120  $\mu V$ , which is smaller than half of the least-significant-bit (LSB) of the whole ADC.

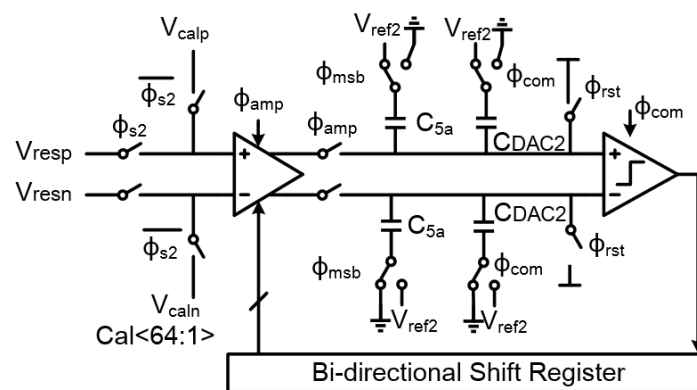


Figure 2. Circuit schematic of the background calibration.

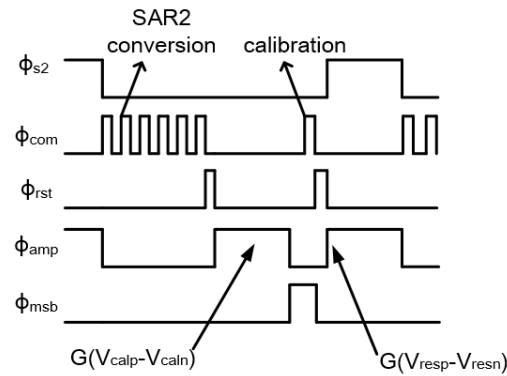


Figure 3. Operation timing of the background calibration.

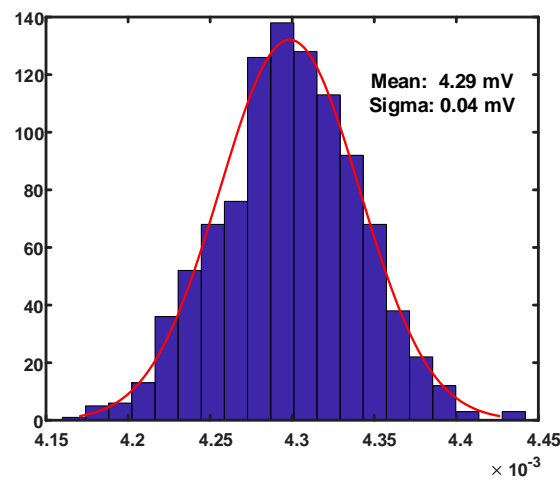


Figure 4. Monte Carlo simulation of the calibration voltage due to the mismatch of the resistors.

The comparison result is equivalent to Equation (1), which can be derived from

$$\begin{aligned} G \times \frac{V_{FS1}}{2^{M-R}} - V_{FS2} &\Leftrightarrow \\ G \times (V_{calp} - V_{caln}) - V_{FS2}/8 & \end{aligned} \quad (2)$$

As a result, when the comparison result is 1, it means  $G$  is larger than the ideal value, and vice versa. The DRA adopts a traditional structure, except that we add a pair of capacitor arrays (64 capacitor units) at nodes 1 and 2. The common-mode detector determines when the DRA is cut off by employing the signal  $V_{cb}$ . When the comparison result is 1 (or 0), it means  $G$  is larger (smaller) than the ideal value. One of the calibration capacitors is then disconnected (added), which can decrease (increase)  $G$  by shortening (enlarging) the integrating time. The gain of this cascode DRA is

$$G = \frac{2(V_{dd} - V_{cm})}{V_{gt}} \left( 1 + \frac{C_1}{C_2} \right) \quad (3)$$

where  $V_{dd}$  and  $V_{cm}$  are determined at the system design level.  $V_{gt}$  is the over-driving voltage, which is 100 mV–200 mV, thereby keeping the transistors in a saturation state and ensuring enough voltage swing.  $C_1$  is the sum of parasitic capacitance and the calibration capacitance at nodes 1 and 2 while  $C_2$  is the parasitic capacitance and the sampling capacitance of SAR2 (Figure 5).



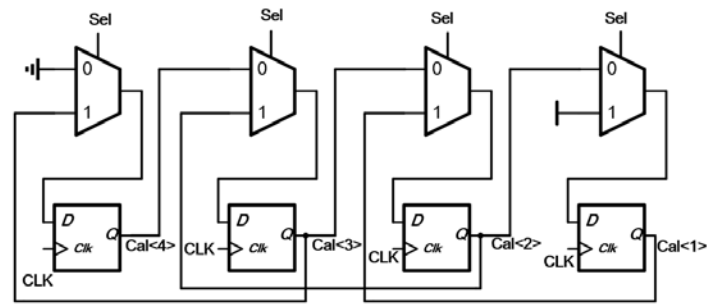


Figure 7. The 4-bit example of the bi-directional shift register (BDSR).

#### 4. Measurement Results

The pipelined-SAR ADC with the proposed background calibration is fabricated on a 40-nm low power (LP) process. The chip photo and its layout graph are shown in Figures 8 and 9, respectively, which occupies about  $270 \times 170 \mu\text{m}$ . The total power consumption of the ADC core is about 8 mW, including the clock generators.

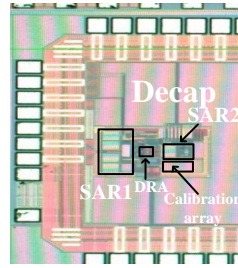


Figure 8. Chip photo of the ADC.

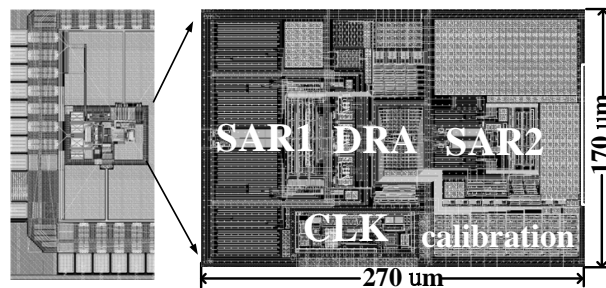


Figure 9. Layout of the proposed ADC.

With 75 MHz input, the signal-to-noise-and-distortion-ratio (SINAD) is improved from 61 dB to 63 dB, and the SFDR is improved from 68 dB to 78 dB, using the proposed calibration, as shown in Figures 10 and 11, respectively. The effective-number-of-bits (ENOB) is also increased. The gain deviation causes large integral-nonlinear (INL) degradation at several discontinuities due to the pipelined-SAR structure. After calibration, differential-nonlinear (DNL) is improved from 0.9 (least-significant-bit) LSB/−0.5LSB to 0.7LSB/−0.3LSB, and INL is improved from 1.9LSBs/−1.89LSBs to 1 LSB/−1.2LSBs, as illustrated in Figures 12 and 13, respectively.

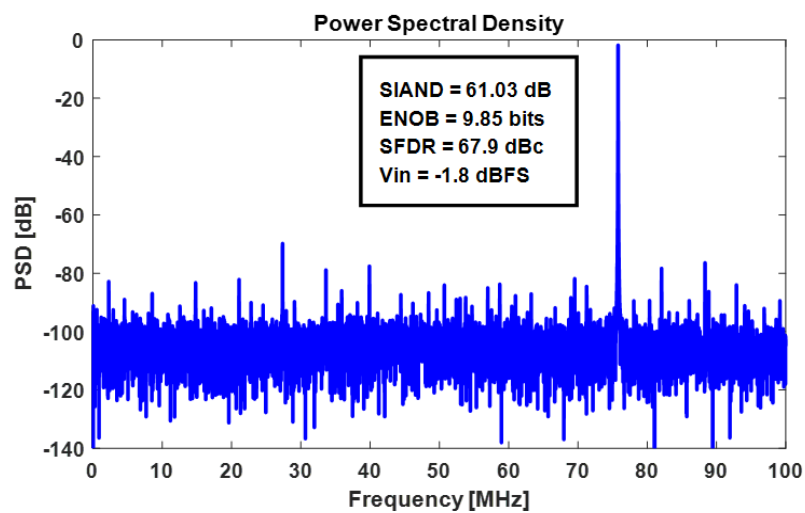


Figure 10. Dynamic performances before calibration.

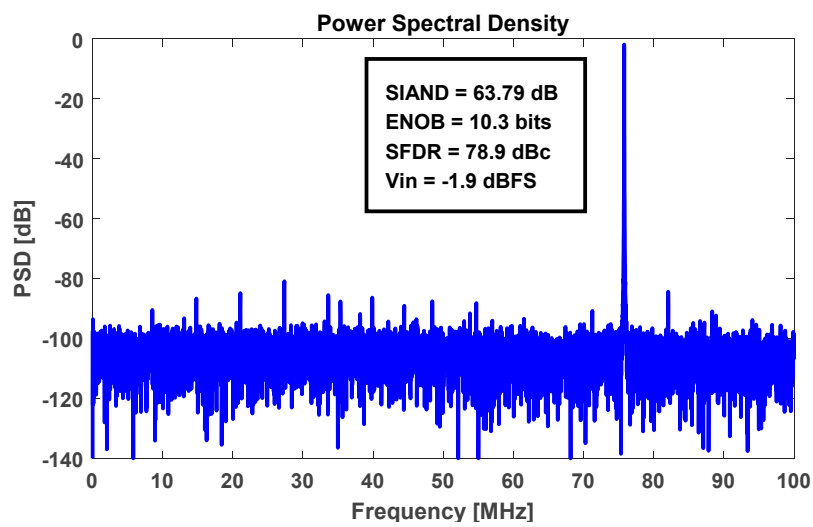


Figure 11. Dynamic performances after calibration.

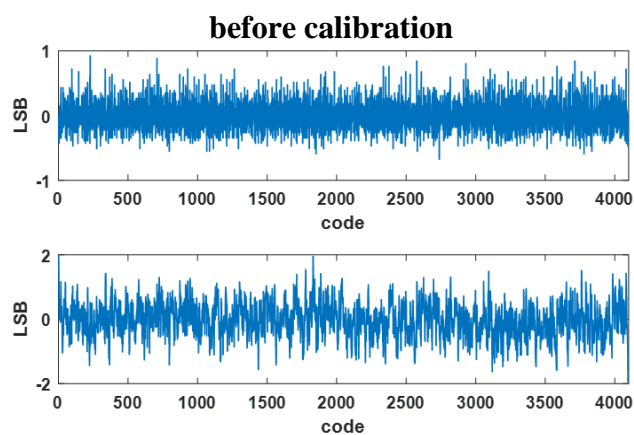


Figure 12. DNL and INL before calibration.



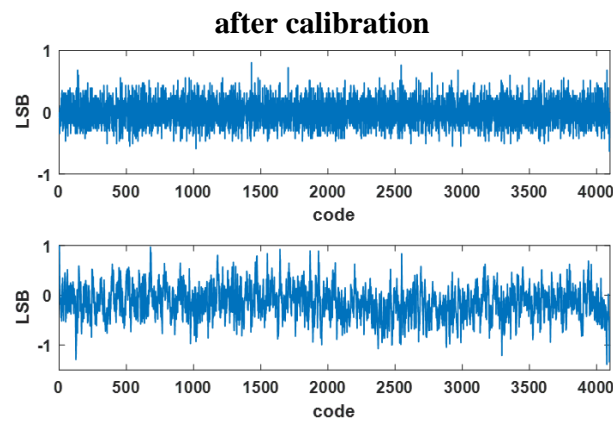


Figure 13. DNL and INL after calibration.

To verify the calibration in real-time, the chip was measured under different power supplies and temperatures. It can be seen that the dynamic performance keeps stable under a wide range of conditions. The SFDR value changed about 1 dB, and the SINAD changed by nearly 0.3 dB under a 1 to 1.2 V supply, as seen in Figure 14. From 0 to 80 °C, the SFDR varied about 2.4 dB, while the SINAD changed about 1.5 dB, as in Figure 15. The Walden figure of merit (FOM) could achieve 31.7 fj/conv-step, which is quite competitive.

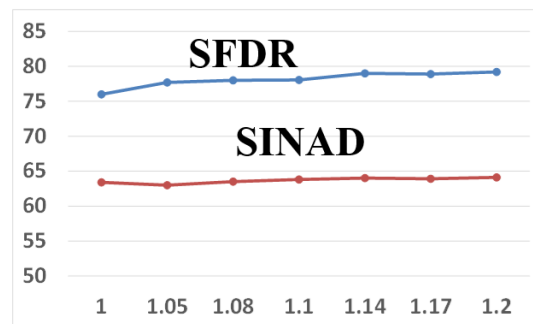


Figure 14. Performances under different supplies.

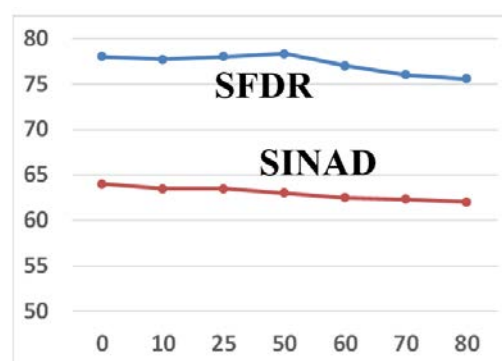


Figure 15. Dynamic performances under different temperatures.

In Table 1, the indexes are compared with the state of art works. Compared to [20], this calibration operates in the background and can converge faster than the method in [19], since no dither is injected. The dynamic performance of [17] probably behaved better, and could also converge quite fast without any dither injection. Nonetheless, it consumed large analog overhead. Comprehensively, the proposed calibration can track PVT variations and greatly improve dynamic performance with small overhead.



**Table 1.** Performance of the proposed ADC and comparison with previous studies.

	[7]	[9]	[20]	This Work
Process (nm)	65	40	65	40
Supply (V)	1.2	1.8	1.2	1.1
Resolution (bits)	12	12	12	12
Power (mW)	6.23	4.96	6	8
Sampling rate (MHz)	330	160	180	200
SFDR (dB)	83.4	86.9	76	78.9
SINAD (dB)	63.5	65.3	63	63.7
Process-voltage-temperature stable	Yes	Yes	No	Yes
Area (mm <sup>2</sup> )	0.08	0.042	0.068	0.0459
Figure of merit (fj/conv-step)	15.4	20.6	36.7	31.7

## 5. Conclusions

A 12-bit 200 MS/s pipelined-SAR ADC implemented on 40 nm CMOS process was presented. This ADC reuses the comparator of SAR2 to obtain information of the adjustment direction of G in the dynamic amplifier, thus avoiding complex digital calibration or large overhead. The proposed calibration operated in the background and improved SFDR and SINAD by 78.9 and 63.7 dB, respectively. This improvement was also stable under various conditions, and the total power consumption was 8 mW, achieving a 31.7 fj/conv-step Walden FOM.

**Author Contributions:** Conceptualization, J.W. (Junjie Wu) and J.W. (Jianhui Wu); Data curation, J.W. (Junjie Wu) and J.W. (Jianhui Wu); Funding acquisition, J.W. (Junjie Wu) and J.W. (Jianhui Wu); Investigation, J.W. (Junjie Wu) and J.W. (Jianhui Wu); Methodology, J.W. (Junjie Wu) and J.W. (Jianhui Wu); Resources, J.W. (Junjie Wu) and J.W. (Jianhui Wu); Writing—original draft, J.W. (Junjie Wu) and J.W. (Jianhui Wu); Writing—review & editing, J.W. (Junjie Wu) and J.W. (Jianhui Wu). All authors have read and agreed to the published version of the manuscript.

**Funding:** This work is supported by the National Natural Science Foundation of China under project number No.61401090 and No.61704088.

**Conflicts of Interest:** The authors declare no conflict of interest. The funders had no role in the design of the study.

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