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New Radiation-Hardened Design of a CMOS Instrumentation Amplifier and its Tolerant Characteristic Analysis

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Abstract: A radiation-hardened instrumentation amplifier (IA) that allows precise measurement in radiation environments, including nuclear power plants, space environments, and radiation therapy rooms, was designed and manufactured, and its characteristics were verified. Most electronic systems are currently designed using silicon-based complementary metal-oxide semiconductor (CMOS) integrated circuits (ICs) to achieve a highly integrated low-power design. However, fixed charges induced in silicon by ionization radiation cause various negative effects, resulting in, for example, the generation of leakage current in circuits, performance degradation, and malfunction. Given that such problems in radiation environments may directly lead to a loss of life or environmental contamination, it is critical to implement radiation-hardened CMOS IC technology. In this study, an IA used to amplify fine signals of the sensors was designed and fabricated in the 0.18 μm CMOS bulk process. The IA contained sub-circuits that ensured the stable voltage supply needed to implement system-on-chip (SoC) solutions. It was also equipped with special radiation-hardening technology by applying an I-gate n-MOSFET that blocks the radiation-induced leakage currents. Its ICs were verified to provide the intended performance following a total cumulative dose of up to 25 kGy(Si), ensuring its safety in radiation environments.

Keywords: radiation-hardening technology; CMOS bulk process; integrated circuit (IC); instrumentation amplifier (IA); total cumulative dose

1. Introduction

Silicon-based complementary metal-oxide semiconductor (CMOS) electronic devices used in environments exposed to radiation, such as in nuclear power plants, space environments, and radiation therapy rooms, end up being subject to the total ionizing dose (TID) effect, which is caused by radiation accumulated over a long period of time. When a MOS structure is exposed to radiation, electron hole pairs are generated in the silicon dioxide by ionization phenomena. Holes, with low mobility, then become trapped at the interface between the silicon dioxide and the silicon oxide. These trapped holes are referred to as fixed charges because they are positive. It is worth noting that the radiation-induced generation of fixed charges in n-type metal-oxide semiconductor field effect transistors (n-MOSFETs) can cause a leakage current between the source and the drain. If this happens, the performance of the affected device can degrade, thereby causing significant damage, such as in the malfunction or failure of the entire circuit system [1–5]. Notably, when such problems occur in instrumentation amplifiers (IAs) that are typically used in safety, control, and instrumentation

electronic systems, it becomes difficult to accurately measure sensor outputs that indicate the status of nuclear power plants, such as pressure, temperature, and radiation doses. This could lead to the failure of safety-related systems, thus causing disastrous consequences, including radiation exposure or nuclear disasters. To prevent such incidents, there is a growing need for radiation-hardened electronic device technologies [5–7]. Active research on radiation-hardened integrated circuits (ICs) is currently underway, and relevant technologies have been implemented and used in various approaches and applications, for example, involving screening techniques, metal shielding, and radiation hardening at the process/circuit/device level. Each approach has its own advantages and disadvantages, and each field of application may require different methods and approaches [8].

With the recent trend toward smaller electronic systems, the number of transistors contained in a specific area is constantly increasing [9]. Device-level radiation-hardening technology is considered to be more efficient in this regard than process-level technology, which requires a great deal of time and cost, or circuit-level technology, which has its own problems, such as increased area and reduced operating speed [10–12]. Among the device-level radiation-hardening technologies, the layout modification method is an approach to developing a device that can shut off the radiation-induced leakage current by modifying the standard n-MOSFET layout structure. The method can be provided by a process fabrication company, and does not require any additional processes because existing commercial lines are used. ELT, DGA, ringed-source, and H-gate structures are prime examples of radiation-hardened n-MOSFET devices in which the layout modification method has been applied [13–15]. Among them, the I-gate n-MOSFET is the most suitable structure for application-specific integrated circuit (ASIC) design because, unlike other structures, the modification of the layout structure does not cause any channel size changes. Additionally, its radiation-hardened performance has already been verified with a total cumulative dose of up to 25 kGy [16].

Figure 1 depicts the structure of a commercial n-MOSFET and its cross-sectional diagram. Here, the path of the leakage current generated by the radiation-induced fixed charges is illustrated [17]. In the present study, the layout modification technology was applied using the I-gate structure. By improving the resistance to radiation from the CMOS unit device and designing the circuits by using it, we achieved the radiation hardening of ICs.

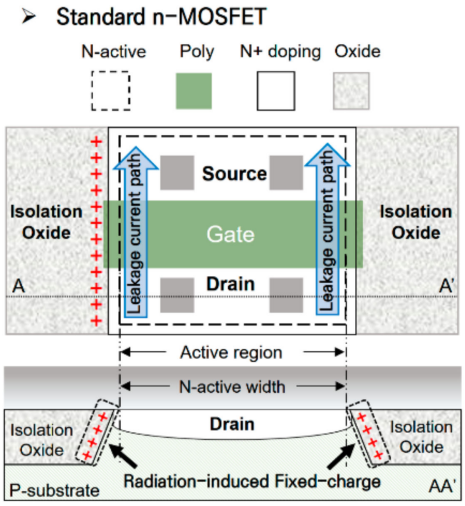


Figure 1. Standard CMOS bulk process: The structure of an n-MOSFET and the path of radiation-induced leakage current.

An IA composed of three op-amps and passive devices was designed in such a way that it could be manufactured in the 0.18 μm CMOS bulk process. The IA was radiation-hardened designed so that it could operate even in radiation environments. The applied amplification factor was 3800. This means that the designed circuit is capable of amplifying a minute signal of 10 μV to levels of up to 38 mV. Additionally, in addition to the main IA circuit, sub-circuits, including bandgap reference

(BGR) circuits, low drop out (LDO) regulators, and bias circuits, were included to ensure the stable bias supply needed to implement system-on-chip (SoC) solutions. Each sub-circuit was radiation-hardened.

2. Proposed Radiation-Hardened Instrumentation Amplifier Implementation

2.1. Standard Instrumentation Amplifier Design

An IA is manufactured for a specific purpose and used to measure or amplify signals in a precise and accurate manner. The technology is mainly used for measuring bio-signals or the minute signals of various sensors, such as in electroencephalography (EEG), electrocardiography (ECG), and electromyography (EMG), although its scope of applications can be extended to various fields [18].

Figure 2 presents a block diagram of the entire IA system. To begin with, the BGR circuit serves to generate a constant current or voltage for the process, voltage, temperature (PVT), that is, process, voltage, and temperature, and apply them to the LDO terminal. The LDO provides a stable voltage supply to the bias circuit, the main circuit (IA), and the hysteresis comparator. Following that, while bias is being applied, the main circuit receives minute signals as inputs and amplifies them. Finally, the one-bit comparator converts the amplified analog signals into digital signals for processing [19].

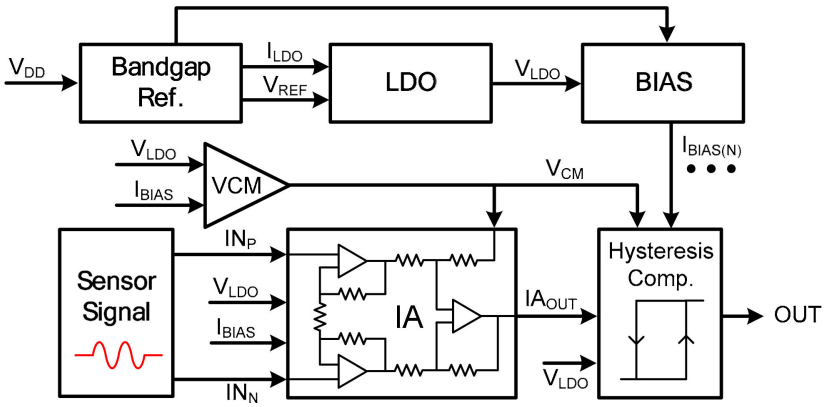


Figure 2. Block diagram of the entire IA system.

Figure 3 presents the circuit diagram of the IA. The IA circuit removes common interference signals measured at the two input terminals while serving to amplify differential signals. Basically, the IA circuit has a high input impedance and high common-mode rejection ratio (CMRR). The circuit detects the potential difference between the two input signals using three operational amplifiers and amplifies the signals to generate output signals. Eventually, the amplification factor of the IA is determined by the ratio of R2 to R1 and the ratio of R4 to R3 [20]. In the present study, the IA was designed to have a gain factor of nearly 3800. Table 1 shows design specifications of the IA.

Table 1. Design specifications of the IA.

Param.	Instrumentation Amplifier Spec.
Supply voltage [V]	3.3
Reference voltage [V]	1.23
LDO voltage [V]	1.8
Amplification factor	3800

The permissible error range is set to ±5%.

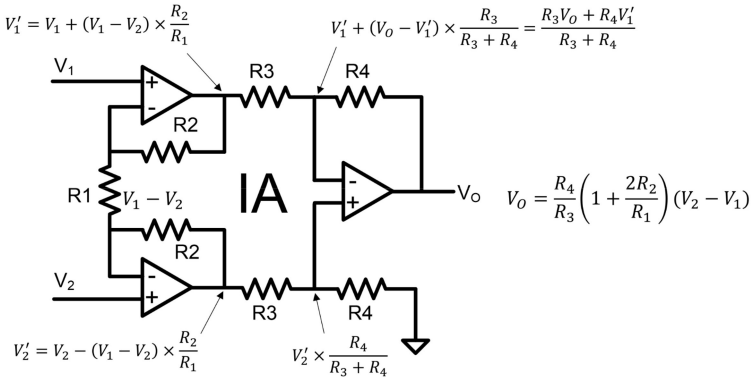


Figure 3. IA circuit diagram.

Following that, the IA process design was implemented using the SKhynix/Magnachip 0.18 μm CMOS commercial process. Figure 4 shows a top layout drawing for chip fabrication. The total area of the fabricated chip was 476.28 × 452.78 μm^2, and the standard ASIC design method was used [21]. At a supply voltage of 3.3 V of the power supply generates an output voltage of 1.23 V through the BGR, which represents the reference voltage (V_{REF}), insensitive to the PVT. The LDO then receives V_{REF} as an input and generates a stable output voltage (V_{LDO}) of 1.8 V. V_{LDO} was designed in such a way that it can be applied to each of the system's circuits as a supply voltage, thereby enabling the IA system to function.

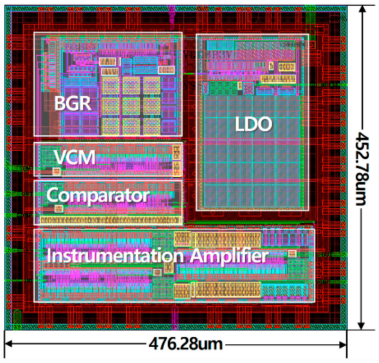


Figure 4. 2D layout drawing of the 0.18-μm CMOS process-based IA.

When preparing layout drawings in the ASIC design process, parasitic components can be generated in different ways depending on various factors, including device arrangement and wiring connection. Given that a post-layout simulation was applied in this study, it is possible to identify each operation of the chip before it is fabricated and, thus, determine in advance whether each operation will be able to meet the desired performance [22,23]. Figure 5 presents the results of the standard IA post-layout simulation. As shown in Table 2, when V_{REF} was 1.21 V, and V_{LDO} was 1.78 V, the IA input increased 3640 times from the input level of 100 μV_{pp} to 364 mV. Simply put, the system was verified to operate normally within the allowable error range.

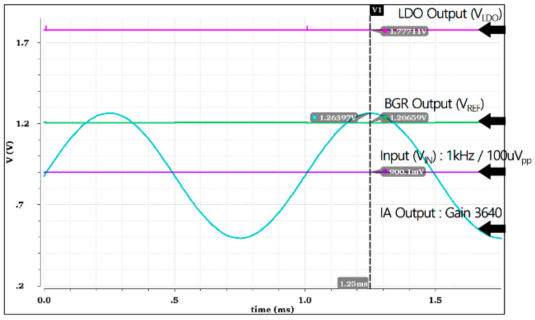


Figure 5. Results of the standard IA post-layout simulation.

Table 2. Summary of the post-layout simulation results of the IA.

Param.	IA Spec.	Post-layout Sim.
Supply voltage [V]	3.3	3.3
Reference voltage [V]	1.23	1.21 (98.4%)
LDO voltage [V]	1.8	1.78 (98.9%)
Amplification factor	3800	3640 (95.8%)

2.2. Proposed Radiation-Hardened Instrumentation Amplifier Design

To implement the IA radiation hardening using the standard commercial process, the layout modification technology was applied. Figure 6 shows a structural diagram of the I-gate type n-MOSFET. By modifying the standard n-MOSFET structure, which is vulnerable to radiation, into the I-gate type, the n+ region was separated from the isolation oxides where fixed charges are trapped, and the threshold voltage increased through the P+ doping process. By doing so, the radiation hardening of the minimum unit transistors that constitute the electronic circuit was achieved. Additionally, the application of the I-gate type n-MOSFET complemented the structural limitations of the existing radiation-hardened devices. Meanwhile, the issue of varying output characteristics depending on the source and drain selection was resolved by maintaining the symmetrical structure of the source and drain. In addition, the device operation speed issue was improved by having a relatively low gate capacitance. Notably, even though the layout structure was modified to shut off the path of the radiation-induced leakage current, the intrinsic characteristics of the device remained almost the same because the n-active region was kept intact [16]. Table 3 shows a comparison of the characteristics of conventional bulk process radiation-hardened n-MOSFETs [13,14] and the I-gate n-MOSFET. As shown in Table 3, the n-active region preservation of the I-gate n-MOSFET means that the channel size of the transistor used in the simulation and the transistor to be fabricated is the same. Therefore, the post-simulation is more reliable than the conventional radiation-hardened n-MOSFETs, and new channel size re-modeling is not required. In addition, it has the advantage of eliminating the bird's beak effect that occurs in the local oxidation of silicon (LOCOS) bulk process.

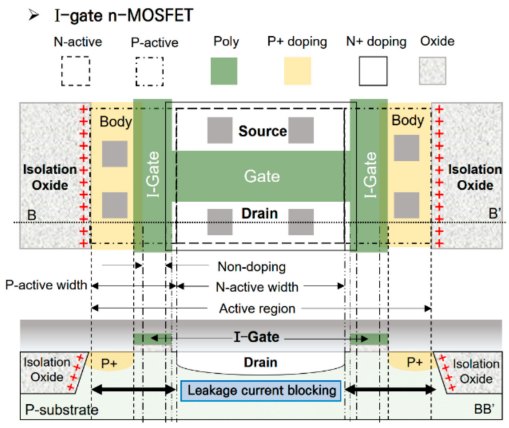


Figure 6. Structure of the CMOS bulk process-based I-gate type n-MOSFET.

Table 3. Comparison of the characteristics of conventional bulk process radiation-hardened n-MOSFETs and the I-gate n-MOSFET.

Pram.	Radiation-hardened n-MOSFETs※a		
	ELT [13]	DGA n-MOSFET [14]	I-gate n-MOSFET [16]
Radiation hardness (kGy)	300	5	**23**
Symmetry structure	N	A	**A**
Gate capacitance	High	Middle	**Low**
Size re-modeling (W/L)	N^R	N^R	**A^R**
Bird's beak elimination	U	U	**A**
N-Active region preservation	N	N	**A**

※a Characteristics of radiation-hardened n-MOSFETs; A: Applicable, N: Not available, A^R: Not required, N^R: required, U: Unknown.

Figure 7 shows the graphs that represent the electrical characteristics of the standard n-MOSFET and the radiation-hardened n-MOSFET with respect to an increasing cumulative radiation dose (up to 23 kGy(Si)). When the gate voltage in the standard n-MOSFET was zero (i.e., the device was turned off), the leakage current increased to 16.2 μA with the increasing cumulative dose, indicating the occurrence of radiation-induced damage [24]. In contrast, the I-gate type n-MOSFET was verified to provide radiation-resistance performance, meaning the electrical characteristics of the device were maintained without an increase in leakage current.

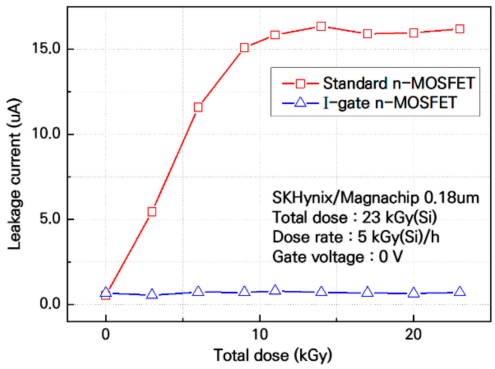


Figure 7. Measurement results of leakage current with respect to the cumulative radiation dose in the standard n-MOSFET and the I-gate n-MOSFET.

To prepare drawings of the radiation-hardened IA layout, the thousands of n-MOSFET structures contained in the electrical circuit must be converted into the I-gate type. Given that these n-MOSFET structures differed in size and finger number, the I-gate structure was extended, or the modification was made to the extent that the radiation-hardened characteristics were maintained. The device arrangement or the status of wiring connections was also considered. Regardless, the I-gate structure could be simply applied to the proposed radiation-hardening design due to its excellent structural expandability and flexibility when compared with other structures.

Radiation hardening presently requires that the structure of each unit device cell in the commercial process be modified and extended. But in this study, such device cells were verified to be radiation-hardened devices, providing radiation-hardened performance. Provided that these device cells can be used as radiation-hardened unit cells in the device manufacturing process going forward, designing radiation-hardened ICs will become much easier.

Figure 8 presents a layout drawing of the radiation-hardened IA. The arrangements of each sub-circuit and the main circuit remained the same, but the area was slightly increased to 476.28 × 464.28 μm^2 due to the additional layers added to implement radiation hardening. Because there was no channel size change of each I-gate n-MOSFET structurally, it was possible to apply the

post-layout simulation [22]. As shown in Figure 9, the BGR voltage was 1.206 V, and the LDO voltage was 1.777 V, and the output peak voltage was increased 3729 times to 1.2729 V. These simulation results confirm that the developed IA exhibits almost the same characteristics as the standard IA, despite the application of the radiation-hardening technology.

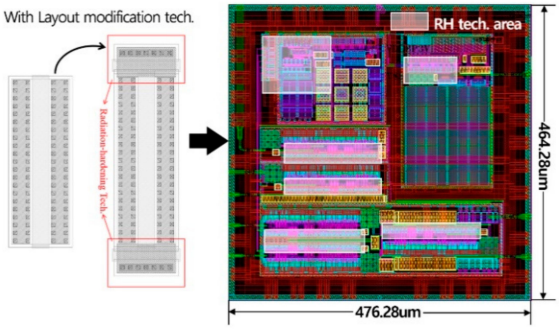


Figure 8. 2D layout drawing of the radiation-hardened IA.

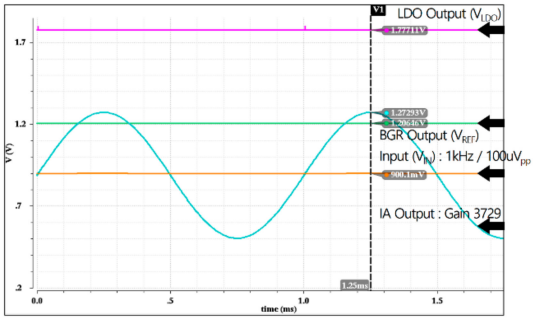


Figure 9. Post-layout simulation results of the radiation-hardened IA.

3. Test Result and Analysis of TID Effects of Radiation-Hardened IA

3.1. Irradiation Test of TID Effects of the Radiation-Hardened And Standard IAs

The designed IA chip was tested with regard to total ionizing dose (TID) effects at the high-level gamma-ray irradiation facility of Advanced Radiation Technology Institute (ARTI) in Jeongeup, North Jeolla Province. The applied radiation source was cobalt-60, and the testing was conducted at a dose rate of 5 kGy/h until the total cumulative dose reached 25 kGy. The test procedures were referenced to globally recognized procedures, including the MIL-STD-883H 1019.8 of the United States Department of Defense and the ESA/SCC Basic Specification No. 22900 of the European Space Agency [25,26]. To verify the functions of the concerned IC and measure its electrical characteristics in real time with respect to the cumulative radiation dose, the applied measurement system was divided in two: The control room where bias signals were applied and measured, and the irradiation room in which the cumulative dose applied to the IC chip by the radiation source was examined. The IC chip in the irradiation room was connected to the measurement equipment in the control room using a 25 m data cable. The standard IA and the radiation-hardened IA were tested using the same measurement methods and experimental conditions.

Based on the actual measurements, the radiation-induced damage in the standard IA and the radiation-resistance characteristics of the radiation-hardened IA were examined and analyzed. Table 4 summarizes the TID test environment, measurement methods, and bias conditions.

Table 4. Summary of the TID test and evaluation environment for IA chips.

Test Environment of TID Effects		
Test facility specifics	Facility	High-energy gamma-ray irradiator
	Manufacturer	MDS Nordion, Canada
	Radiation source	Cobalt-60
	Radiation shield	Water
	Capacity	490 KCi
	Temperature (TA°C)	25
Measurement Conditions	Test circuit	Instrumentation amplifier Bandgap reference circuit Low dropout regulator
	Dose rate (kGy/h(Si))	5
	Total dose (kGy(Si))	25.8
	Performance	Output duty, Average voltage
	Test method	Real-time using 25 m cable
	Bias condition	Supply voltage: 3.3 V Input: sine/1 kHz/10 mV_{PP}

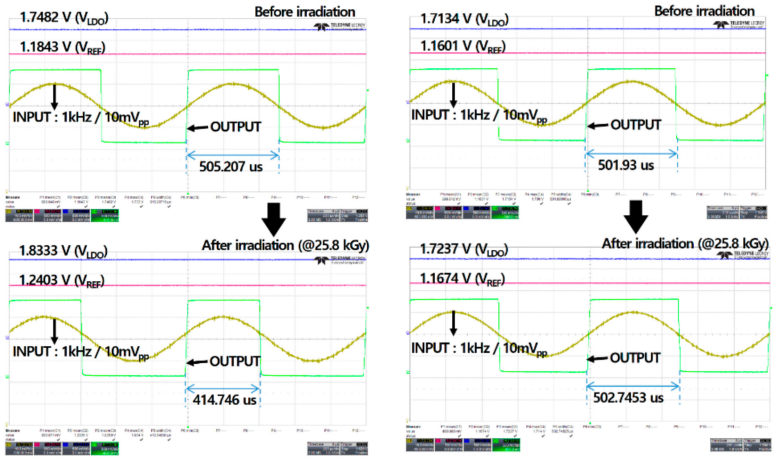
The ASIC design-based IA fabricated by the 0.18 μm CMOS process was tested for radiation-induced damage in accordance with the measurement environment and bias conditions set for the TID test and evaluation procedures. After being irradiated until the total cumulative radiation dose reached 25.8 kGy(Si), the electrical characteristics of the IA, BGR, and LDO were monitored in real time. Here, the input voltage of 100 μV_{pp} that was selected and used in the simulation was impossible to identify due to noise from the oscilloscope and power supplier and, thus, the input voltage was set to 10 mV_{pp} in the tests.

As the output voltage was supposed to be increased nearly 3800 times from the input voltage, it was confirmed that output pulse signals with a maximum voltage of 1.8 V were generated Eventually, it was predicted that if the tested IA ended up being damaged by radiation, it would be impossible for the IA to achieve full swing at common voltage 0.9 V (VDD/2) and, thus, the duty ratio of the output pulse signals would also change.

According to the TID test results, before the irradiation treatment, the BGR voltage was 1.1843 V, and the LDO voltage 1.7482 V; both were within the allowable error ranges. Additionally, the width of the output pulse was 505.207 us, and the duty ratio was 50.5%, indicating that the device was properly operating. After the irradiation treatment, the BGR voltage was increased by 0.056 V to 1.24 V, and the LDO voltage was increased by 0.085 V to 1.833 V; both were still within the allowable error ranges. However, the changes in the bias voltage caused the reference voltage within the IA (V_{CM}) to change, and they overlapped with the radiation-induced offset generated in the operational amplifiers contained in the IA, giving rise to damage. As shown in Figure 10a, the width of the output pulse changed to 414.746 μs and, thus, the duty ratio decreased to 41.5%. Such damage hinders the IA from full swing of its output signal, making it difficult to precisely measure and amplify minute signals in radiation environments.

To prevent such radiation-induced damage, as frequently observed in the standard IA, the radiation-hardening design was implemented. The TID evaluation results confirmed that the radiation-hardened IA maintained its electrical properties after the irradiation. To be precise, there was almost no change in the voltage of its sub-circuits. This means the IA can be operated under stable voltage conditions, and this stability can be further enhanced by the operational amplifiers that constitute the IA. Therefore, it is possible for this radiation-hardened IA to measure and amplify minute

signals in a precise manner. As shown in Figure 10b, it was found that the output duty ratio remained at the 50% level even after the irradiation treatment, and the output full swing could be achieved.



(**a**) (**b**)

Figure 10. Electrical characteristics before and after irradiation with a cumulative radiation dose of 25.8 kGy of (**a**) the standard IA and (**b**) of the radiation-hardened IA.

The relatively low-voltage measurement of the sub-circuits, when compared with the post-layout simulation results, can be ascribed to the line noise that was generated from the 25 m cable used for real-time measurement. Nevertheless, the figure is still within the allowable error range.

3.2. Irradiation Test Result and Analysis of IAs

Table 5 summarizes the degree of damage observed in both the standard IA and the radiation-hardened I-gate type IA that was designed and manufactured herein. To begin with, radiation-induced damage occurred in the standard IA, and the performance of its sub-circuits and main circuit were degraded, resulting in a decrease in gain factor. To be more specific, first, the BGR voltage was increased by the applied radiation, which led to an increase in the LDO voltage. This change caused the bias voltage and the reference voltage, which govern the operation of the IA, to change by nearly 5%, and the output duty ratio of the IA also ended up being changed by 18%. In a radiation environment, these bias and reference voltage errors affect the common voltage (V_{CM}) that determines the operating point of the IA. This will negatively affect the common-mode rejection ratio (CMRR) and bandwidth that indicate the performance of the IA. Since these performance indicators are difficult to measure in real-time during the irradiation, the damage was confirmed by the duty ratio caused by the change of the operating point of the output of the IA.

Eventually, all this will lead to malfunction, changing the gain factor of the IA. At the same time, the radiation-induced leakage current that is generated inside each of its circuits accelerates the overall damage process when combined with other radiation-induced damage factors.

Table 5. Radiation-induced damage by TID effects in the radiation-hardened IA.

Measurement Results			
Param.	**Irradiation**	**Conventional IA**	**Radiation-hardened IA**
BGR voltage [V]	Before	1.1843	1.1601
	After (25.8 kGy)	1.2403	1.1674
	Damage (%)*	4.72	0.63

Table 5. *Cont.*

Measurement Results			
Param.	**Irradiation**	**Conventional IA**	**Radiation-hardened IA**
LDO voltage [V]	Before	1.7482	1.7134
	After (25.8 kGy)	1.8333	1.7237
	Damage (%)*	4.86	0.6
Output pulse duty [%]	Before	50.52	50.19
	After (25.8 kGy)	41.47	50.27
	Damage (%)*	-17.91	0.16

*Change in the electrical characteristics before and after the irradiation treatment (radiation-induced damage).

In contrast, the electrical characteristics of the radiation-hardened IA were maintained before and after the irradiation. In other words, it was verified that the radiation-hardened IA was capable of precisely measuring and amplifying minute signals in radiation environments. Considering the disastrous consequences of possible failures in measuring sensor signals in radiation facilities, such as nuclear power plants and radiation therapy rooms at hospitals, which could result in safety accidents or loss of life, this radiation-hardened device technology is of critical importance.

Figures 11 and 12 present the electrical characteristics of the standard/radiation-hardened IAs, its sub-circuits, BGR, and LDO circuits, and how they change with respect to the increasing total cumulative dose. In the standard IA, the voltage of the sub-circuits sharply increased with the increased cumulative dose, but as the total cumulative dose exceeded 5 kGy, the change slowed, and the radiation-induced damage was saturated. However, due to the offset generated by the radiation-induced damage, the IA could hardly function properly. In contrast, in the radiation-hardened IA, the output voltage of its sub-circuits remained almost the same, and the output duty of the IA remained at the 50% level despite the increasing cumulative radiation dose, demonstrating that the radiation-hardened IA provided radiation-resistance performance.

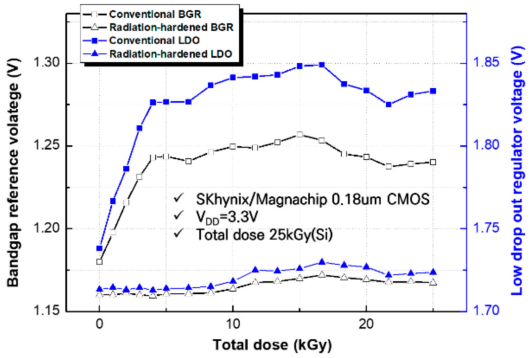


Figure 11. Change in the BGR output and LDO voltage with respect to the increasing total cumulative dose.

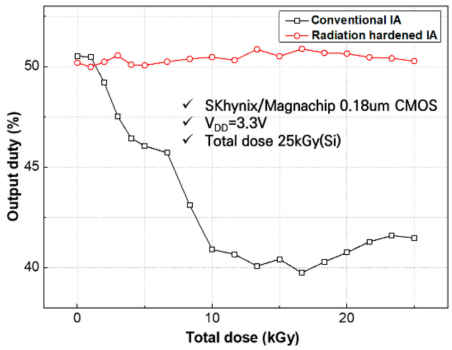


Figure 12. Change in the duty ratio of the IA with respect to the increasing total cumulative dose.

4. Conclusions

An instrumentation amplifier (IA) capable of precisely measuring minute signals in radiation environments was proposed, and its characteristics were verified. The IA chips were manufactured using the application-specific integrated circuit (ASIC) design-based layout modification method, which is the most suitable approach to implement radiation hardening. Apart from the IA, all necessary components needed for the actual chip operation, including bandgap reference (BGR) circuits and low dropout (LDO) regulators, were radiation-hardened. Irradiation tests were conducted to verify the resistance performance of the developed IA to the total ionizing dose (TID) effect. The tests were conducted until the total cumulative radiation dose reached 25.8 kGy. As a result, radiation-induced damage was found to occur in the standard IA, causing the malfunction of its electric circuits. In contrast, the radiation-hardened IA maintained its electrical characteristics before and after the irradiation.

The major findings of the present study are expected to greatly contribute to ensuring that sensor systems for control and instrumentation applications can fulfill their intended purposes, even in radiation environments. Additionally, the data provided in the present study will serve as key basic data to establish radiation-hardened electronic systems going forward.

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