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Efficient Approach for Electrical Design and Analysis of High-Speed Interconnect in Integrated Circuit Packages

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Abstract: In recent integrated circuit (IC) packages, the structure of the interconnect is highly complex, and the effect of high-frequency parasitics is significant. These factors increase the number and level of design variables and extend the analysis frequency range to tens of gigahertz. As a result of the high dimensions of the design space, it is difficult to reduce the design gap between the current design approach and the physical limits of the practical IC-package interconnect. In this paper, we present an efficient approach for designing and analyzing the electrical characteristics of the high-speed interconnect in IC packages. The proposed approach is developed using a hybrid method involving the design of experiments, the domain decomposition method, and the finite-element method. We present a procedure to identify critical design variables for the IC-package interconnect, and we derive a method to recombine the impedance parameters of a segmented interconnect. The proposed hybrid method is verified by comparing its characteristic impedance (Z_o) with the Z_o value from a full-wave simulation of a complete interconnect. We demonstrate that the proposed hybrid method significantly reduces the design space of the IC-package interconnect so that we can efficiently and rapidly obtain the optimized solution, thereby improving the system performance.

Keywords: domain decomposition method (DDM); IC package; signal integrity; Taguchi method

1. Introduction

Integrated circuit (IC) package design is a complex and time-consuming process for achieving a reliable and high-performance system. It requires the multidisciplinary optimization of multiple design variables associated with thermomechanical and electrical characteristics. In thermomechanical design, various parameters, such as the materials and thicknesses of an epoxy molding compound and the adhesive for die attachment, must be considered in IC-package analysis. The analysis objective is to minimize the package warpage and avoid delamination, thus ensuring structural reliability and manufacturing process availability. To perform the analysis, numerical techniques, e.g., the finite-element modeling of an IC package, can be employed, which require large amounts of computational resources and simulation time.

In the electrical design of an IC package, numerous design variables, including the geometric parameters of the signal interconnects and power-delivery networks, must be considered for achieving the high throughputs, bandwidths, and data rates of the devices in the package. The electrical characteristics of an IC package are determined using computationally expensive simulations involving the finite-element method (FEM), the finite-difference time-domain (FDTD) method, and the method of moments.

A difficulty in IC-package design is that the results of the electrical and thermomechanical designs are affected by each other, as they share common design variables, necessitating a tradeoff design. To efficiently obtain an optimized solution for both designs, a multiphysics simulation scheme is preferred; however, such a scheme is not suitable for the development of practical applications [1,2]. During industrial developments of an IC package, thermomechanical and electrical engineers separately perform simulations and analyses for their own goals and iteratively modify their designs by communicating with each other. It is time-consuming to optimize a tradeoff design, because both the electrical and thermomechanical characteristics are predicted via computationally expensive methods.

Additionally, the package types are continuously evolving into complex multichip packages such as the embedded multimedia card, the embedded multichip package, and universal flash storage. From the viewpoint of electrical design, these package types significantly increase the difficulty of IC-package design, because they employ high-density ICs vertically and horizontally stacked in the package substrate, as well as differential interconnects of SERDES devices for high-speed IC communications. In particular, high-speed interconnect design is one of the crucial parts of real IC-package design, which is the focus of this study. The reason why it is critical is that the use of high-speed interconnect in the state-of-the-art IC package dramatically increases; however, its analysis and optimization method become more difficult and less efficient [3–5].

As the data rate and density of the IC-package interconnect increase, the effects of parasitics such as mutual capacitance, mutual inductance, and the skin effect cannot be ignored. In the simulation, a broadband interconnect model must be adopted to successfully capture the high-frequency effect of parasitics and accurately analyze various electrical characteristics, as shown in Figure 1. Full-wave simulation techniques using the FEM and the FDTD method are effective for practical design. They provide a convenient method for the analysis of an arbitrary interconnect structure in the wideband frequency range. In [6–8], the previous approach was used to successfully extract scattering parameters and estimate the signal integrity characteristics of an IC-package interconnect. However, even with the advantages of the high design flexibility and accurate results, this approach has the practical problem of being time-consuming. To obtain accurate results using the full-wave simulation of the entire IC-package interconnect, a large number of analysis meshes are inevitably generated, which leads to an extremely long simulation time for one design case. Moreover, the high complexity of a multichip package significantly increases the numbers of geometric parameters and degrees of freedom in the electrical design. Consequently, the solution space is substantially expanded. It requires a large amount of time to complete an examination of all design cases and obtain an optimized solution using conventional design methods. It is difficult to achieve the timely completion of the IC-package design using the conventional methods for the electrical design of an IC package [9,10].

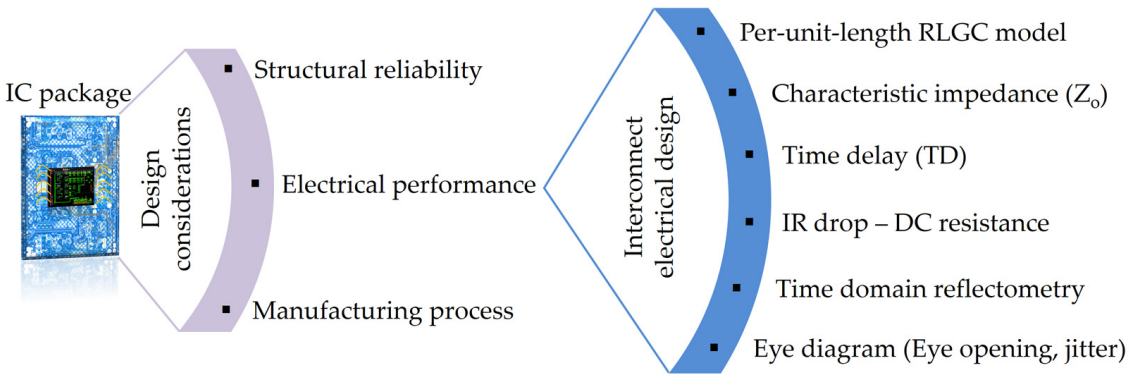

Figure 1. Design considerations and specifications for the electrical design of the integrated circuit (IC)-package interconnect.

In this paper, an efficient method for the reduction of a solution space and the optimization of the electrical design of an IC package using design of experiments (DoE) and the domain decomposition method (DDM) is presented [11–15]. For rapid analysis, the number of degrees of freedom is reduced according to the DoE results, and the analysis domain is decomposed into subdomains. A recombined impedance matrix for the subdomain solutions is analytically derived.

2. Methods

The proposed approach is intended to facilitate the development of the high-speed interconnect for practical IC packages. For the rapid and efficient design and analysis of the electrical characteristics of the IC-package interconnect, the proposed method adopts two approaches: reducing the number of degrees of freedom in the IC-package design and reducing the maximum number of computational meshes generated during a full-wave simulation. The reduction of the number of degrees of freedom in the IC-package interconnect design is achieved by determining a critical variable (CV) of the interconnect design via the Taguchi method, which employs an orthogonal array to efficiently reduce the number of test sets required in a design procedure [16]. The computational mesh number is reduced by applying the DDM to the IC-package interconnect and deriving a closed-form expression for the recombination impedance parameters, which is simply converted into the scattering parameters (S-parameters) and characteristic impedance (Z_o). The proposed approach is a hybrid method that involves identifying the critical design variables and dividing the IC-package interconnect into segmented parts, i.e., the CV-based DDM (CVDDM).

The proposed CVDDM mainly comprises two parts—CV analysis and the CV-based DDM—as shown in Figure 2 [11–13,17,18]. In the CV analysis, a strategy using DoE based on the Taguchi method is employed. The design variables of the IC-package interconnect are discriminated between low and high sensitivities to electrical characteristics such as Z_o, the RLGC parameters, and the S parameters. The objective of the CV analysis step is determining the CVs, which significantly affect the electrical characteristics of the IC-package interconnect. Since the solution space for the electrical design of a recent IC-package interconnect is extremely large when all the geometric parameters are considered, CV-based design is easier than the previous approach that involves a full factorial test of the IC-package interconnect and the evaluation of all combinations of design variables in a full-wave simulation.

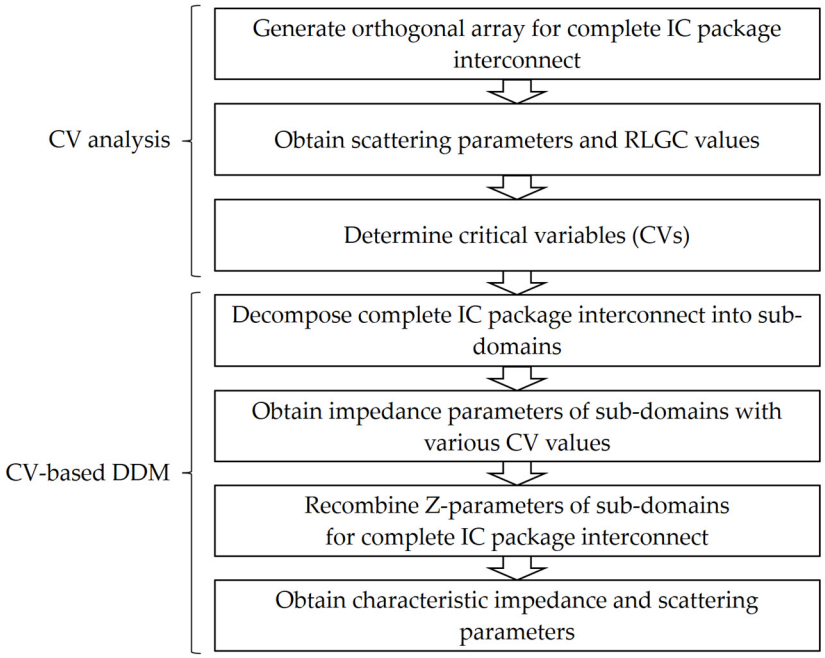

Figure 2. Overall procedure of the CVDDM (critical variable-based domain decomposition method).

2.1. CV Analysis

The first step in the CV analysis is the generation of an orthogonal array (OA) considering the numbers and levels of all geometric parameters in the complete IC-package interconnect. To reduce the number of simulations and efficiently determine the CVs, a fractional factorial characteristic based on the Taguchi method is adopted rather than a full factorial approach. In statistics, the optimized result using OAs and the Taguchi method is close to that of the full factorial approach. The existence and construction of OAs are introduced in [16]. The notation OA (N, q, s, t) is adopted, which represents a matrix of N rows and q columns with entries from S. N and q represent the numbers of simulation runs and design parameters, respectively. S is a set of the levels of the design variables, and t represents the strength, as described in [16]. To appropriately select an OA, an existing database for OAs can be used [19]. A useful property of OAs is that a subarray with N rows and k columns extracted from an OA (N, q, s, t) can be an OA (N, k, s, u) whose u is equal to the minimum value between k and t. Thus, a new OA (N, k, s, u) is simply obtained by discarding one or more columns of an OA (N, q, s, t) found in the database when a number of parameters of j smaller than k is needed in the IC-package interconnect design.

The next step of the CV analysis is extracting the electrical characteristics of a complete IC-package interconnect represented as an RLGC model, which can be reduced to an LC model with the assumption of a lossless transmission line. All LC models corresponding to simulation runs of OA (N, k, s, u) are obtained. The technique of S parameter-based transmission-line characterization [20] is employed to extract the LC models from the S parameters of complete IC-package interconnects. Each S-parameter result is acquired using a full-wave simulation based on the FEM. In this study, an IC-package interconnect based on differential transmission lines is characterized, because such interconnects have been widely adopted in recent high-speed packages. Through a full-wave simulation of differential transmission lines, the results for S parameters with four ports and a single-ended configuration are extracted. These are converted into mixed-mode S parameters [21] to construct an LC model of a coupled line. The LC model of a coupled line consists of self-inductances (L_{11}, L_{22}), self-capacitances (C_{11}, C_{22}), mutual inductances (L_{12}, L_{21}), and mutual capacitances (C_{12}, C_{21}). These parameters are obtained from the mixed-mode S parameters via S-parameter-based RLGC extraction [20]. The even and odd-mode propagation constants (γ_e, γ_o) are given as follows:

$$\gamma_e = \frac{1}{d}\ln\left\{\frac{1-S_{dd11}^2+S_{dd21}^2}{2S_{dd21}}+\left(\frac{\left(S_{dd11}^2-S_{dd21}^2+1\right)^2-\left(2S_{dd11}\right)^2}{\left(2S_{dd21}\right)^2}\right)^{1/2}\right\}, \tag{1}$$

$$\gamma_o = \frac{1}{d}\ln\left\{\frac{1-S_{cc11}^2+S_{cc21}^2}{2S_{cc21}}+\left(\frac{\left(S_{cc11}^2-S_{cc21}^2+1\right)^2-\left(2S_{cc11}\right)^2}{\left(2S_{cc21}\right)^2}\right)^{1/2}\right\}, \tag{2}$$

where S_{dd} and S_{cc} represent the differential-mode and common-mode submatrices, respectively, of the mixed-mode S parameters.

The closed-form expressions for even and odd-mode characteristic impedances (Z_{oe}, Z_{oo}) are derived as follows [22]:

$$Z_{oe} = Z_{oe,ref}\cdot\sqrt{\frac{\left(1+S_{dd11}\right)^2-S_{dd21}^2}{\left(1-S_{dd11}\right)^2-S_{dd21}^2}}, \tag{3}$$

$$Z_{oo} = Z_{oo,ref}\cdot\sqrt{\frac{\left(1+S_{cc11}\right)^2-S_{cc21}^2}{\left(1-S_{cc11}\right)^2-S_{cc21}^2}}, \tag{4}$$

where $Z_{oe,ref}$ and $Z_{oo,ref}$ represent the reference impedances for even and odd-mode propagations, respectively.

Finally, the LC model is extracted as follows:

$$L_{11} = \frac{\mathrm{Im}\{\gamma_e Z_{oe} + \gamma_o Z_{oo}\}}{(2\pi f)}, \tag{5}$$

$$L_{12} = \frac{\mathrm{Im}\{\gamma_e Z_{oe} - \gamma_o Z_{oo}\}}{(2\pi f)}, \tag{6}$$

$$C_{11} = \frac{\mathrm{Im}\{\gamma_e / Z_{oe} + \gamma_o / Z_{oo}\}}{(2\pi f)}, \tag{7}$$

$$C_{12} = \frac{\mathrm{Im}\{\gamma_e / Z_{oe} - \gamma_o / Z_{oo}\}}{(2\pi f)}. \tag{8}$$

It is worth noting that the proposed method is limited to a lossless package interconnect. To extend the method to a lossy package interconnect including R and G components, we will verify it in a further study. The effects of the design variables on the L and C values are examined using a sensitivity analysis based on the Taguchi method. The L and C variations of all the simulation runs corresponding to OA (N, k, s, u) are calculated. The design variables (i.e., V_1, V_2, ... , V_k) for each case of L_{11}, L_{12}, C_{11}, and C_{12} are ranked according to the sensitivity. A design variable where a larger variation is observed is assigned higher priority. Thus, the priority order of the design variables is established for each L and C value. For instance, a line width represented as V_i may significantly affect L_{11}, L_{12}, and C_{11}, whereas its effect on C_{12} may be smaller. Then, the line width V_i has a small priority-order number for L_{11}, L_{12}, and C_{11} and a large priority-order number for C_{12}. Hence, all the design variables have four numbers indicating the priority order for L_{11}, L_{12}, C_{11}, and C_{12}. The priority-order numbers of V_i for L_{11}, L_{12}, C_{11}, and C_{12} are denoted as $P_{i,L11}$, $P_{i,L12}$, $P_{i,C11}$, and $P_{i,C12}$, respectively. A linear combination of the priority numbers for V_i is given as follows:

$$P_i = w_{L11} \cdot P_{i,L11} + w_{L12} \cdot P_{i,L12} + w_{C11} \cdot P_{i,C11} + w_{C12} \cdot P_{i,C12}, \tag{9}$$

where w_{L11}, w_{L12}, w_{C11}, and w_{C12} represent the weights, which are equal to 1 in this study. However, the values can be adjusted for other design objectives. For instance, w_{L12} and w_{C12} are more significant than w_{L11} and w_{C11} when crosstalk reduction is a primary goal of an IC-package interconnect design. The CVs for the high-speed IC-package interconnect design are determined according to the linear combination of the priority numbers. The CVs are selected among the design variables for which the result of the linear combination is smaller than a specific number.

2.2. CV-Based DDM

In this subsection, a DDM for a high-speed IC-package interconnect is presented to reduce the number of analysis meshes handled during a single simulation run. In the DDM, the analysis domain of the original and complete package interconnect is decomposed into nonoverlapping subdomains. The solutions of the adjacent subdomains are related by the continuity conditions at the interfaces. In this study, on the basis of the geometry, the original domain of the IC-package interconnect is divided into several subdomains corresponding to bonding wires, transmission lines, vias, and solder balls, as shown in Figure 3. The subdomains are nonoverlapping, and the current–continuity relationship is valid at their interfaces. Intersegment coupling is not considered in this DDM, for the simplicity of the design and analysis.

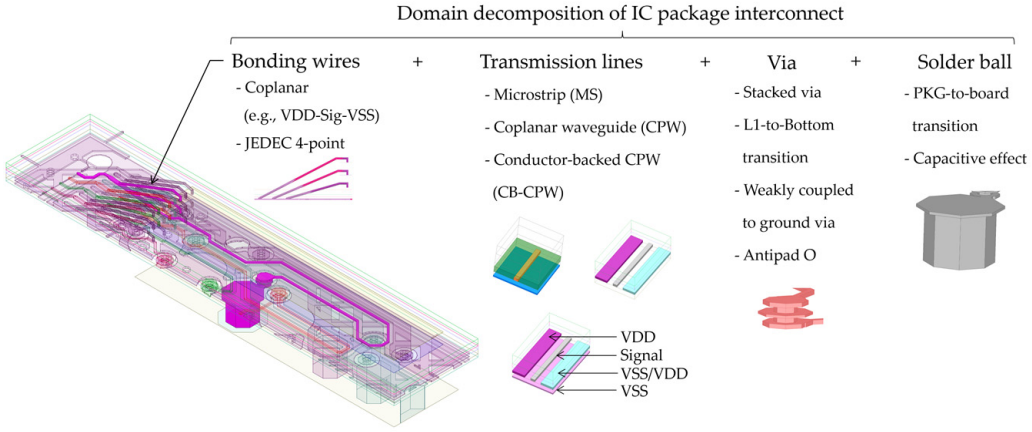

Figure 3. IC-package interconnect decomposed into various segments, i.e., bonding wires, transmission lines, vias, and solder balls.

For the bonding-wire segment, four coplanar bonding wires (ground–signal–signal–ground (G-S-S-G) configuration) are commonly employed [23–25]. Its shape follows the JEDEC 4-point. A transmission-line segment can consist of various types of transmission lines, such as a microstrip, coplanar waveguide, and conductor-backed coplanar waveguide lines. A via has a stacked structure and is employed for layer transition. A solder-ball segment connects the signal and power nets of an IC package to those of printed circuit boards. Its shape is modeled as a polygonal column rather than a sphere for the simplicity of the analysis. The polygonal column model successfully captures the capacitive effect of a solder ball, which significantly affects the electrical characteristics of the entire IC-package interconnect.

Next, the impedance parameters of all the segments with nominal values of the design variables are determined using full-wave simulations. Since an interconnect structure is partitioned into small segments, full-wave simulations for the segments are more efficient than the analysis of the entire structure with large meshes. Additionally, by sweeping the CVs, more impedance parameters of the segments (including the various values of the CVs) can be determined, allowing an electrical design engineer to easily explore the solution space of an IC-package interconnect and obtain a tradeoff solution.

An analytical method to recombine the impedance parameters of subdomains is developed to rapidly and systematically obtain the original impedance parameter of a complete IC-package interconnect. The signaling-type IC-package interconnect, which is the focus of the present study, performs differential signaling with five conductors. The segments of the IC-package interconnect comprise four narrow conductors with the configuration of G-S-S-G, which are located on a wide conductor. Since all the ground conductors are regarded as a return path in the complete IC-package interconnect, the electrical performance of the entire IC-package interconnect can be completely characterized using a four-port impedance parameter. However, the segments of the decomposed IC-package interconnect require the impedance parameters containing more ports. The narrow conductors of the segments at the decomposition interface are considered as the microstrip lines or striplines to examine the CV effect. Hence, the bonding-wire and solder-ball segments contain six ports, whereas the transmission-line and via segments have eight ports.

Figure 4 presents the block diagram for deriving analytical expressions for a recombination impedance parameter. Suppose that $Z_{C(i,j)}$ is the impedance parameter of the original interconnect and that $Z_{A(i)}$ and $Z_{B(j)}$ are those of the segments where the original interconnect is decomposed. The indices i and j represent the order of the impedance parameter sets when the segments A and B contain the results obtained by sweeping the various values of the CVs. As explained previously, $Z_{A(i)}$ and $Z_{B(j)}$ can be easily determined using full-wave simulations. The objective of the recombination step is to express $Z_{C(i,j)}$ using $Z_{A(i)}$ and $Z_{B(j)}$. Here, the notation $\oplus$ is defined as the recombination operation.

Moreover, the external and internal ports are defined as the port of the original interconnect and the port at the interface generated by the DDM, respectively. The external port $\overline{P}$ and internal ports $\overline{q}$ and $\overline{r}$ are shown in Figure 5. Then, the impedance parameter Z_C is given as follows [26]:

$$Z_{C(i,j)} = Z_{A(i)} \oplus Z_{B(j)} = Z_{PP} - \left(Z_{Pq} - Z_{Pr}\right)\left(Z_{qq} + Z_{rr}\right)^{-1}\left(Z_{qP} - Z_{rP}\right), \tag{10}$$

where

$$Z_{PP} = \begin{pmatrix} Z_{11,A(i)} & Z_{12,A(i)} & 0 & 0 & 0 & 0 \\ Z_{21,A(i)} & Z_{22,A(i)} & 0 & 0 & 0 & 0 \\ 0 & 0 & Z_{55,B(j)} & Z_{56,B(j)} & Z_{57,B(j)} & Z_{58,B(j)} \\ 0 & 0 & Z_{65,B(j)} & Z_{66,B(j)} & Z_{67,B(j)} & Z_{68,B(j)} \\ 0 & 0 & Z_{75,B(j)} & Z_{76,B(j)} & Z_{77,B(j)} & Z_{78,B(j)} \\ 0 & 0 & Z_{85,B(j)} & Z_{86,B(j)} & Z_{87,B(j)} & Z_{88,B(j)} \end{pmatrix}, \tag{11}$$

$$Z_{Pq} = \begin{pmatrix} Z_{13,A(i)} & Z_{14,A(i)} & Z_{15,A(i)} & Z_{16,A(i)} \\ Z_{23,A(i)} & Z_{24,A(i)} & Z_{25,A(i)} & Z_{26,A(i)} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix}, \tag{12}$$

$$Z_{Pr} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ Z_{51,B(j)} & Z_{52,B(j)} & Z_{53,B(j)} & Z_{54,B(j)} \\ Z_{61,B(j)} & Z_{62,B(j)} & Z_{63,B(j)} & Z_{64,B(j)} \\ Z_{71,B(j)} & Z_{72,B(j)} & Z_{73,B(j)} & Z_{74,B(j)} \\ Z_{81,B(j)} & Z_{82,B(j)} & Z_{83,B(j)} & Z_{84,B(j)} \end{pmatrix}, \tag{13}$$

$$Z_{qq} = \begin{pmatrix} Z_{33,A(i)} & Z_{34,A(i)} & Z_{35,A(i)} & Z_{36,A(i)} \\ Z_{43,A(i)} & Z_{44,A(i)} & Z_{45,A(i)} & Z_{46,A(i)} \\ Z_{53,A(i)} & Z_{54,A(i)} & Z_{55,A(i)} & Z_{56,A(i)} \\ Z_{63,A(i)} & Z_{64,A(i)} & Z_{65,A(i)} & Z_{66,A(i)} \end{pmatrix}, \tag{14}$$

$$Z_{rr} = \begin{pmatrix} Z_{11,B(j)} & Z_{11,B(j)} & Z_{11,B(j)} & Z_{11,B(j)} \\ Z_{43,A(i)} & Z_{44,A(i)} & Z_{45,A(i)} & Z_{46,A(i)} \\ Z_{53,A(i)} & Z_{54,A(i)} & Z_{55,A(i)} & Z_{56,A(i)} \\ Z_{63,A(i)} & Z_{64,A(i)} & Z_{65,A(i)} & Z_{66,A(i)} \end{pmatrix}, \tag{15}$$

$$Z_{qP} = \begin{pmatrix} Z_{31,A(i)} & Z_{32,A(i)} & 0 & 0 & 0 & 0 \\ Z_{41,A(i)} & Z_{42,A(i)} & 0 & 0 & 0 & 0 \\ Z_{51,A(i)} & Z_{52,A(i)} & 0 & 0 & 0 & 0 \\ Z_{61,A(i)} & Z_{62,A(i)} & 0 & 0 & 0 & 0 \end{pmatrix}, \tag{16}$$

$$Z_{rP} = \begin{pmatrix} 0 & 0 & Z_{15,B(j)} & Z_{16,B(j)} & Z_{17,B(j)} & Z_{18,B(j)} \\ 0 & 0 & Z_{25,B(j)} & Z_{26,B(j)} & Z_{27,B(j)} & Z_{28,B(j)} \\ 0 & 0 & Z_{35,B(j)} & Z_{36,B(j)} & Z_{37,B(j)} & Z_{38,B(j)} \\ 0 & 0 & Z_{45,B(j)} & Z_{46,B(j)} & Z_{47,B(j)} & Z_{48,B(j)} \end{pmatrix}. \tag{17}$$

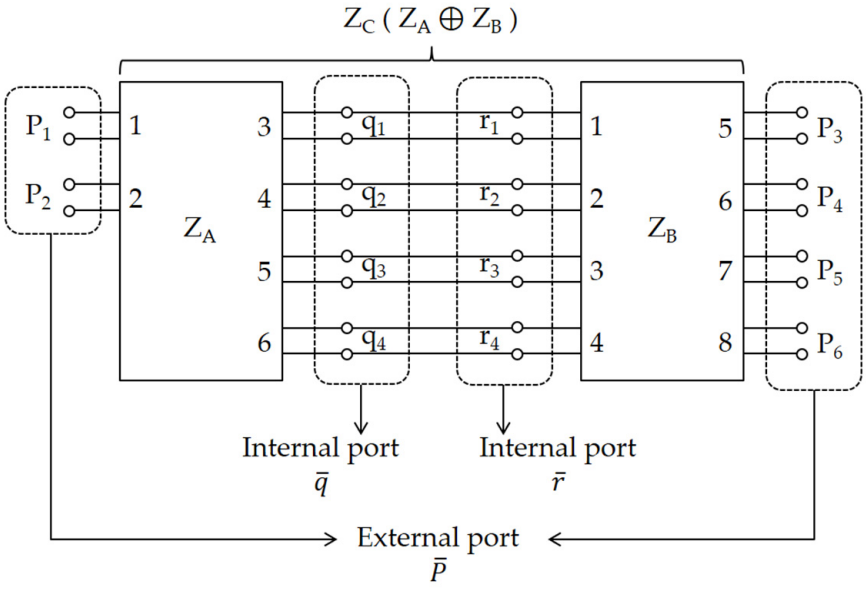

Figure 4. Impedance block diagram for determining the recombination impedance parameters of domain decomposition method (DDM) segments A and B.

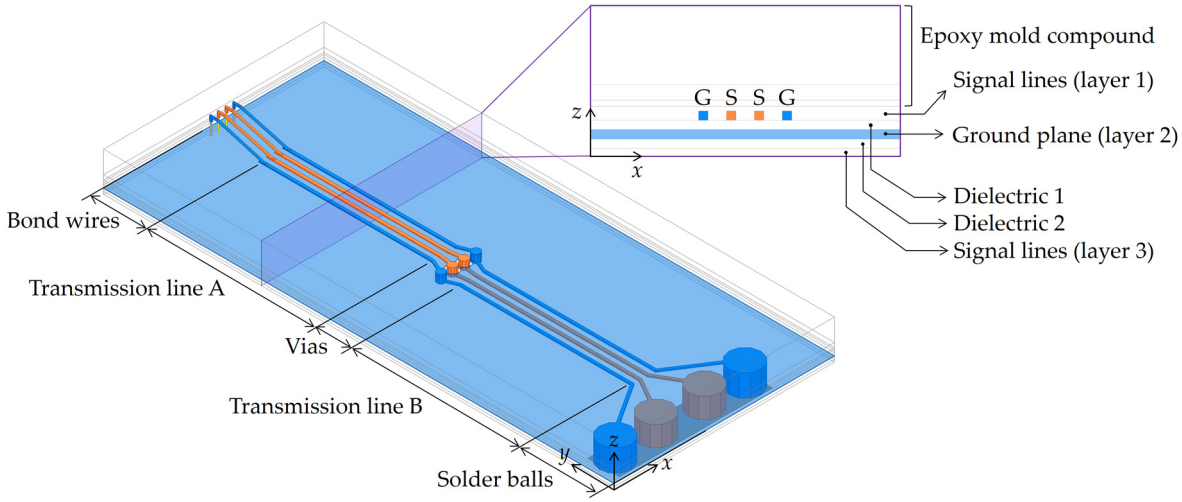

Figure 5. Basic structure of the IC-package interconnect for demonstration of the proposed CVDDM.

$Z_{mn,A}$ (m, n = 1, 2, . . . , 6) and $Z_{mn,B}$ (m, n = 1, 2, . . . , 8) are the entities of the impedance parameters Z_A and Z_B, respectively.

The specific impedance parameter associated with the differential interconnect of the IC package is analytically derived. Even though the impedance parameters of the DDM segments can be completely recombined using computer-aided engineering tools such as ANSYS Electronics Desktop and Keysight Advanced Design Systems, the proposed method based on the analytical expressions has the advantages of rapid estimation and systematic automation based on script-level programming, which is not dedicated to particular languages. Thus, the development of the IC-package interconnect can be more flexible.

In the final step of the CV-based DDM, the impedance parameter is converted into the S-parameter S_C as follows:

$$\mathrm{S_C} = (\mathrm{Z_C} + \mathrm{Z_o E})^{-1}(\mathrm{Z_c} - \mathrm{Z_o E}), \tag{18}$$

where Z_o represents a reference impedance value, which is nominally 50 Ω. E represents the identity matrix.

Then, a mixed-mode S-parameter is given as follows [27]:

$$S_{dd11} = \frac{1}{2}(S_{11,C} - S_{21,C} - S_{12,C} + S_{22,C}), \quad (19)$$

$$S_{dd21} = \frac{1}{2}(S_{31,C} - S_{41,C} - S_{32,C} + S_{42,C}) = S_{dd12}, \quad (20)$$

$$S_{dd22} = \frac{1}{2}(S_{33,C} - S_{43,C} - S_{34,C} + S_{44,C}). \quad (21)$$

3. Results and Discussion

The proposed CVDDM for the electrical design of the IC-package interconnect was demonstrated using a full-wave simulation of a basic structure of a differential interconnect. We adopt the ANSYS HFSS software for a full-wave simulation. Figure 5 shows the simple structure and the stacked layers of the IC-package interconnect, which included bond wires, transmission lines, vias, and solder balls. The simulation model comprised three conductor layers. Copper was used as the conductor material. Dielectrics 1 and 2 were placed above and below the ground plane on layer 2, respectively. The nominal values of the dielectric constant and loss tangent were 4.3 and 0.009, respectively. An epoxy mold compound (EMC) was placed on dielectric 1 for package protection. The dielectric constant and loss tangent of the EMC were 4.1 and 0.022, respectively.

Before the proposed CVDDM was applied, the design variables of the IC-package interconnect were defined, as shown in Figure 6. The bond-wire segment heights, length, diameter, and spacing were represented as h_{bw1}, h_{bw2}, L_{bw}, w_{bw}, and s_{bw}, respectively. From a practical viewpoint, it is preferred that the electrical characteristics of the bond-wire segment are adjusted using the length variable L_{bw}. This variable may be a CV, while the other variables use nominal values. For the transmission-line segment, d_{TL}, s_{TL}, w_{TL}, and h_{TL} represent the length, spacing, and width of the signal line and the distance between the signal line and the ground plane, respectively. ε_r represents the dielectric constant. For the via segment, d_v, s_v, and h_v represent the diameter, spacing, and length of the via, respectively. w_t represents the width of the transition part from a via to a transmission line. L_v represents the total length of the via segment, including the transition part. Commonly, via designs using the variables h_v and L_v are not flexible in the practical IC-package process. For the solder-ball segment, d_{sb}, s_{sb}, and h_{sb} represent the diameter, spacing, and height of the solder ball, respectively. w_t represents the width of the transition part. L_{sb} represents the total length of the solder-ball segment. Nominally, w_t is equivalent to the width of the transmission line.

To demonstrate the proposed CVDDM for the basic structure of the IC-package interconnect, the design variables and their levels were determined considering the package manufacturing process. Eleven variables were employed: d_{bw}, d_{TL}, s_{TL}, w_{TL}, h_{TL}, ε_r, d_v, s_v, d_{sb}, h_{sb}, and s_{sb}. Their levels were varied from 50% to 150% of the nominal value (i.e., level 2), as shown in Table 1. The non-included variables in the CV list were h_{bw1}, h_{bw2}, w_{bw}, s_{bw}, L_v, L_{sb}, and w_t. The default values of h_{bw1}, h_{bw2}, w_{bw}, s_{bw}, L_v, and L_{sb} were 50, 110, 25, 40, 310, and 530 µm, respectively. The w_t value was equivalent to w_{TL} for each simulation run. Using these variables, the Taguchi method was applied to the complete IC-package interconnect. An OA, i.e., OA (27, 11, 3, 2), was generated [19], as shown in Table 2. The OA had 27 rows and 11 columns. The rows represent the 27 distinct experiments to conduct a FEM-based simulation of the entire IC-package interconnect.

As described in the previous section, the self-inductance, mutual inductance, and capacitances for all the experiments were extracted using the S parameters obtained via the FEM simulations and the S-parameter-based RLGC extraction method, as shown in Table 2. The self-inductance L_{11} varied from 1.63 to 3.41 nH, and the L_{12} values were between 0.33 and 1.06 nH. Moreover, the FEM simulation results indicated that the self-capacitance C_{11} ranged from 0.70 to 1.91 pF, and the mutual capacitance C_{12} ranged from 0.11 to 0.27 pF. According to these results, a DoE analysis was performed, as shown in Figure 7. The effects of all the design variables on the electrical characteristics of the

complete IC-package interconnect were clearly revealed using the Taguchi method. Additionally, the priority-order numbers of all the variables for the L_{11}, L_{12}, C_{11}, and C_{12} effects were obtained, as shown in Table 3. When the linear combination of the priority-order numbers (i.e., P_i) was estimated, w_{L11}, w_{L12}, w_{C11}, and w_{C12} were all set to 1. According to the P_i values, five variables (d_{bw}, d_{TL}, s_{TL}, w_{TL}, and h_{TL}) were selected as CVs. Thus, the bond-wire length and transmission-line design significantly affected the overall electrical characteristics of the complete IC-package interconnect. The nominal designs of the vias and solder balls were considered to be less important.

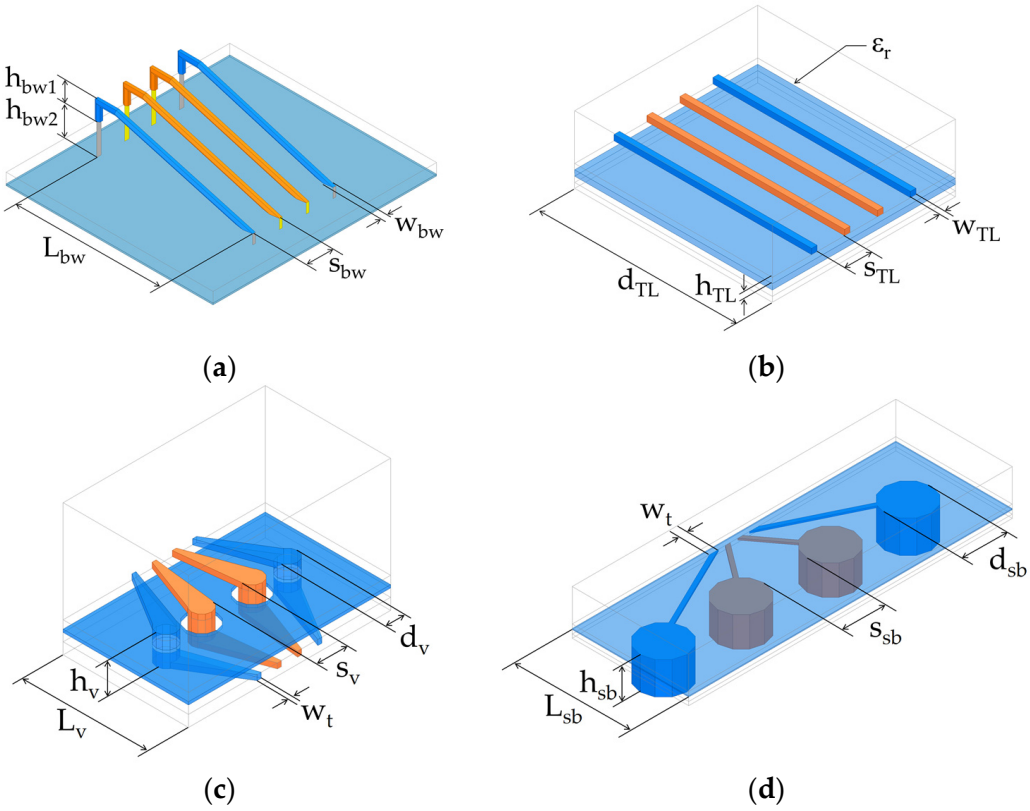

Figure 6. DDM segments: (**a**) bonding wires; (**b**) transmission lines; (**c**) vias; (**d**) solder balls.

Table 1. Design variables and their levels.

Design Variable	Description	Levels		
		1	**2**	**3**
d_{bw} (μm)	bonding-wire length	350	700	1050
d_{TL} (mm)	length of transmission lines	1	2	3
s_{TL} (μm)	spacing between signal lines	20	40	60
w_{TL} (μm)	width of signal line	10	20	30
h_{TL} (μm)	dielectric thickness	10	20	30
ε_r	dielectric constant	3.44	4.30	5.16
d_v (μm)	via diameter	35	65	95
s_v (μm)	spacing between vias	37.5	75	112.5
d_{sb} (mm)	diameter of solder ball	0.24	0.30	0.36
h_{sb} (mm)	height of solder ball	0.115	0.230	0.345
s_{sb} (mm)	spacing between solder balls	0.1	0.2	0.3

Table 2. Orthogonal array (OA) of the IC-package interconnect for the Taguchi analysis.

No.	d_{sb}	d_v	d_{TL}	d_{BW}	h_{sb}	s_{sb}	s_{TL}	s_v	h_{TL}	w_{TL}	ε_r	L_{11}(nH)	L_{12} (nH)	C_{11} (pF)	C_{12} (pF)
1	0.24	35	1	350	0.115	0.1	20	37.5	10	10	3.44	2.52	0.85	1.41	0.24
2	0.24	65	2	700	0.230	0.2	40	112.5	30	30	3.44	2.44	0.75	0.80	0.14
3	0.24	95	3	1050	0.345	0.3	60	75	20	20	3.44	2.44	0.64	0.70	0.07
4	0.30	35	2	1050	0.115	0.2	60	37.5	20	30	3.44	2.14	0.56	0.84	0.08
5	0.30	65	3	350	0.230	0.3	20	112.5	10	20	3.44	1.85	0.55	1.32	0.20
6	0.30	95	1	700	0.345	0.1	40	75	30	10	3.44	3.14	1.06	0.86	0.14
7	0.36	35	3	700	0.115	0.3	40	37.5	30	20	3.44	2.58	0.80	0.75	0.13
8	0.36	65	1	1050	0.230	0.1	60	112.5	20	10	3.44	2.78	0.81	0.87	0.08
9	0.36	95	2	350	0.345	0.2	20	75	10	30	3.44	1.79	0.53	1.76	0.21
10	0.24	35	1	350	0.230	0.2	40	75	20	20	4.30	3.02	0.92	1.20	0.12
11	0.24	65	2	700	0.345	0.3	60	37.5	10	10	4.30	2.61	0.67	1.06	0.05
12	0.24	95	3	1050	0.115	0.1	20	112.5	30	30	4.30	1.88	0.65	0.94	0.24
13	0.30	35	2	1050	0.230	0.3	20	75	30	10	4.30	2.47	0.97	0.92	0.27
14	0.30	65	3	350	0.345	0.1	40	37.5	20	30	4.30	2.12	0.56	1.11	0.13
15	0.30	95	1	700	0.115	0.2	60	112.5	10	20	4.30	2.26	0.60	1.55	0.06
16	0.36	35	3	700	0.230	0.1	60	75	10	30	4.30	1.63	0.33	1.54	0.06
17	0.36	65	1	1050	0.345	0.2	20	37.5	30	20	4.30	2.26	0.88	1.13	0.25
18	0.36	95	2	350	0.115	0.3	40	112.5	20	10	4.30	3.12	0.94	1.06	0.11
19	0.24	35	1	350	0.345	0.3	60	112.5	30	30	5.16	3.41	1.00	1.21	0.09
20	0.24	65	2	700	0.115	0.1	20	75	20	20	5.16	2.07	0.71	1.15	0.24
21	0.24	95	3	1050	0.230	0.2	40	37.5	10	10	5.16	2.19	0.58	1.03	0.09
22	0.30	35	2	1050	0.345	0.1	40	112.5	10	20	5.16	1.90	0.50	1.41	0.10
23	0.30	65	3	350	0.115	0.2	60	75	30	10	5.16	3.28	0.86	0.78	0.07
24	0.30	95	1	700	0.230	0.3	20	37.5	20	30	5.16	2.27	0.82	1.50	0.23
25	0.36	35	3	700	0.345	0.2	20	112.5	20	10	5.16	2.37	0.83	1.11	0.24
26	0.36	65	1	1050	0.115	0.3	40	75	10	30	5.16	1.88	0.53	1.91	0.10
27	0.36	95	2	350	0.230	0.1	60	37.5	30	20	5.16	2.96	0.81	1.08	0.09

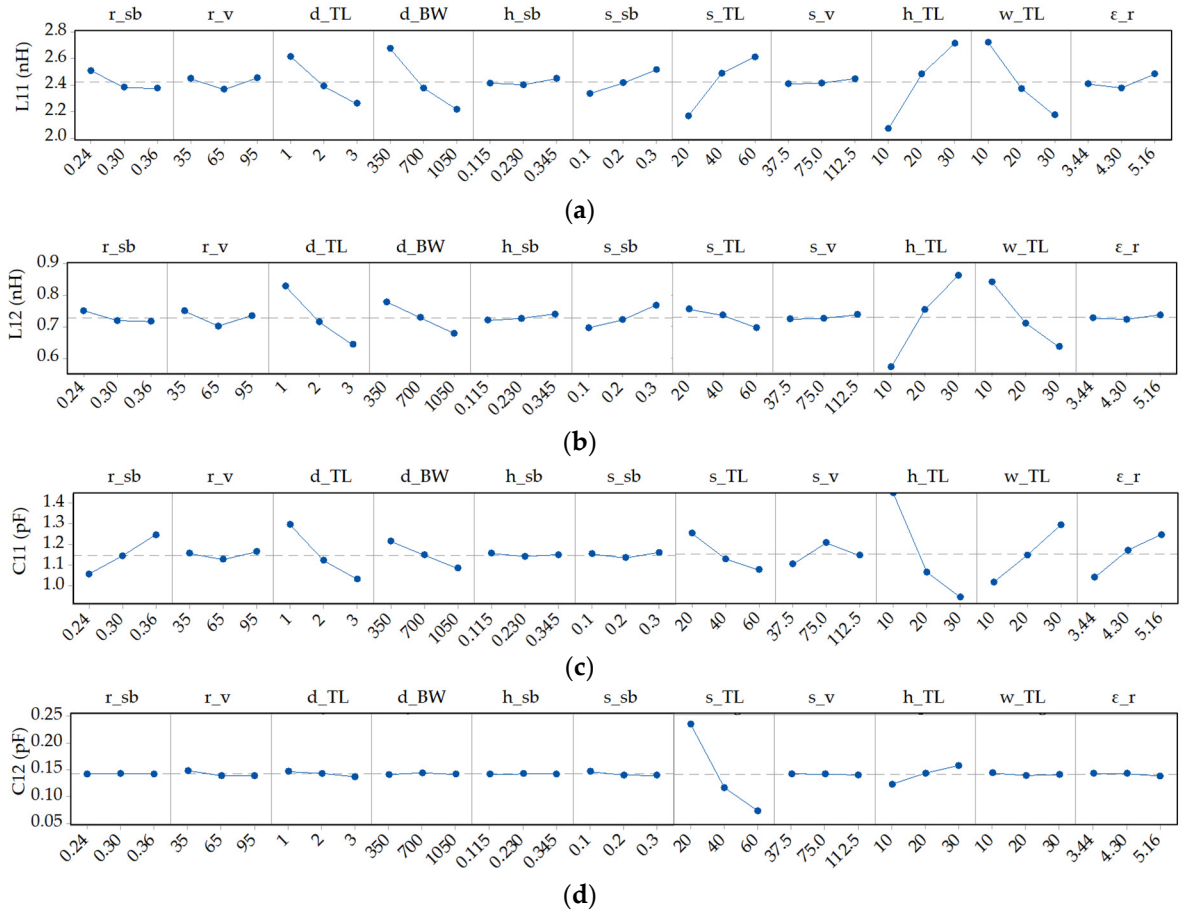

Figure 7. Design of experiments (DoE) results obtained using the Taguchi method for (**a**) L_{11}, (**b**) L_{12}, (**c**) C_{11}, and (**d**) C_{12}.

Table 3. Priority analysis for critical variable (CV) determination.

No.	Variable	$P_{i,L11}$	$P_{i,L12}$	$P_{i,C11}$	$P_{i,C12}$	P_i [1]	CV or non-CV
1	d_{bw}	4	4	7	6	21	CV
2	d_{TL}	5	3	2	3	13	CV
3	s_{TL}	3	6	5	1	15	CV
4	w_{TL}	2	2	3	9	16	CV
5	h_{TL}	1	1	1	2	5	CV
6	ε_r	8	9	4	4	25	Non-CV
7	d_v	9	10	9	7	35	Non-CV
8	s_v	10	8	8	11	37	Non-CV
9	d_{sb}	7	7	6	8	28	Non-CV
10	h_{sb}	11	11	11	10	43	Non-CV
11	s_{sb}	6	5	10	5	26	Non-CV

[1] w_{L11}, w_{L12}, w_{C11}, and w_{C12} were all set to 1.

In this study, the limit value of P_i was empirically determined. A number between 22 and 24 was selected as the limit value of P_i, so that we had only five CVs, for design simplicity. A rigorous study for determining P_i depending on the application of the IC-package interconnect was not conducted. Future research can be performed to identify more effective P_i values; the use of the limit number of P_i is desirable for the systematic approach, which enables design optimization and automation employing a new method such as a machine-learning technique.

Finally, numerous datasets containing the impedance parameters of the DDM segment were obtained by sweeping the CVs in the range of interest. By applying the recombination technique to the datasets, the electrical characteristics of the IC-package interconnect were rapidly determined for various cases. Before beginning the design based on the CVDDM, it will be verified via comparison with the full-wave simulation results of the complete interconnect structure. Since the differential characteristic impedance (Z_{diff}) of the IC-package interconnect is a good metric to evaluate the interconnect performance in a simple manner, the Z_{diff} for the proposed CVDDM was compared with the result of a full-wave simulation of a complete IC-package interconnect, as shown in Figure 8. The differential characteristic impedances for the 27 cases shown in Table 2 were compared. As shown in Figure 8, the proposed CVDDM exhibited good agreement with the full-wave simulation of the entire IC-package interconnect. Although there were discrepancies in the Z_{diff} values for a few cases, they were insignificant considering practical use in the early design stage. The discrepancy is caused by ignoring intersegment coupling.

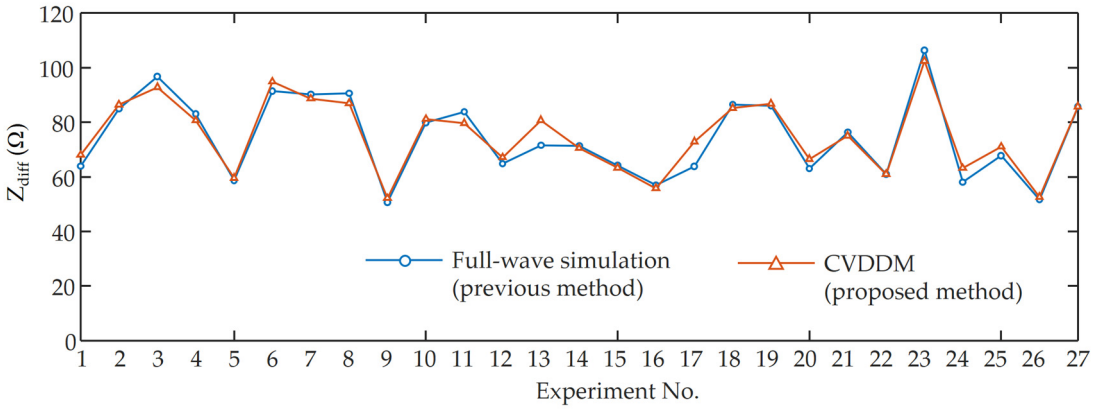

Figure 8. Comparison of differential impedances between the proposed CVDDM and the full-wave simulation for the cases of the Taguchi analysis.

The proposed CVDDM produces a design space providing direct insight into the signal integrity of the high-speed IC-package interconnect. It allows a package design engineer to rapidly and efficiently

optimize an IC-package interconnect and easily develop a new package solution. For instance, a design space with the CVs w_{TL} and h_{TL} is shown in Figure 9. The figure presents all the Z_{diff} values of the full IC-package interconnect for various cases of interest when the development of a new package. Suppose that the thermal and mechanical group provides two possible choices of the dimensions associated with A (h_{TL} = 30 µm, w_{TL} = 10 µm) and B (h_{TL} = 10 µm, w_{TL} = 30 µm). An immediate response can be achieved using the design space constructed via the CVDDM. As shown in Figure 10, the S-parameter results for A and B were significantly different. The dimensions of A must be selected to ensure the good electrical characteristics of the IC-package interconnect. When the previous method involving full-wave simulation is used, the computation time is long, and the proper decision cannot be made. We compare the total amount of simulation time between the previous full-wave simulation method and the proposed CVDDM for the cases A and B shown in Figure 9. The simulation times of the previous and the proposed methods are 2761 seconds and 1470 seconds, respectively. The simulation time is substantially reduced up to 46.7%. Even though the reduced time is 1291 seconds, this is only considering two cases. In a real design process, there are so many cases of interest. Thereby, the time difference between the previous and proposed methods is too much larger. The time evaluation is summarized as shown in Table 4 in the revised manuscript.

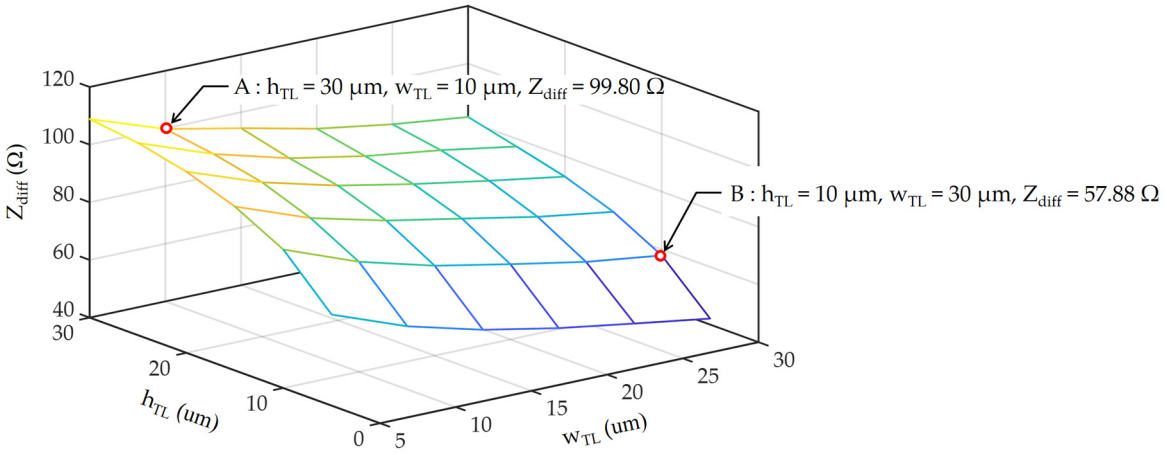

Figure 9. Example of design-space exploration using the rapid and efficient CVDDM.

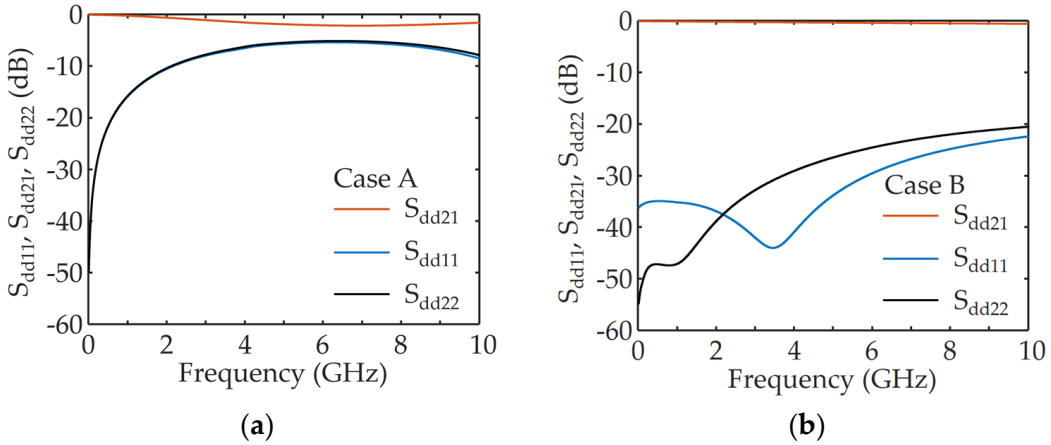

Figure 10. Mixed-mode S-parameters for (**a**) case A and (**b**) case B.

Table 4. Example of simulation time comparison.

	Full-WAVE Simulation	CVDDM	Reduced Time
Case A	1628 s	848 s	780 s (47.9%)
Case B	1133 s	622 s	511 s (45.1%)

Computation platform: Intel Xeon processor (3.2 GHz), 512 GB RAM (E5-2667 v4 @3.20 GHz, Intel, Santa Clara, CA, USA).

4. Conclusions

A hybrid design method called the CVDDM was proposed for efficient and practical design of high-speed IC-package interconnects. The proposed method combines DoE based on the Taguchi method, the DDM with the analytical recombination technique, and the FEM for the decomposed segments. The CVDDM was verified and demonstrated using a test structure of an IC-package interconnect. The CVDDM can significantly reduce the development time and is a systematic approach. Using the CVDDM, script-based design and automation of the IC-package interconnect can be achieved. In the future, the method will be incorporated with an in-house tool and extended to machine-learning-based package design.

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